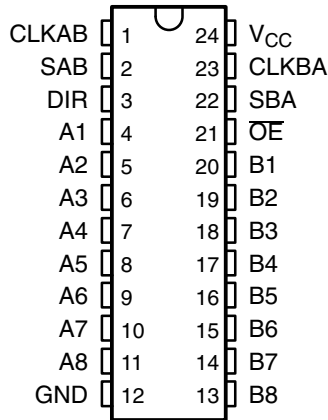


# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

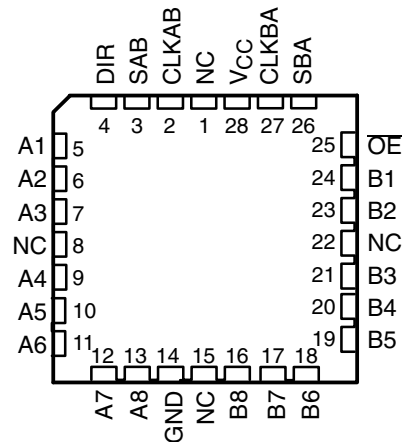
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- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54BCT646 . . . JT OR W PACKAGE  
SN74BCT646 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT646 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'BCT646 devices.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data can be stored in one register and/or B data can be stored in the other register.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – NT	Tube	SN74BCT646NT	BCT646
	SOIC – DW	Tube	SN74BCT646DW	
		Tape and reel	SN74BCT646DWR	
–55°C to 125°C	CDIP – JT	Tube	SNJ54BCT646JT	SNJ54BCT646JT
	CFP – W	Tube	SNJ54BCT646W	SNJ54BCT646W
	LCCC – FK	Tube	SNJ54BCT646FK	SNJ54BCT646FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54BCT646, SN74BCT646**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

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**description/ordering information(continued)**

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

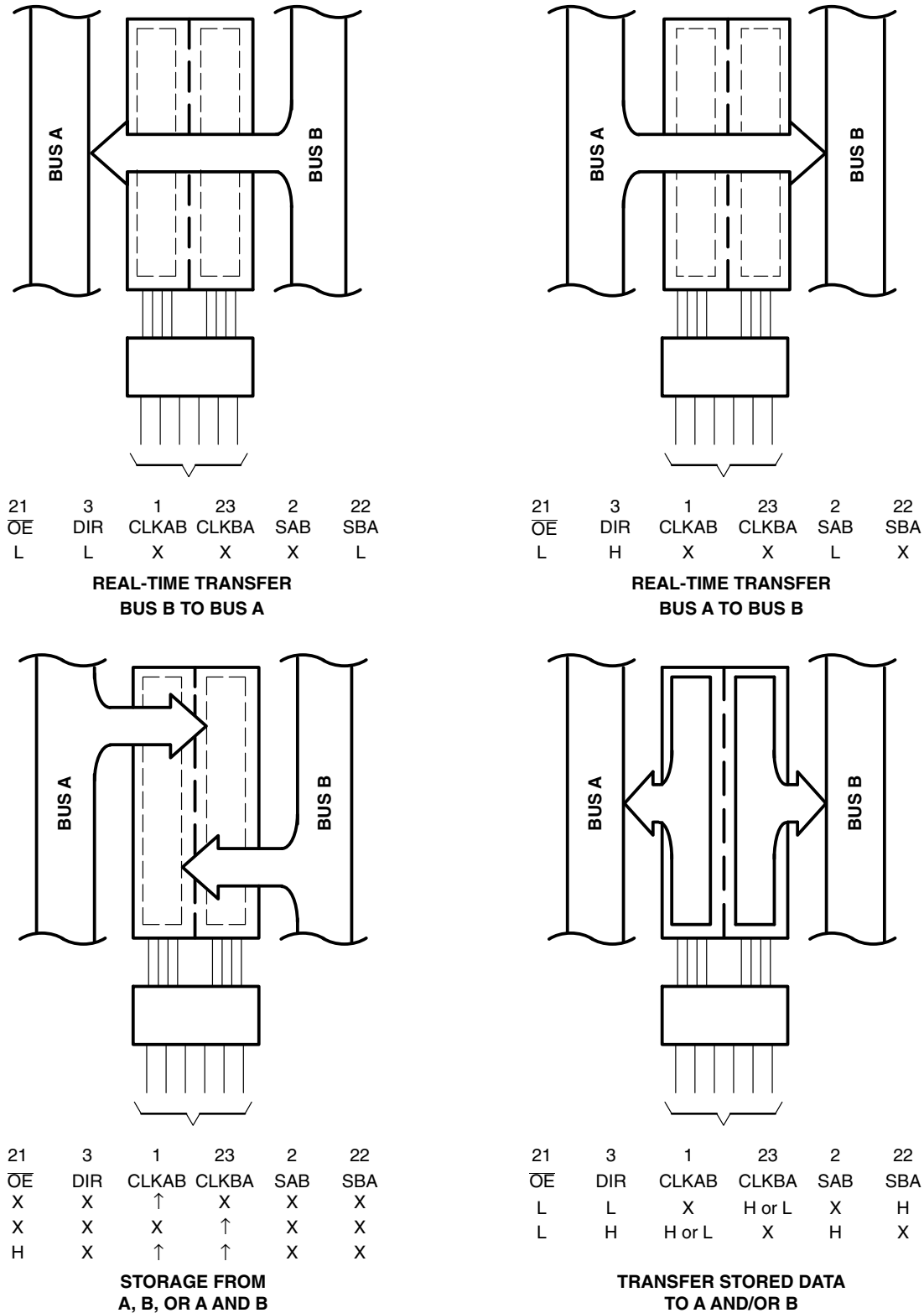
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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Pin numbers shown are for the DW, JT, NT, and W packages.

Figure 1. Bus-Management Functions



# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

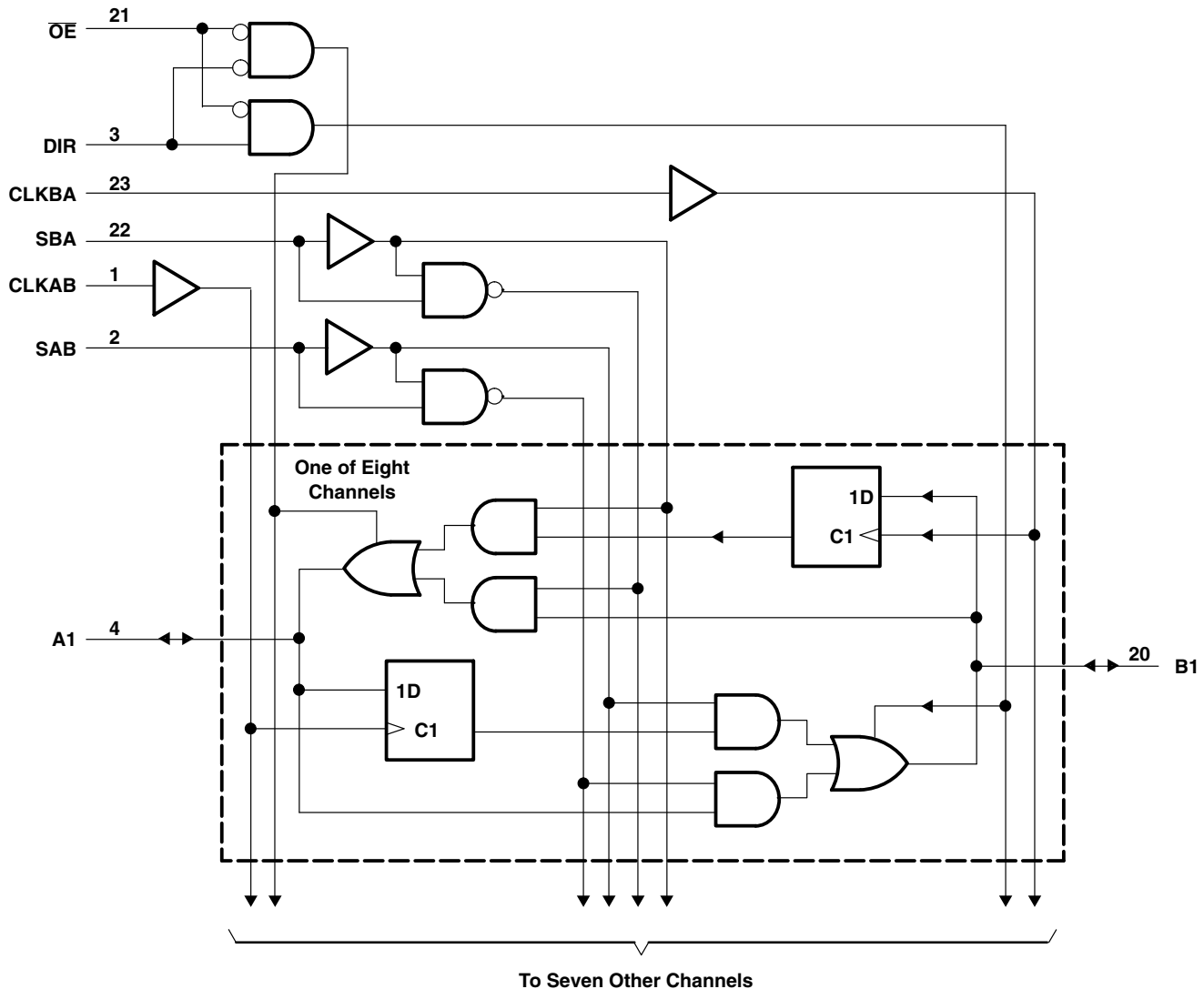
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FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.



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# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range: Control inputs (see Note 1) .....	–0.5 V to 7 V
I/O ports (see Note 1) .....	–0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ .....	–0.5 V to $V_{CC}$
Current into any output in the low state: SN54BCT646 .....	96 mA
SN74BCT646 .....	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	46°C/W
(see Note 3): NT package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-3.

## recommended operating conditions (see Note 4)

		SN54BCT646			SN74BCT646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT646			SN74BCT646			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		V
		$I_{OH} = -12\text{ mA}$	2	3.2					
		$I_{OH} = -15\text{ mA}$				2	3.1		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.38 0.55					V	
		$I_{OL} = 64\text{ mA}$			0.42 0.55				
$I_I$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V}$	1			1			mA
	Control inputs		1			1			
$I_{IH}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	70			70			$\mu\text{A}$
	Control inputs		20			20			
$I_{IL}^\ddagger$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$	-0.7			-0.7			mA
	Control inputs		-0.7			-0.7			
$I_{OS}^\S$		$V_{CC} = 5.5\text{ V}$ , $V_O = 0$	-100	-225		-100	-225		mA
$I_{CCL}$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = \text{GND}$	42	67		42	67		mA
$I_{CCH}$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = 4.5\text{ V}$	5.6	9		5.6	9		mA
$I_{CCZ}$	A or B port	$V_{CC} = 5.5\text{ V}$ , $V_I = \text{GND}$	10	16		10	16		mA
$C_i$	Control inputs	$V_{CC} = 5\text{ V}$ , $V_I = 2.5\text{ V}$ or $0.5\text{ V}$	6		6		6		pF
$C_{io}$	A or B port	$V_{CC} = 5\text{ V}$ , $V_O = 2.5\text{ V}$ or $0.5\text{ V}$	12		14		14		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54BCT646		SN74BCT646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	83		83		83		MHz
$t_w$	Pulse duration, CLK high or low	6		6		6		ns
$t_{su}$	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	6		7		6		ns
$t_h$	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	0.5		0.5		0.5		ns



# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54BCT646		SN74BCT646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			83			83		83		MHz
$t_{PLH}$	CLKBA or CLKAB	A or B	3.6	7	9.4	3.6	12.4	3.6	11.2	ns
$t_{PHL}$			3.9	7	9.2	3.9	11.5	3.9	10.6	
$t_{PLH}$	A or B	B or A	3.1	6	8.1	3.1	11.1	3.1	9.5	ns
$t_{PHL}$			3.7	6.8	8.9	3.7	12.1	3.7	10.5	
$t_{PLH}$	SAB or SBA <sup>†</sup> (with A or B high)	A or B	4.5	8.8	11.2	4.5	15.2	4.5	13.8	ns
$t_{PHL}$			3.3	6	8.1	3.3	9.8	3.3	9.1	
$t_{PLH}$	SAB or SBA <sup>†</sup> (with A or B low)	A or B	3.9	7.7	10.2	3.9	13.3	3.9	12	ns
$t_{PHL}$			4.7	8.3	10.8	4.7	13.7	4.7	12.9	
$t_{PZH}$	$\overline{OE}$	A or B	4	7.9	10.7	4	14	4	13.2	ns
$t_{PZL}$			4.6	8.8	11.8	4.6	15.4	4.6	14.4	
$t_{PHZ}$	$\overline{OE}$	A or B	4	7.2	9.4	4	12	4	10.9	ns
$t_{PLZ}$			3.4	7	9.3	3.4	11.6	3.4	10.5	
$t_{PZH}$	DIR	A or B	2.8	7.8	10.7	2.8	14	2.8	13.1	ns
$t_{PZL}$			3.8	8.9	11.9	3.8	15.6	3.8	14.6	
$t_{PHZ}$	DIR	A or B	3.8	8.4	10.7	3.8	13.2	3.8	12.6	ns
$t_{PLZ}$			3.2	7.3	9.9	3.2	12.6	3.2	11.8	

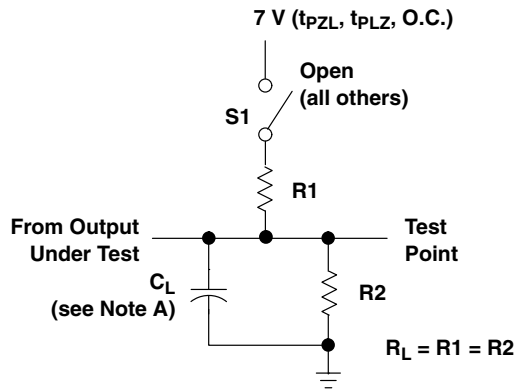
<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite that of the bus input.



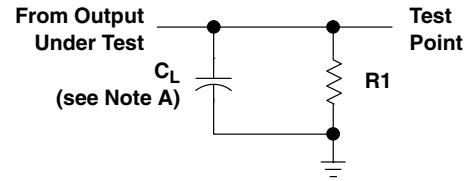
# SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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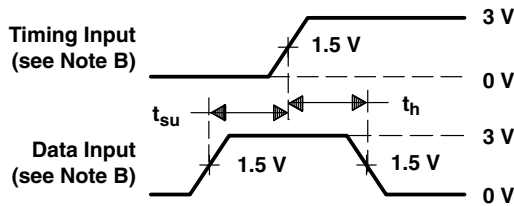
## PARAMETER MEASUREMENT INFORMATION



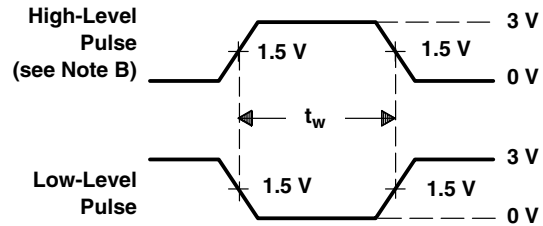
LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS



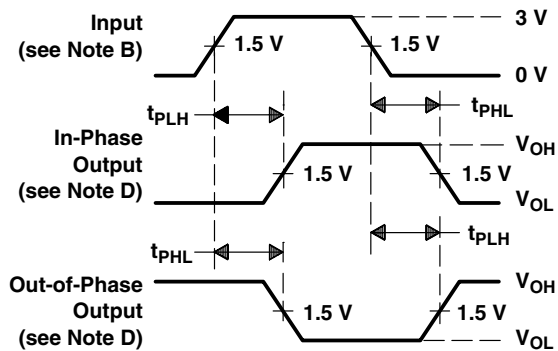
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



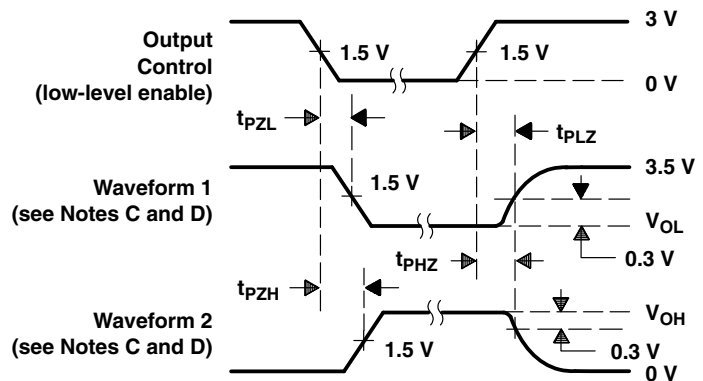
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.
- C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9155501M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9155501MKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9155501MLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN74BCT646DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT646NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT646NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54BCT646FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT646JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SNJ54BCT646W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

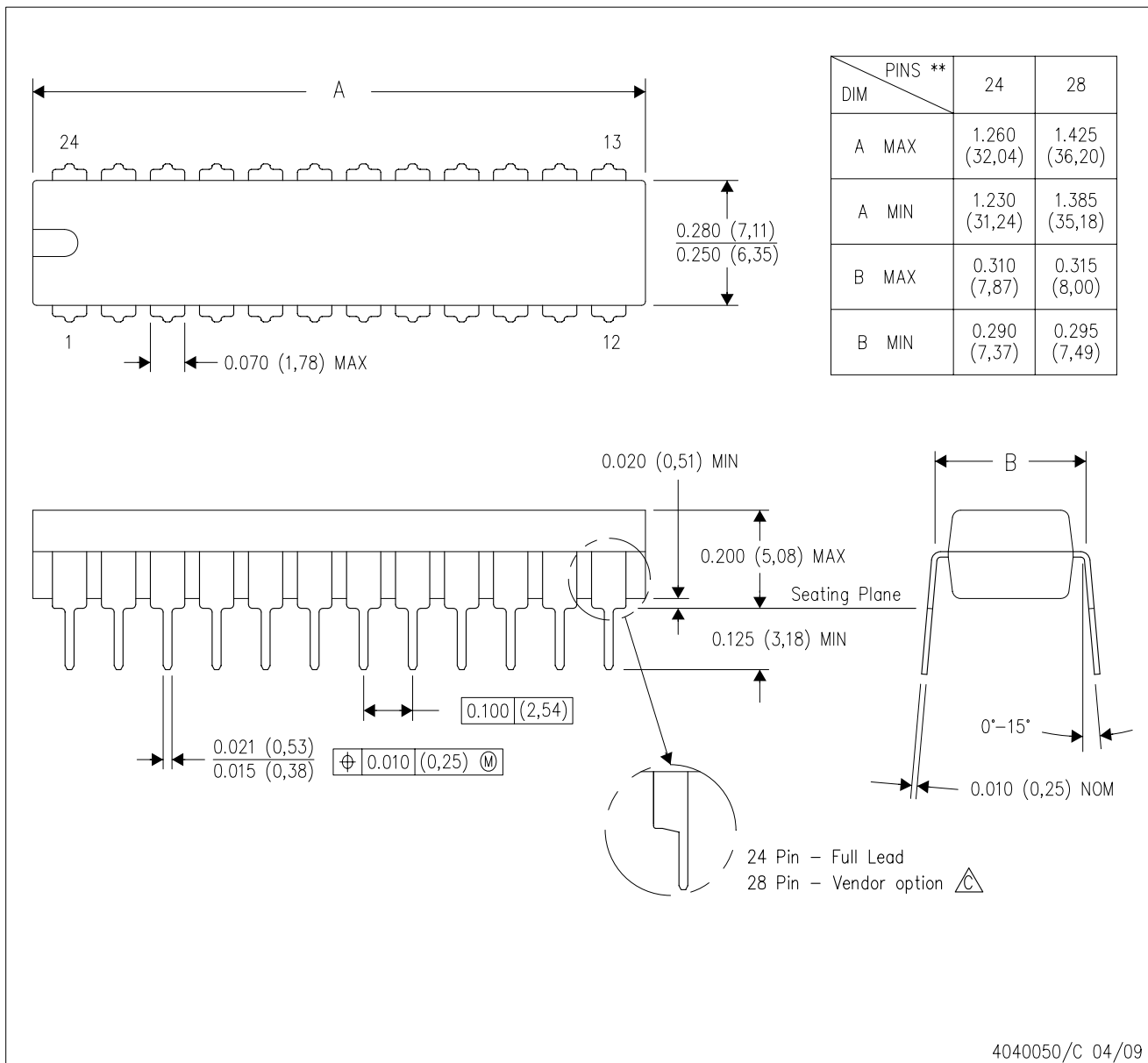
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004


# MECHANICAL DATA

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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