

# SN75476 THRU SN75478 DUAL PERIPHERAL DRIVERS

SLRS025A – DECEMBER 1976 – REVISED NOVEMBER 1995

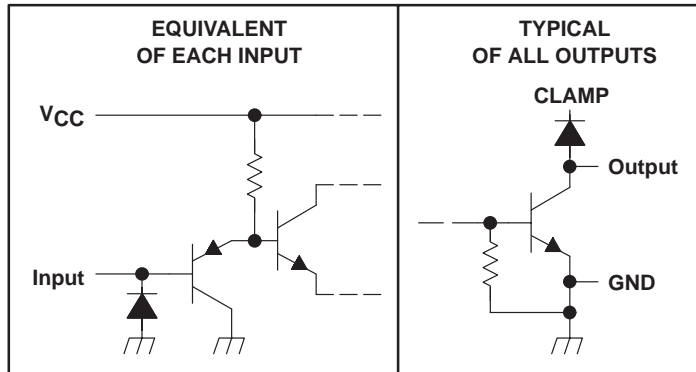
- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typ)
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- pnp Transistor Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Plastic DIP (P) With Copper-Lead Frame Provides Cooler Operation and Improved Reliability

## description

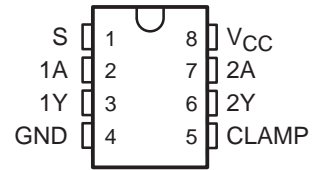
The SN75476 through SN75478 are dual peripheral drivers designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, and SN75478 provide AND, NAND, and OR drivers respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, and SN75478 drivers are characterized for operation from 0°C to 70°C.

## schematics of inputs and outputs



D OR P PACKAGE  
(TOP VIEW)



## Function Tables

SN75476  
(each AND driver)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75477  
(each NAND driver)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75478  
(each OR driver)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

H = high level, L = low level  
X = irrelevant

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

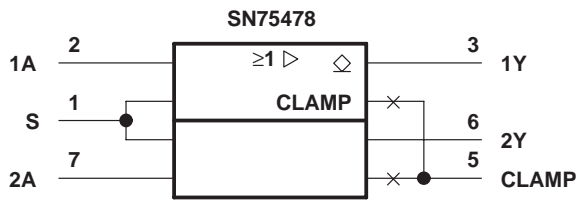
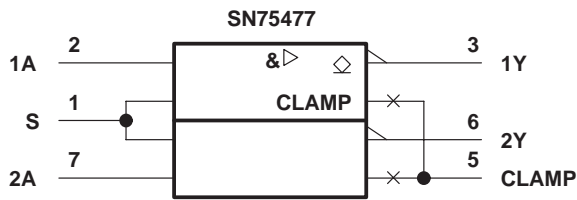
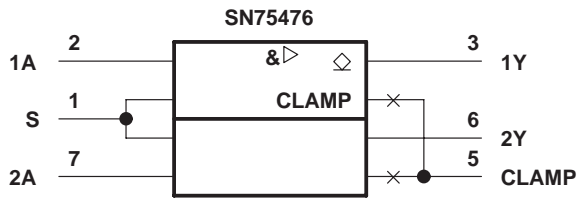


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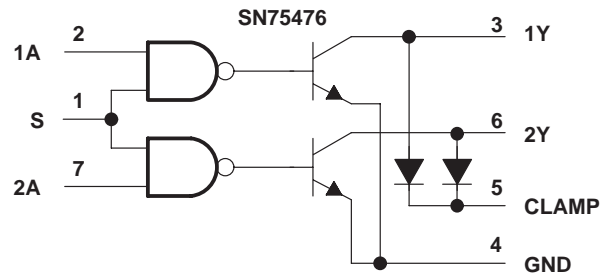
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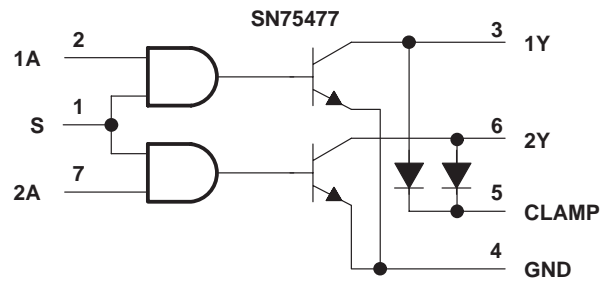
## logic symbols†



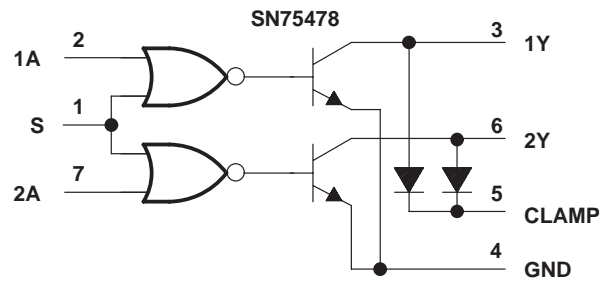
## logic diagrams (positive logic)



Positive Logic:  $Y = AS$  or  $\overline{A+S}$



Positive Logic:  $Y = \overline{AS}$  or  $\overline{A+S}$



Positive Logic:  $Y = A+S$  or  $\overline{\overline{A} \overline{S}}$

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

# SN75476 THRU SN75478 DUAL PERIPHERAL DRIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	5.5 V
Continuous output current (see Note 2)	400 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$	500 mA
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$	3 A
Output clamp current, $I_{OK}$	400 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- NOTES: 1. Voltage values are with respect to network GND.  
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous power dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.5	5	5.5	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Operating free-air temperature, $T_A$	0		70	°C



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## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -12 mA		-0.95	-1.5		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	I <sub>OL</sub> = 100 mA	0.16	0.3		V
			I <sub>OL</sub> = 175 mA	0.22	0.5		
			I <sub>OL</sub> = 300 mA	0.33	0.6		
V <sub>O(BR)</sub>	Output breakdown voltage	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = 100 μA	70	100		V
V <sub>R(K)</sub>	Output clamp reverse voltage	V <sub>CC</sub> = 4.5 V,	I <sub>R</sub> = 100 μA	70	100		V
V <sub>F(K)</sub>	Output clamp forward voltage	V <sub>CC</sub> = 4.5 V,	I <sub>F</sub> = 300 mA	0.8	1.15	1.6	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V, V <sub>IL</sub> = 0.8 V,	V <sub>IH</sub> = 2 V, V <sub>OH</sub> = 70 V		1	100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V		0.01	10	μA
I <sub>IL</sub>	Low-level input current	A input	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.8 V		-80	-110	μA
		S input			-160	-220	
I <sub>CCH</sub>	Supply current, outputs high	SN75476	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5 V	10	17	mA
		SN75477		V <sub>I</sub> = 0	10	17	
		SN75478		V <sub>I</sub> = 5 V	10	17	
I <sub>CCL</sub>	Supply current, outputs low	SN75476	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 0	54	75	mA
		SN75477		V <sub>I</sub> = 5 V	54	75	
		SN75478		V <sub>I</sub> = 0	54	75	

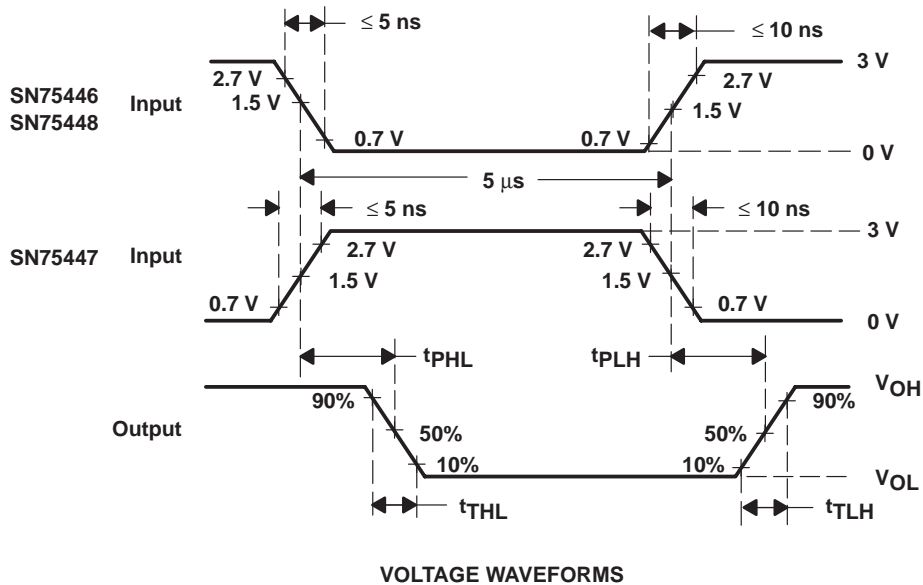
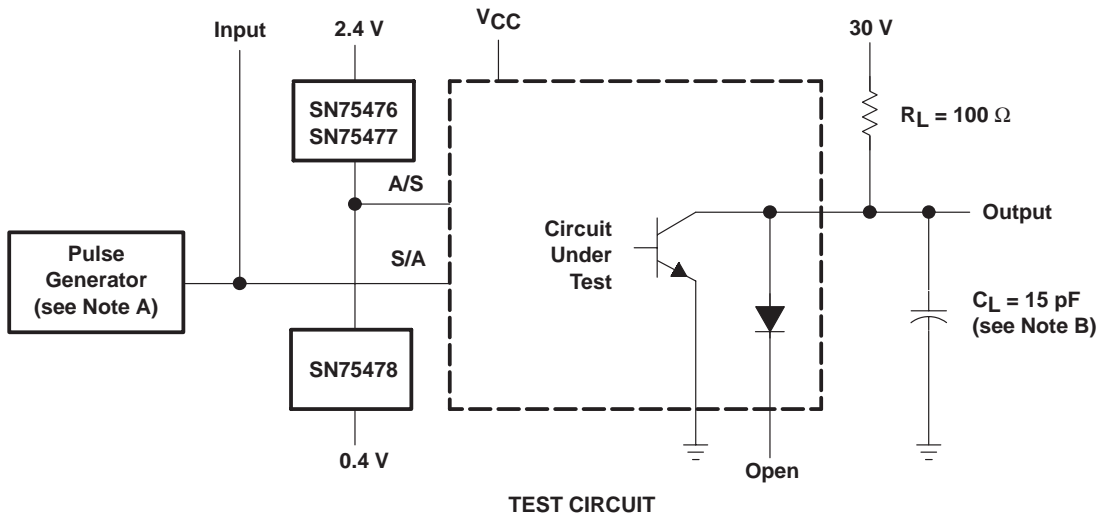
† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 100 Ω, See Figure 1			200	350	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output				200	350	ns
t <sub>TLH</sub>	Transition time, low-to-high-level output				50	125	ns
t <sub>THL</sub>	Transition time, high-to-low-level output				90	125	ns
V <sub>OH</sub>	High-level output voltage after switching	V <sub>S</sub> = 55 V, See Figure 2	I <sub>O</sub> ≈ 300 mA,	V <sub>S</sub> -18			mV



## PARAMETER MEASUREMENT INFORMATION



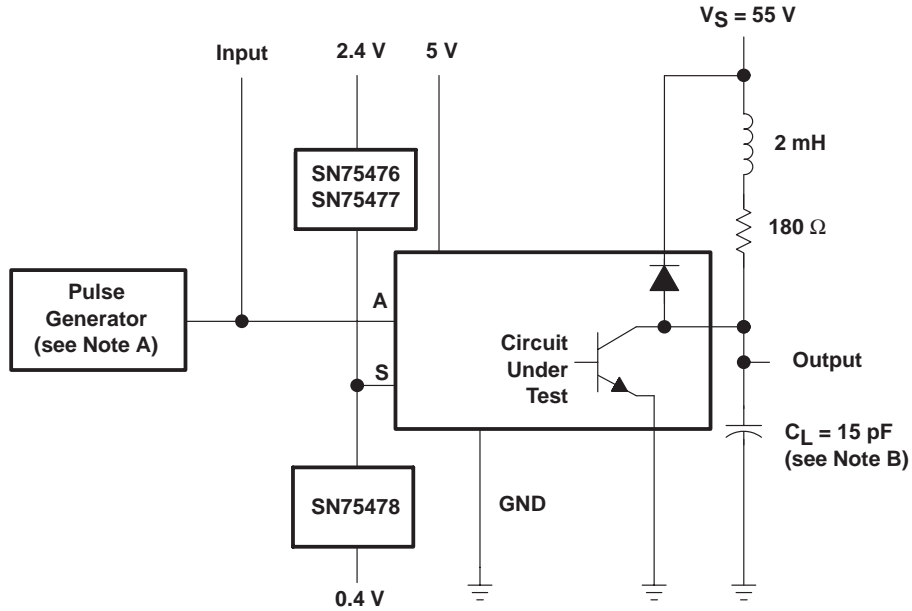
- NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics**

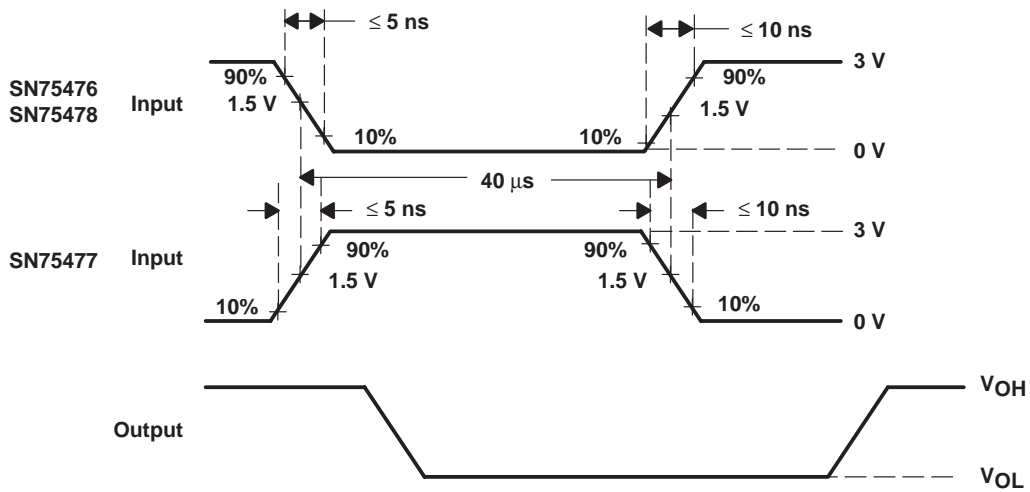
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## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_0 = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75476D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
SN75476DR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
SN75476P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
SN75477D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75477DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75477DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75477DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75477DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75477DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75477P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75477PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75478D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
SN75478P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75478PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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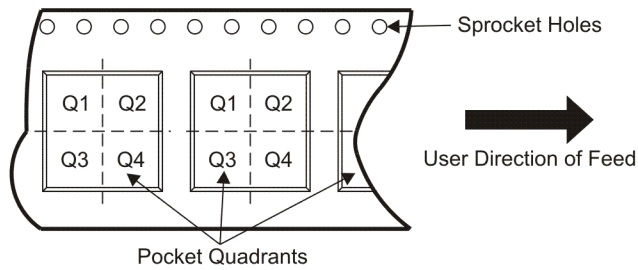
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75477DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

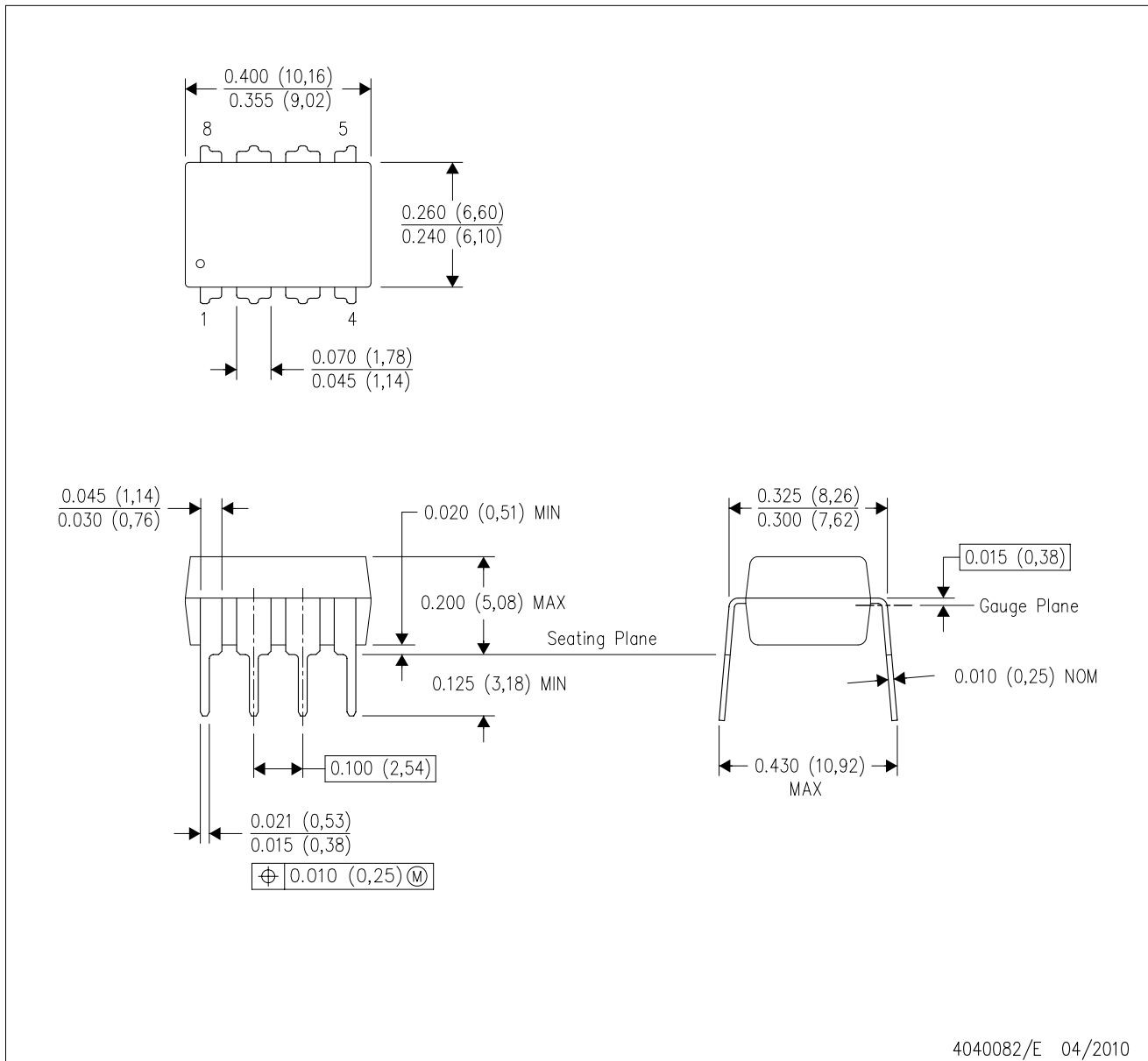


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75477DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

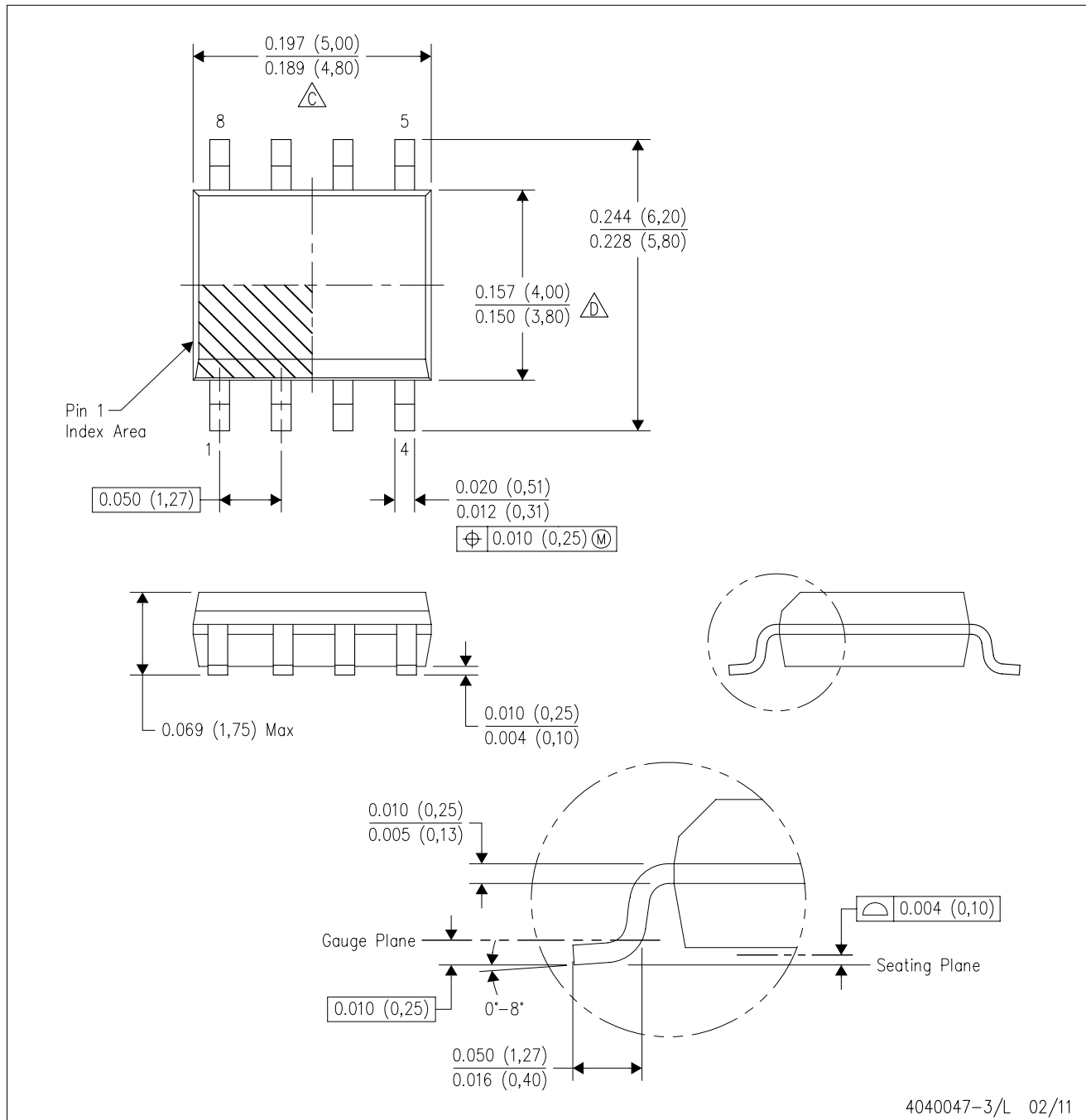
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

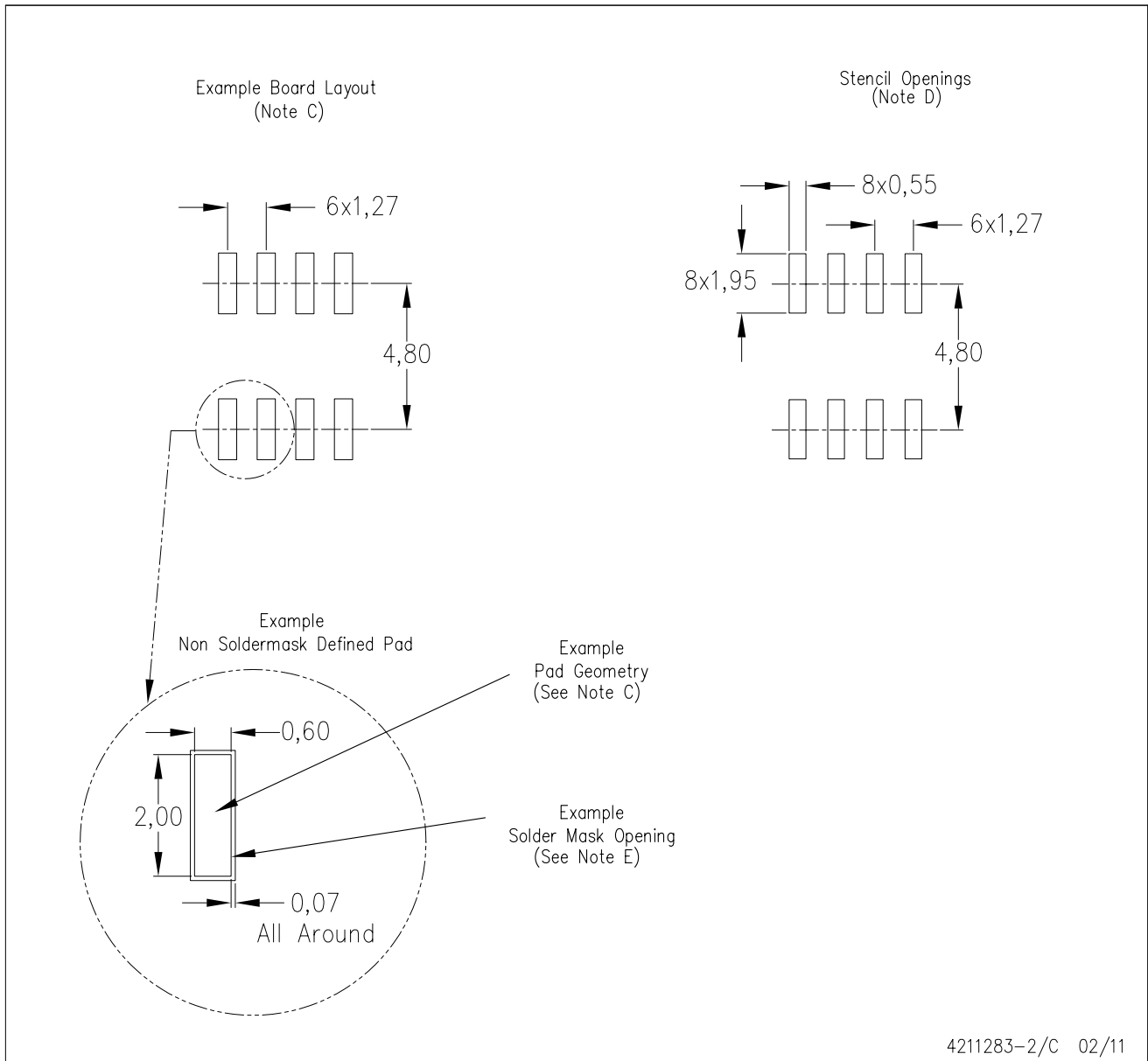
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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