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Jameco Part Number 1053260

SN55115, SN75115 DUAL DIFFERENTIAL RECEIVERS

SLLS072D – SEPTEMBER 1973 – REVISED MAY 1998

- Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual-Channel Operation
- TTL Compatible
- ± 15 -V Common-Mode Input Voltage Range
- Optional-Use Built-In 130- Ω Line-Terminating Resistor
- Individual Frequency-Response Controls
- Individual Channel Strobes
- Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers
- Designed to Be Interchangeable With National DS9615 Line Receivers

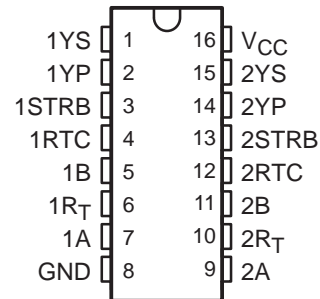
description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay.

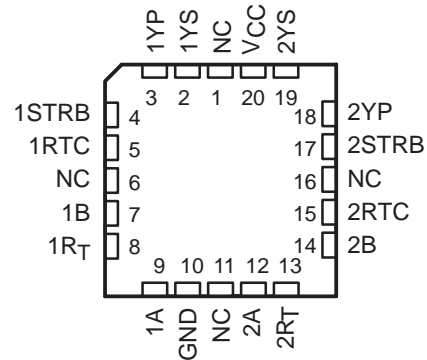
The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

The SN55115 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75115 is characterized for operation from 0°C to 70°C .

SN55115 . . . J OR W PACKAGE
SN75115 . . . N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

STRB	DIFF INPUT (A AND B)	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH \text{ min}}$ or V_{ID} more positive than $V_{T+ \text{ max}}$
L = $V_I \leq V_{IL \text{ max}}$ or V_{ID} more negative than $V_{T- \text{ max}}$
X = irrelevant



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 **TEXAS
INSTRUMENTS**

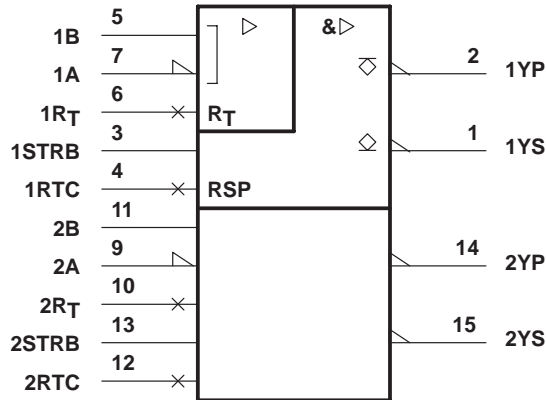
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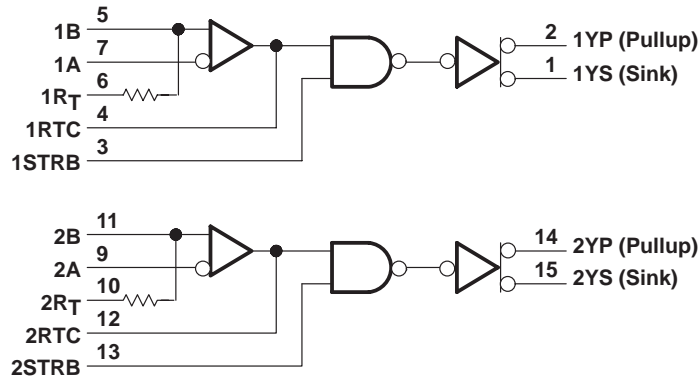
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logic symbol†

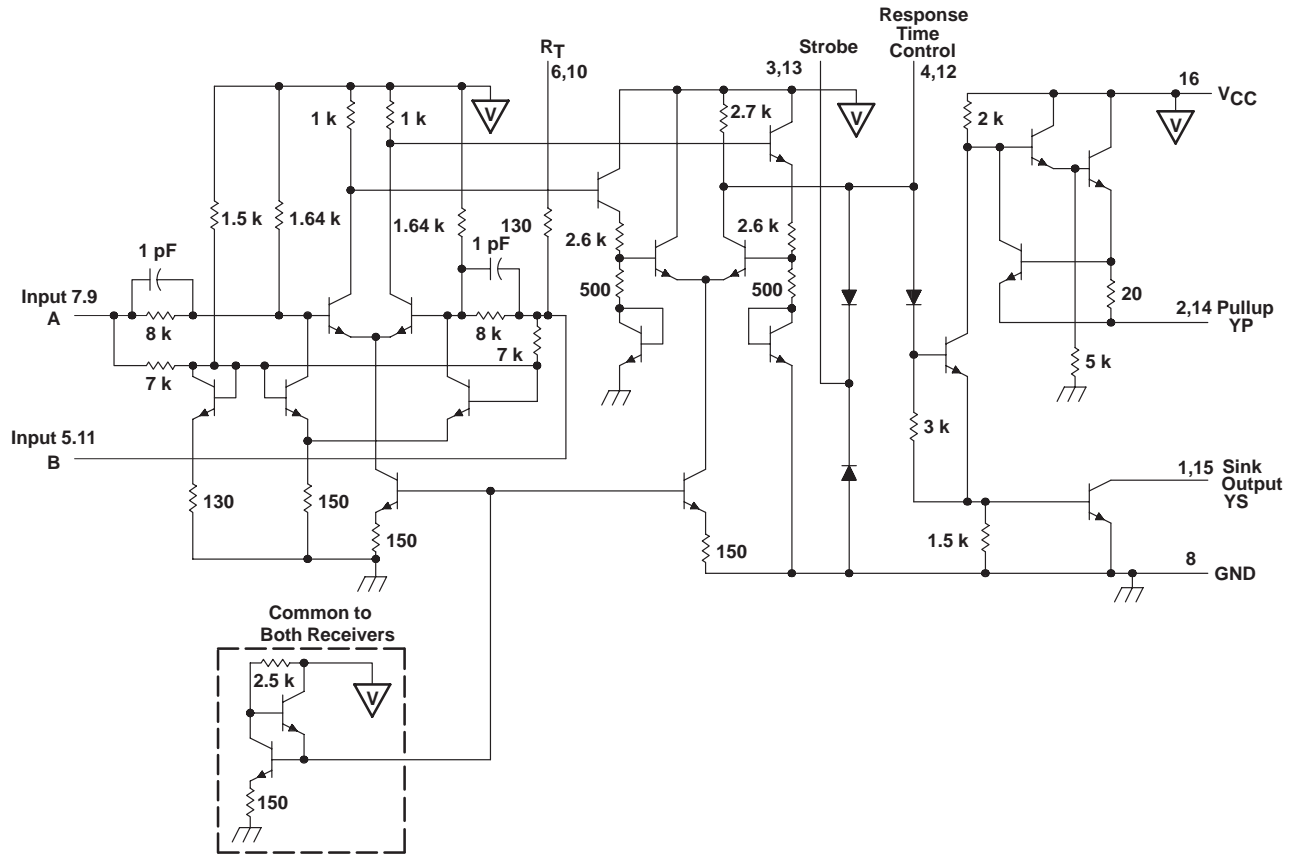


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values are nominal and in ohms.
Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage V_I (A, B, and R_T)	± 25 V
Input voltage V_I (STRB)	5.5 V
Off-state voltage applied to open-collector outputs	14 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{Stg}	-65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input voltage, are with respect to network ground terminal.

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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK, J, and W packages, SN55115 chips are either silver glass or alloy mounted. SN75115 chips are glass mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at STRB, V_{IH}	2.4			2.4			V
Low-level input voltage at STRB, V_{IL}	0.4			0.4			V
High-level output current, I_{OH}	-5			-5			mA
Low-level output current, I_{OL}	15			15			mA
Operating free-air temperature, T_A	-55			125			°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55115			SN75115			UNIT			
		MIN	TYP‡	MAX	MIN	TYP‡	MAX				
V_{IT+} §	Positive-going threshold voltage $V_O = 0.4$ V, $I_{OL} = 15$ mA, $V_{IC} = 0$	500			500			mV			
V_{IT-} §	Negative-going threshold voltage $V_O = 2.4$ V, $I_{OH} = -5$ mA, $V_{IC} = 0$	-500¶			-500¶			mV			
V_{ICR}	Common-mode input voltage range $V_{ID} = \pm 1$ V	+15 to -15	+24 to -19		+15 to -15	+24 to -19		V			
V_{OH}	High-level output voltage $V_{CC} = \text{MIN}$, $I_{OH} = -5$ mA, $V_{ID} = -0.5$ V	$T_A = \text{MIN}$		2.2	2.4		V				
		$T_A = 25^\circ\text{C}$		2.4	3.4	2.4		3.4			
		$T_A = \text{MAX}$		2.4	2.4						
V_{OL}	Low-level output voltage $V_{CC} = \text{MIN}$, $I_{OL} = 15$ mA, $V_{ID} = -0.5$ V	0.22		0.4	0.22		0.45	V			
I_{IL}	Low-level input current $V_{CC} = \text{MAX}$, $V_I = 0.4$ V, Other input at 5.5 V	$T_A = \text{MIN}$		-0.9		-0.9		mA			
		$T_A = 25^\circ\text{C}$		-0.5	-0.7	-0.5	-0.7				
		$T_A = \text{MAX}$		-0.7		-0.7					
I_{SH}	High-level strobe current $V_{CC} = \text{MIN}$, $V_{ID} = -0.5$ V, $V_{\text{strobe}} = 4.5$ V	$T_A = 25^\circ\text{C}$		2		5		μA			
		$T_A = \text{MAX}$		5		10					
I_{SL}	Low-level strobe current $V_{CC} = \text{MAX}$, $V_{ID} = 0.5$ V, $V_{\text{strobe}} = 0.4$ V	$T_A = 25^\circ\text{C}$		-1.15	-2.4	-1.15	-2.4	mA			
$I_{(RTC)}$	Response-time-control current $V_{CC} = \text{MAX}$, $V_{ID} = 0.5$ V, $V_{RC} = 0$	$T_A = 25^\circ\text{C}$		-1.2	-3.4	-1.2	-3.4	mA			
$I_{O(\text{off})}$	Off-state open-collector output current $V_{CC} = \text{MIN}$, $V_{ID} = -4.5$ V, $V_{OH} = 12$ V	$T_A = 25^\circ\text{C}$		100				μA			
		$T_A = \text{MAX}$		200							
	$V_{CC} = \text{MIN}$, $V_{ID} = -4.75$ V, $V_{OH} = 5.25$ V	$T_A = 25^\circ\text{C}$				100					
		$T_A = \text{MAX}$				200					
R_T	Line-terminating resistance $V_{CC} = 5$ V	$T_A = 25^\circ\text{C}$		77	130	167	74	130	179	Ω	
I_{OS}	Supply-circuit output current# $V_{CC} = \text{MAX}$, $V_{ID} = -0.5$ V, $V_O = 0$	$T_A = 25^\circ\text{C}$		-15	-40	-80	-14	-40	-100	mA	
I_{CC}	Supply current (both receivers) $V_{CC} = \text{MAX}$, $V_{ID} = 0.5$ V, $V_{IC} = 0$	$T_A = 25^\circ\text{C}$		32		50		32		50	mA

† Unless otherwise noted, $V_{\text{strobe}} = 2.4$ V. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output.

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, and $V_{IC} = 0$.

§ Differential voltages are at the B input terminal with respect to the A input terminal.

¶ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.



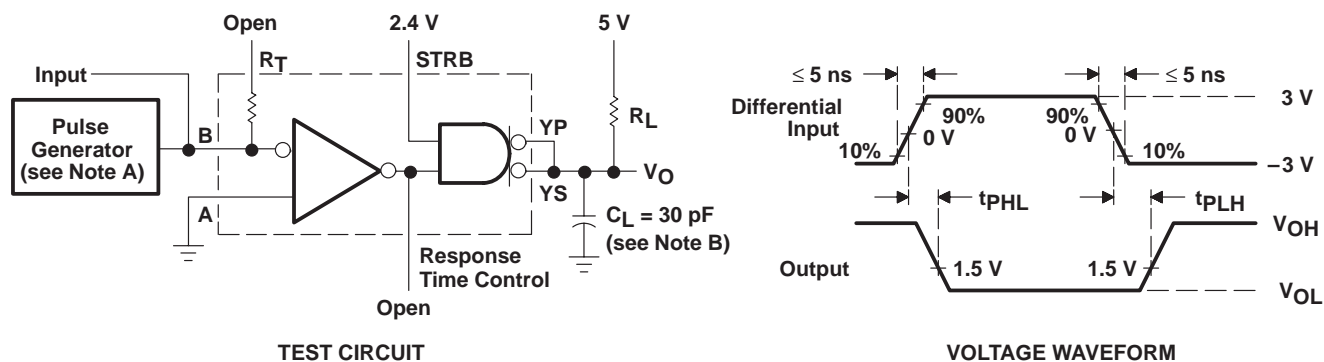
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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 30\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	SN55115			SN75115			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high level output	$R_L = 3.9\text{ k}\Omega$, See Figure 1		18	50		18	75	ns
t_{PHL} Propagation delay time, high-to-low level output	$R_L = 390\ \Omega$, See Figure 1		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $PRR \leq 500\text{ kHz}$, $t_w \leq 100\text{ ns}$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

INPUT CURRENT
vs
INPUT VOLTAGE

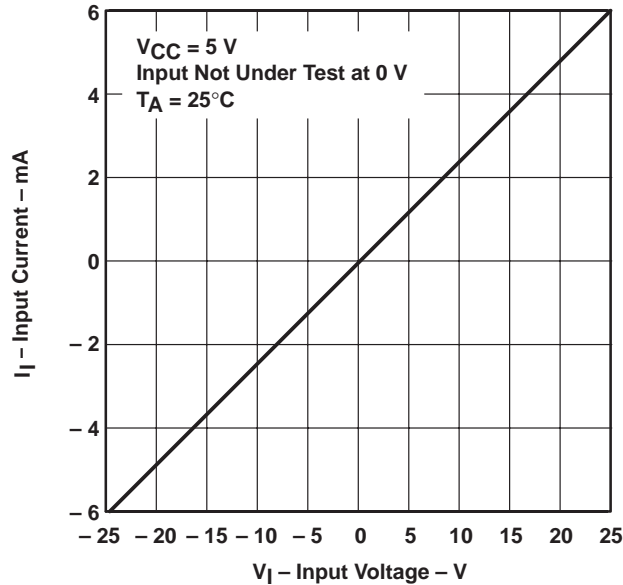


Figure 2

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

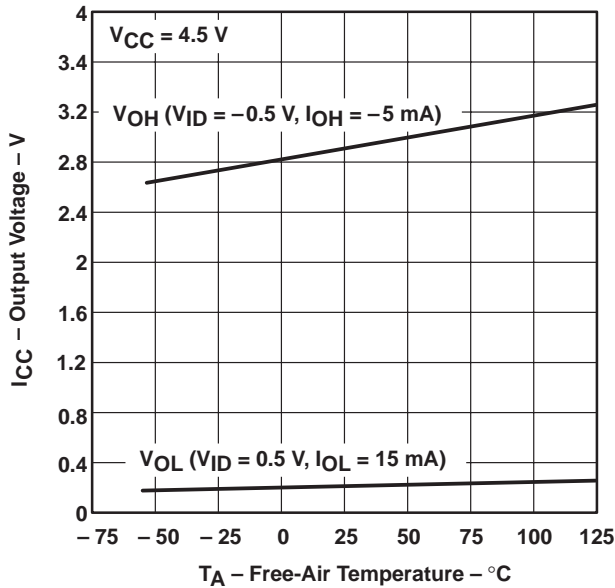


Figure 3

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

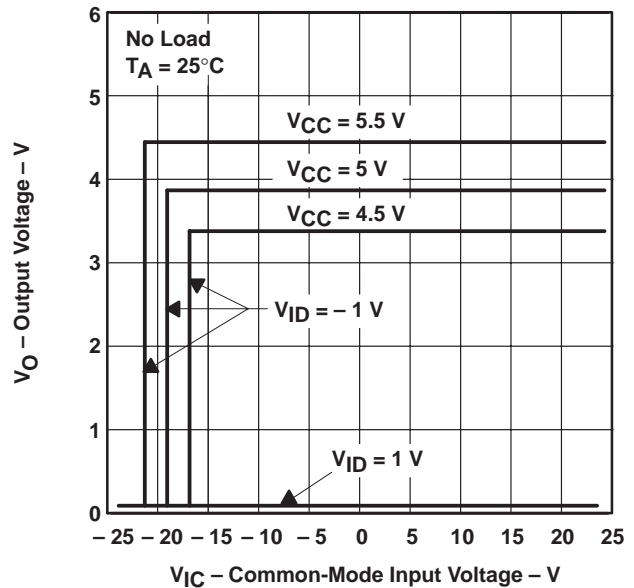


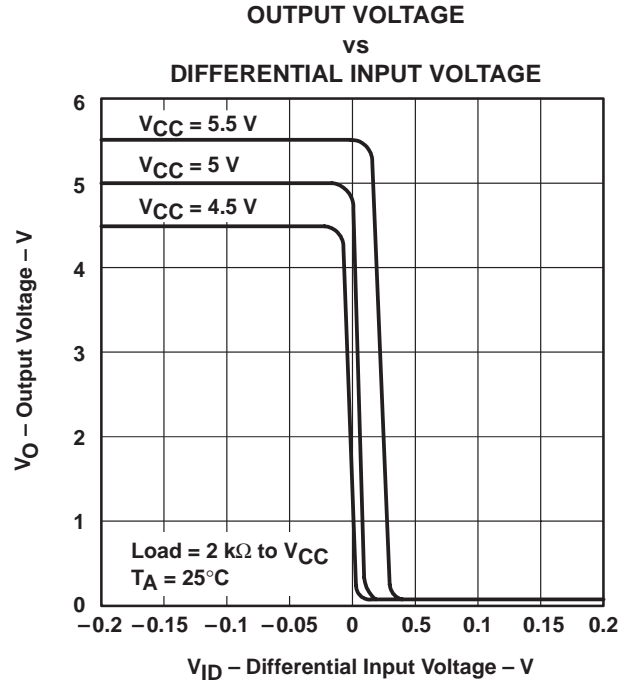
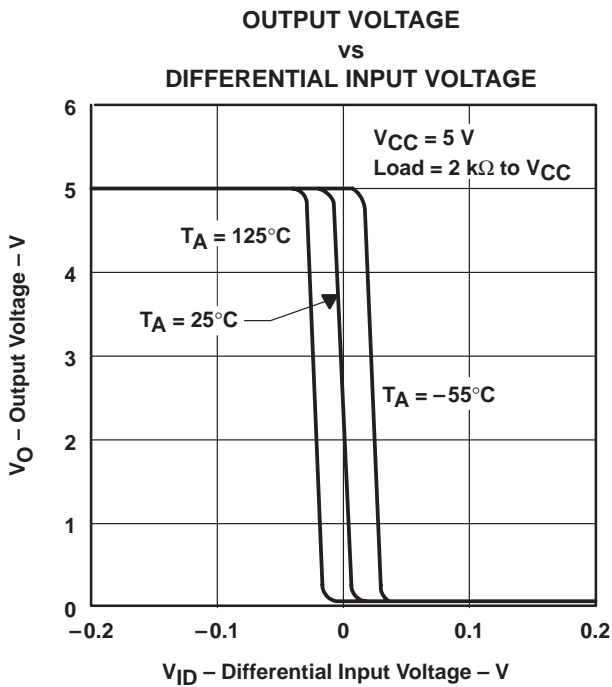
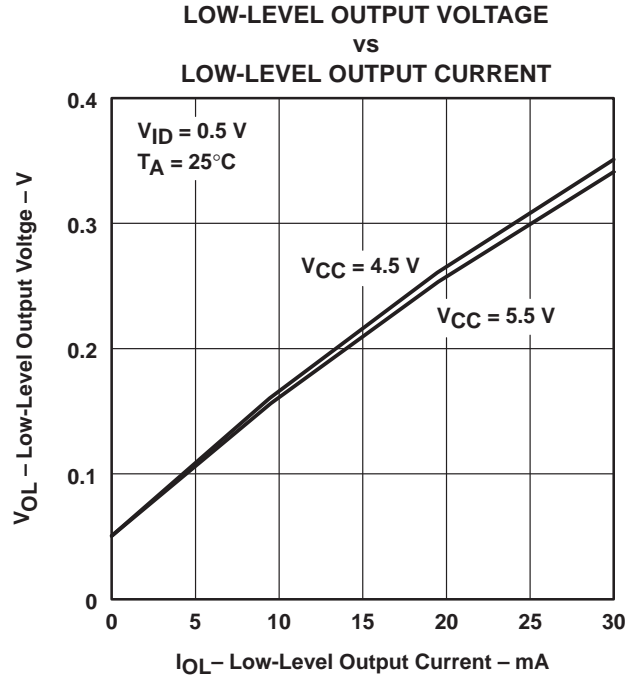
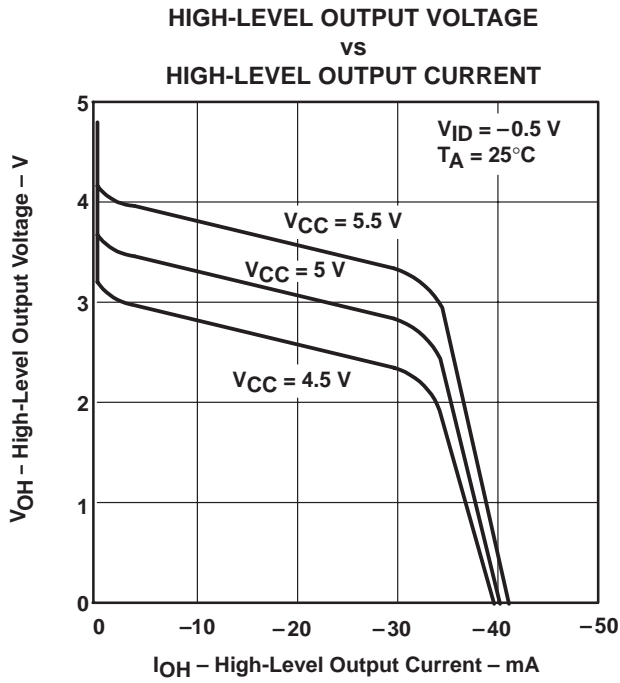
Figure 4

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS†

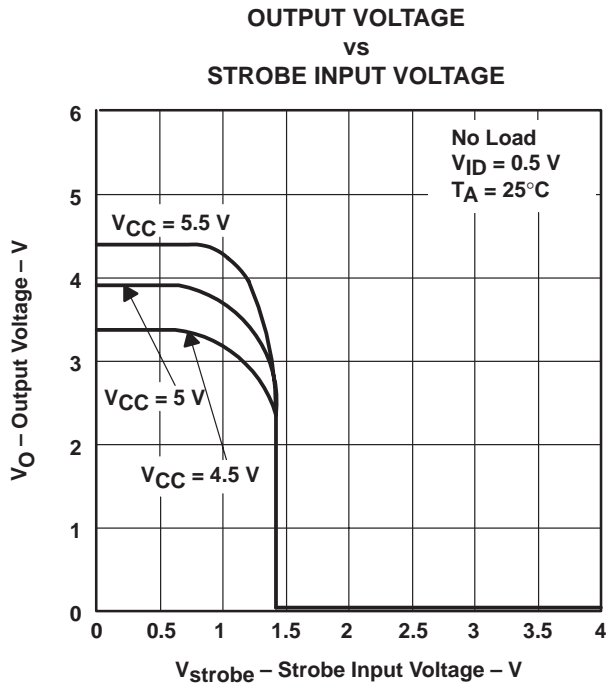


Figure 9

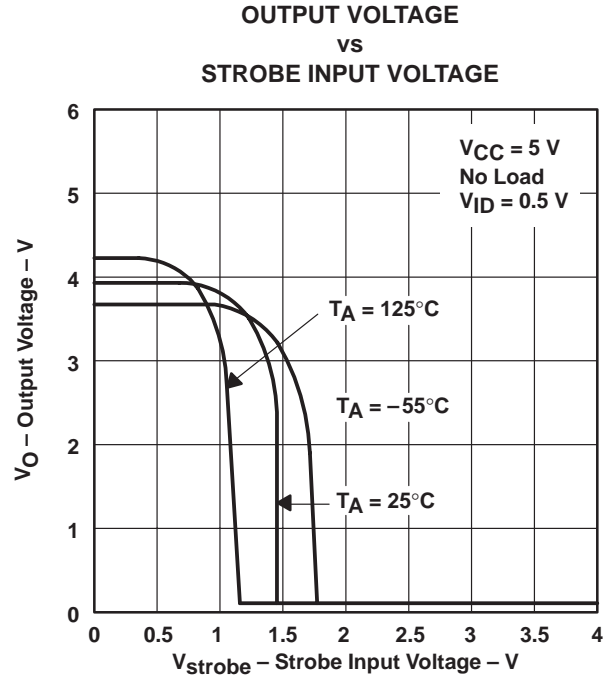


Figure 10

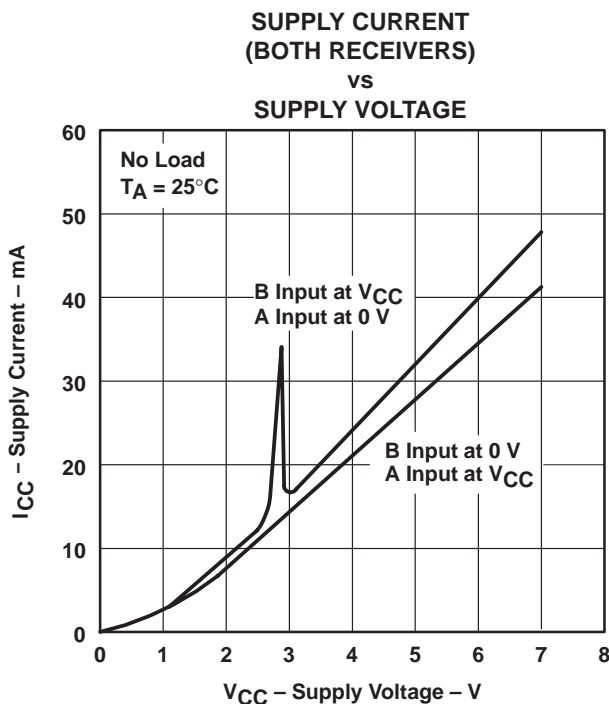


Figure 11

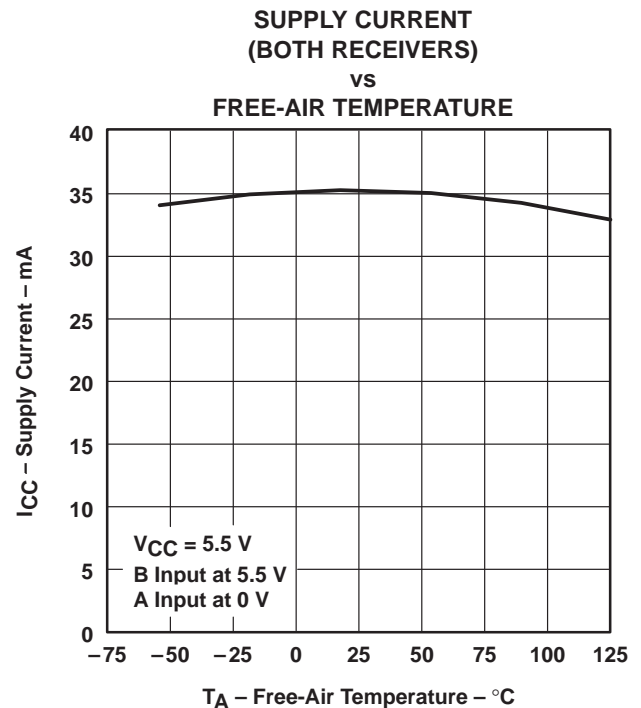


Figure 12

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

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TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

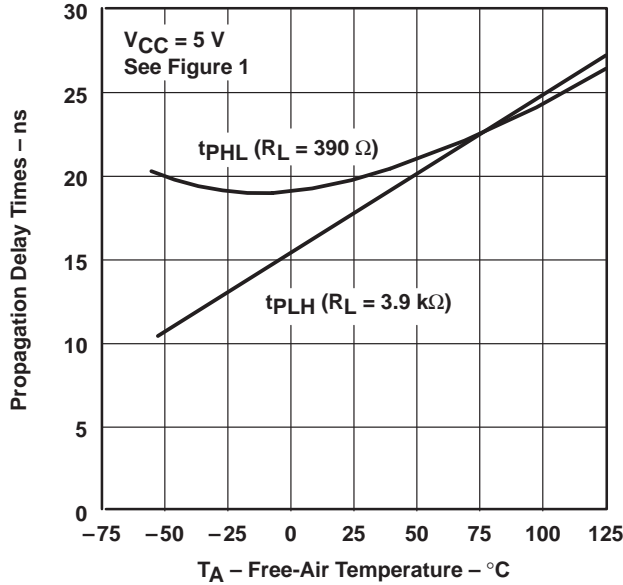


Figure 13

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

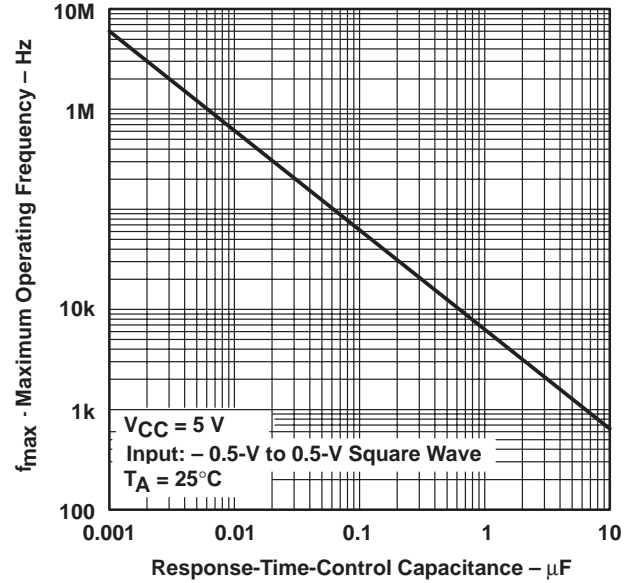
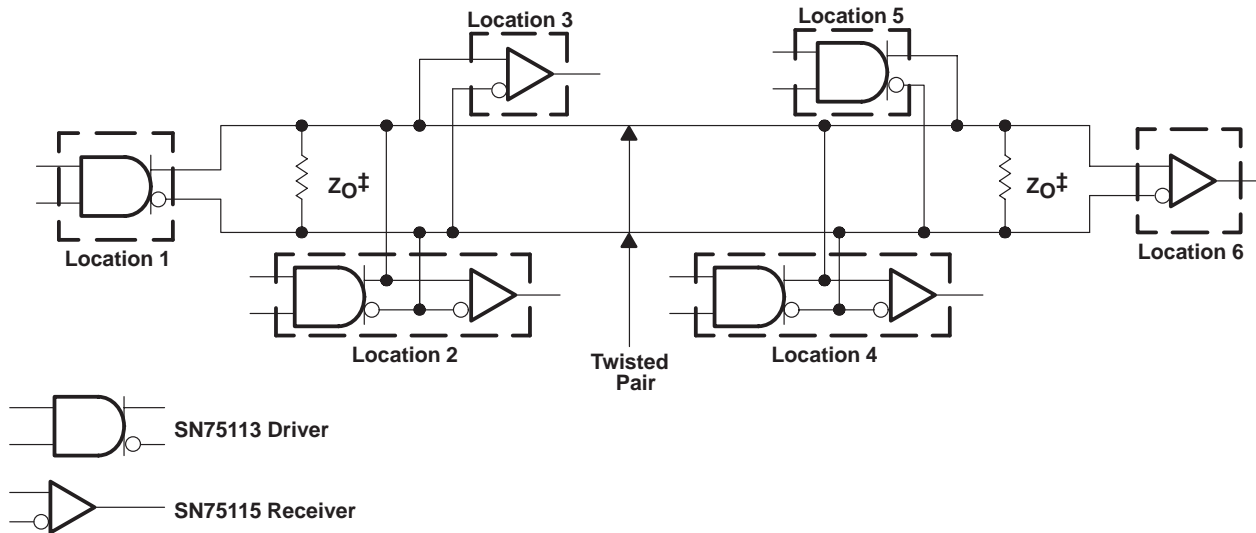


Figure 14

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



‡ $Z_O = R_T$. A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 15. Basic Party-Line or Data-Bus Differential Data Transmission

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-88745012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-88745012A-T	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8874501FA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/10404BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN55115J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN75115D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75115NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75115NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75115NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ55115FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55115J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55115W	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

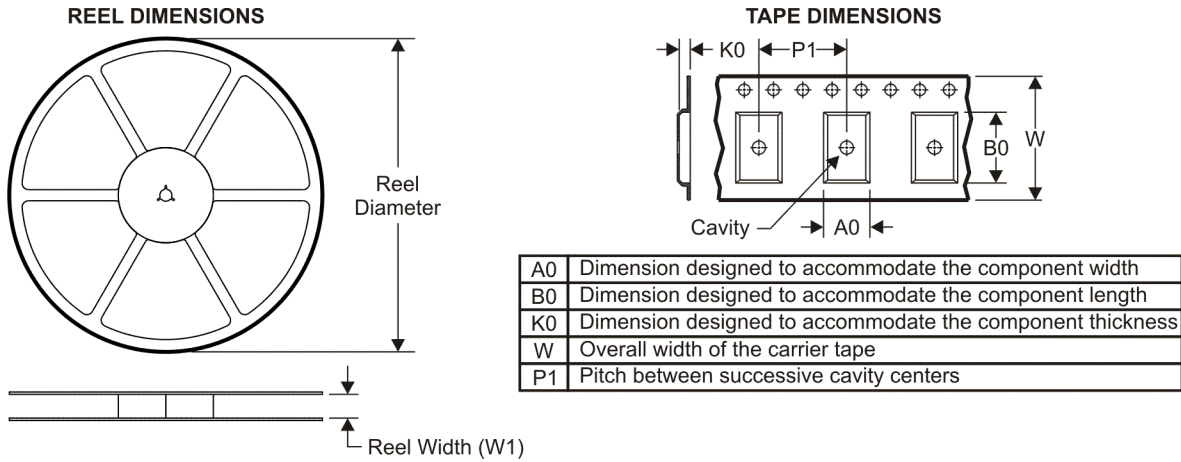
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75115DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75115NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75115DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75115NSR	SO	NS	16	2000	346.0	346.0	33.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

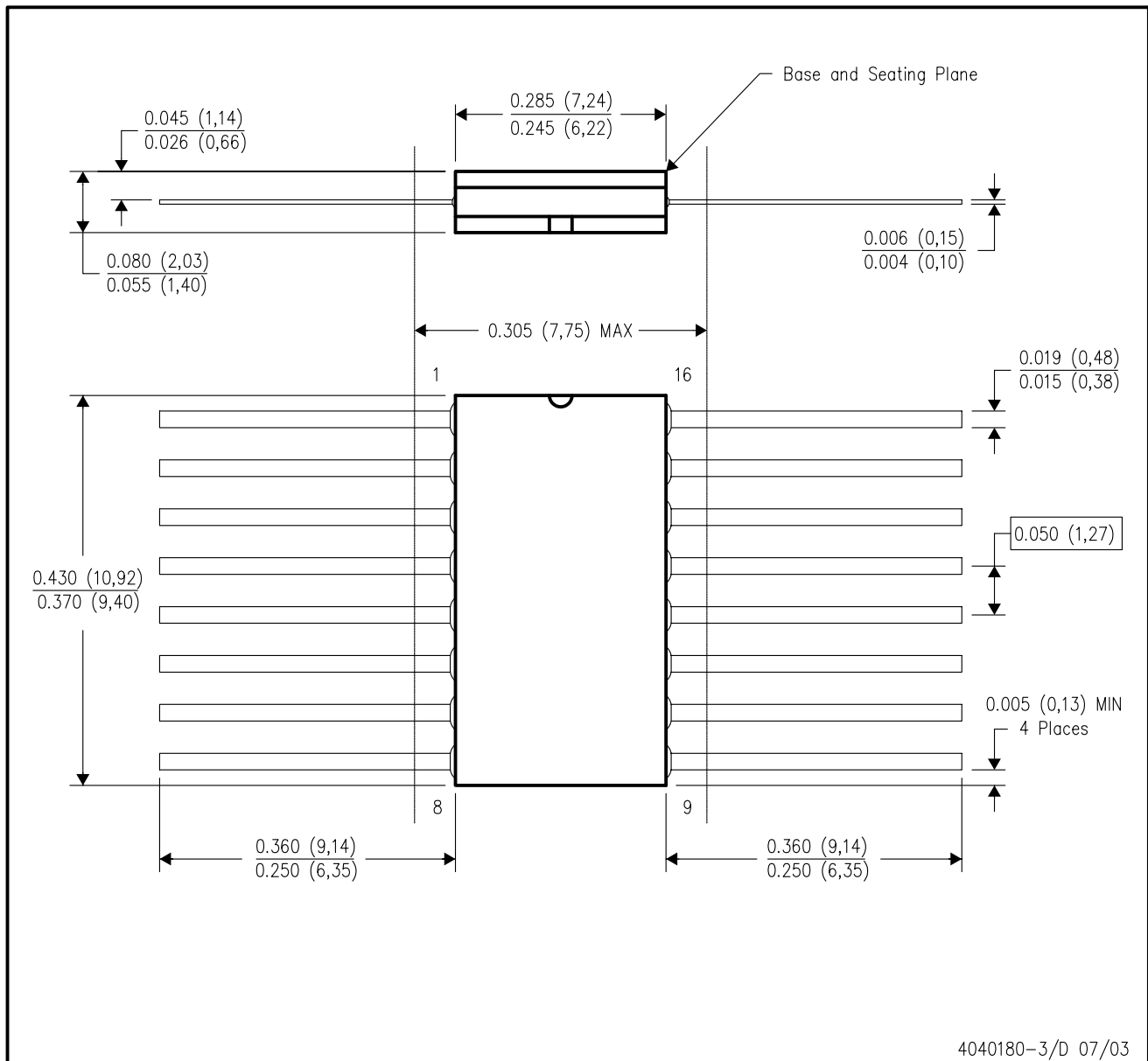


4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

W (R-GDFP-F16)

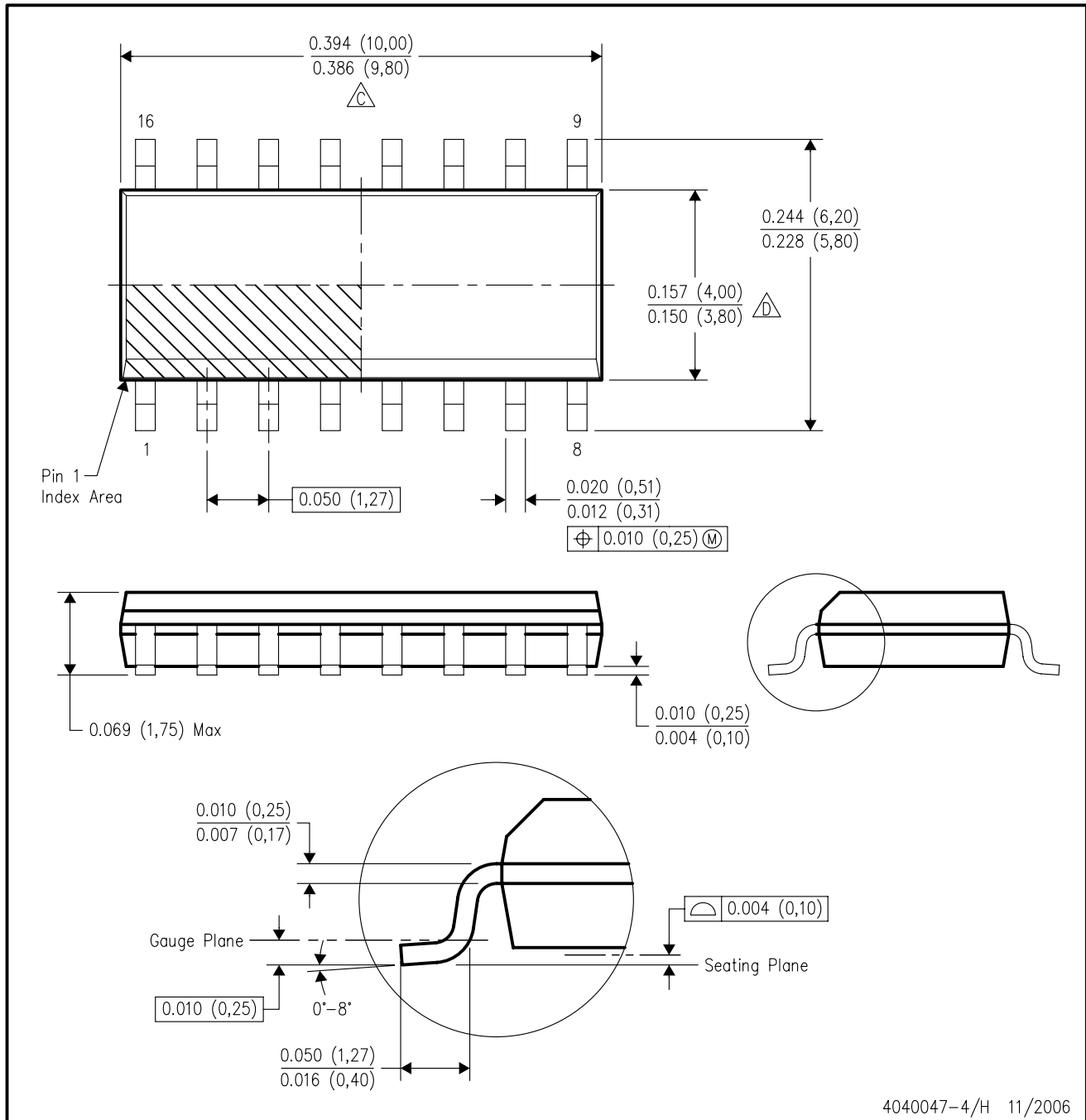
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

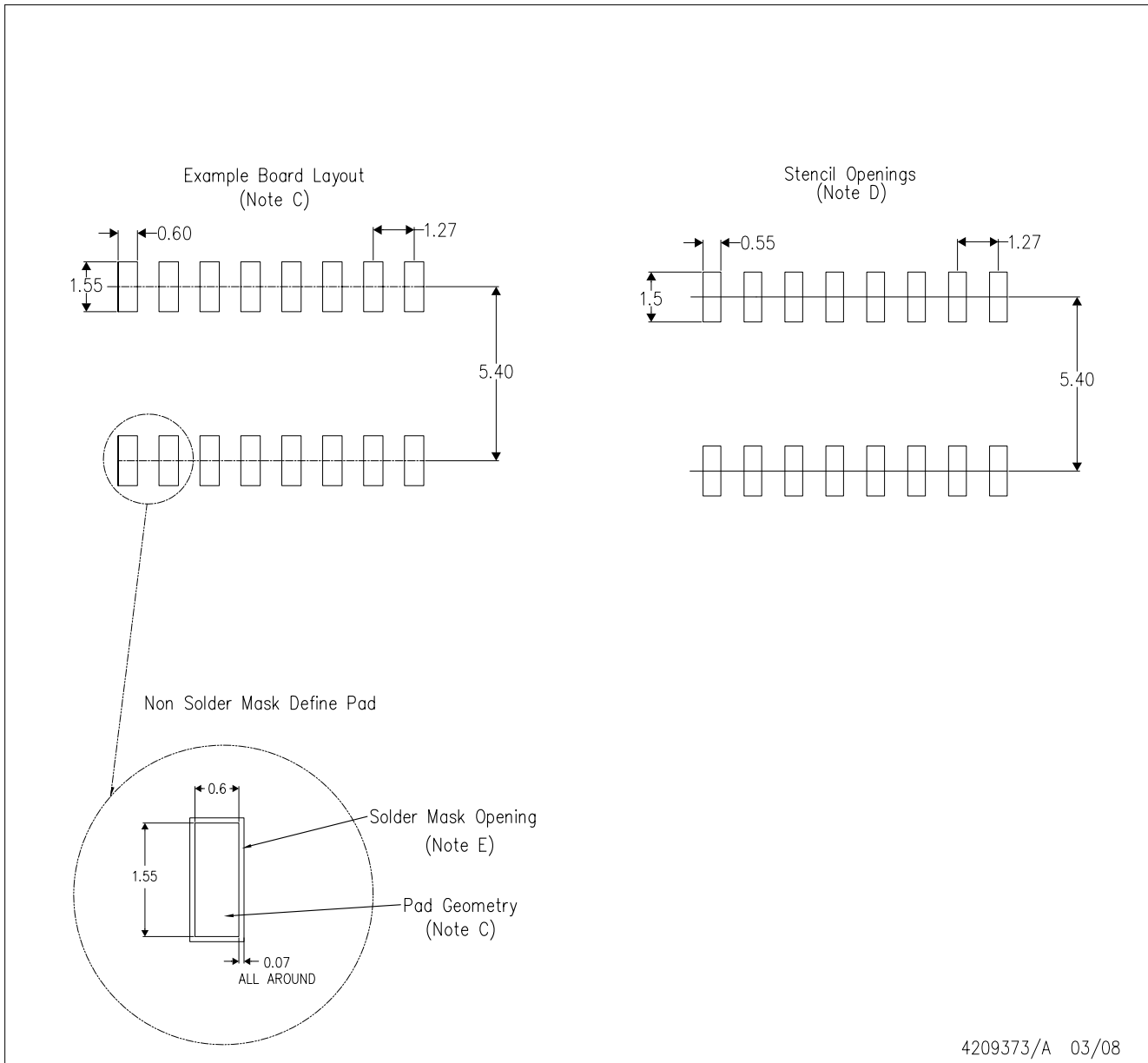
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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