

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer
- Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Supports SSTL\_18 Data Inputs
- Differential Clock (CLK and  $\overline{\text{CLK}}$ ) Inputs
- Supports LVCMOS Switching Levels on the Control and  $\overline{\text{RESET}}$  Inputs
- Supports Industrial Temperature Range (-40°C to 85°C)
- $\overline{\text{RESET}}$  Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low

### DESCRIPTION

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VCC operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL\_18, except the reset ( $\overline{\text{RESET}}$ ) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL\_18 specifications.

The SN74SSTUB32864 operates from a differential clock (CLK and  $\overline{\text{CLK}}$ ). Data are registered at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and are do-not-use (DNU) pins.

In the DDR2 RDIMM application,  $\overline{\text{RESET}}$  is specified to be completely asynchronous with respect to CLK and  $\overline{\text{CLK}}$ . Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared, and the data outputs are driven low quickly, relative to the time required to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of  $\overline{\text{RESET}}$  until the input receivers are fully enabled, the design of the SN74SSTUB32864 ensures that the outputs remain low, thus ensuring there will be no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

The device supports low-power standby operation. When  $\overline{\text{RESET}}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ( $V_{\text{REF}}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are forced low, except QERR. The LVCMOS  $\overline{\text{RESET}}$  and Cn inputs always must be held at a valid logic high or low level.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA-ZKE	Tape and reel	SN74SSTUB32864ZKER	SB864

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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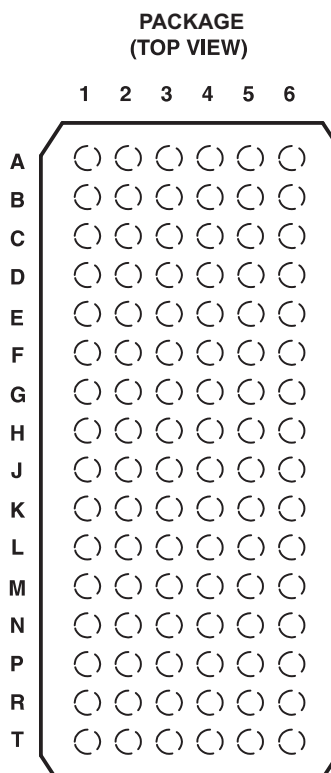


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The device also supports low-power active operation by monitoring both system chip select ( $\overline{DCS}$  and  $\overline{CSR}$ ) inputs and gates the Qn outputs from changing states when both  $\overline{DCS}$  and  $\overline{CSR}$  inputs are high. If either DCS or CSR input is low, the Qn outputs function normally. The  $\overline{RESET}$  input has priority over the  $\overline{DCS}$  and  $\overline{CSR}$  control and, when driven low, forces the Qn outputs low. If the  $\overline{DCS}$  control functionality is not desired, the  $\overline{CSR}$  input can be hard-wired to ground, in which case the setup-time requirement for DCS is the same as for the other D data inputs. To control the low-power mode with  $\overline{DCS}$  only, the  $\overline{CSR}$  input should be pulled up to  $V_{CC}$  through a pullup resistor.

The two  $V_{REF}$  pins (A3 and T3) are connected together internally by approximately 150 $\Omega$ . However, it is necessary to connect only one of the two  $V_{REF}$  pins to the external  $V_{REF}$  power supply. An unused  $V_{REF}$  pin should be terminated with a  $V_{REF}$  coupling capacitor.



**Terminal Assignments for 1:1 Register-A (C0 = 0, C1 = 0)**

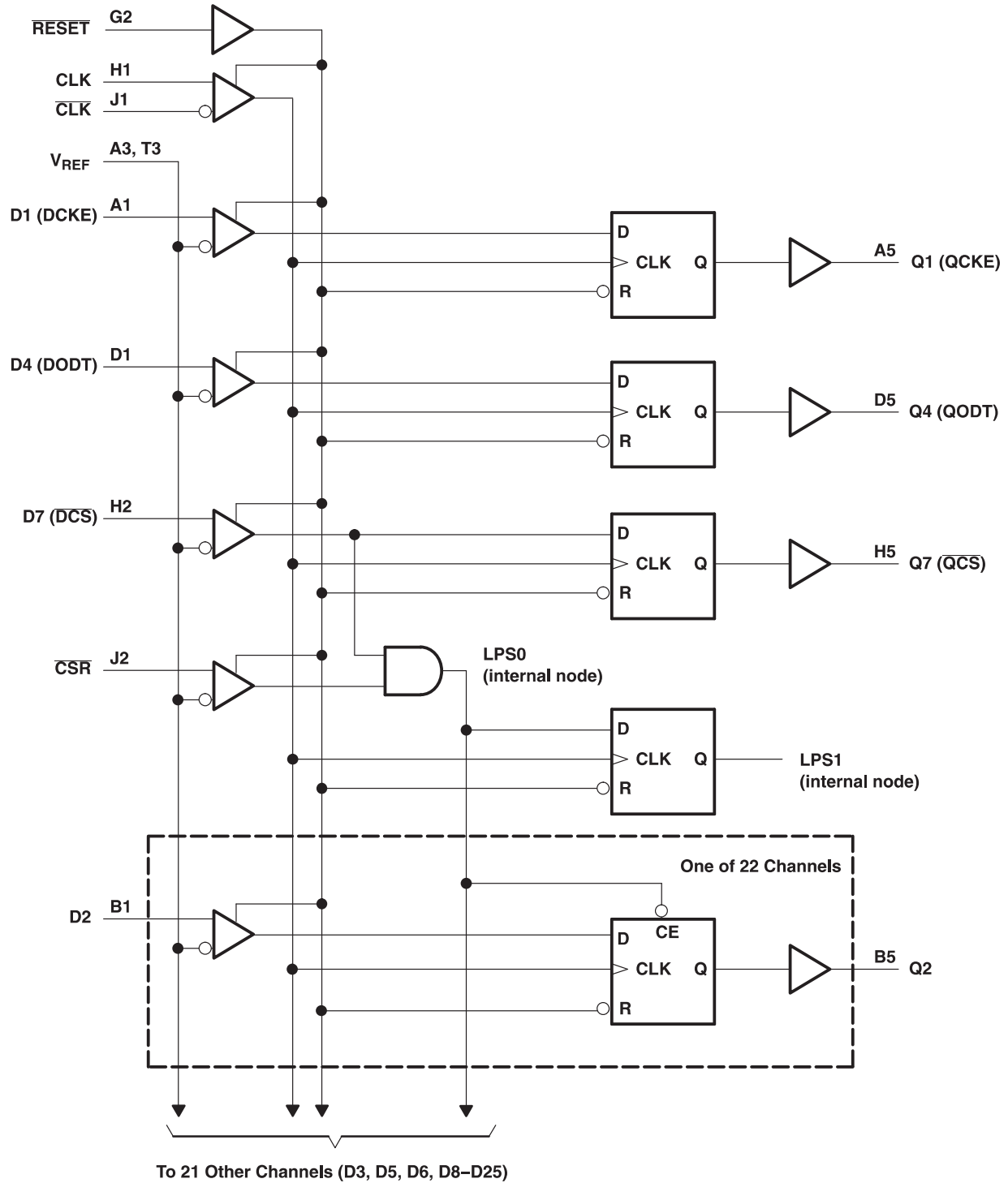
	1	2	3	4	5	6
<b>A</b>	D1 (DCKE)	NC	V <sub>REF</sub>	V <sub>CC</sub>	Q1 (QCKE)	DNU
<b>B</b>	D2	D15	GND	GND	Q2	Q15
<b>S</b>	D3	D16	V <sub>CC</sub>	V <sub>CC</sub>	Q3	Q16
<b>D</b>	D4 (DODT)	NC	GND	GND	Q4 (QODT)	DNU
<b>E</b>	D5	D17	V <sub>CC</sub>	V <sub>CC</sub>	Q5	Q17
<b>F</b>	D6	D18	GND	GND	Q6	Q18
<b>G</b>	NC	$\overline{\text{RESET}}$	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
<b>H</b>	CLK	D7 ( $\overline{\text{DCS}}$ )	GND	GND	Q7 ( $\overline{\text{QCS}}$ )	DNU
<b>J</b>	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
<b>K</b>	D8	D19	GND	GND	Q8	Q19
<b>L</b>	D9	D20	V <sub>CC</sub>	V <sub>CC</sub>	Q9	Q20
<b>M</b>	D10	D21	GND	GND	Q10	Q21
<b>N</b>	D11	D22	V <sub>CC</sub>	V <sub>CC</sub>	Q11	Q22
<b>P</b>	D12	D23	GND	GND	Q12	Q23
<b>R</b>	D13	D24	V <sub>CC</sub>	V <sub>CC</sub>	Q13	Q24
<b>T</b>	D14	D25	V <sub>REF</sub>	V <sub>CC</sub>	Q14	Q25

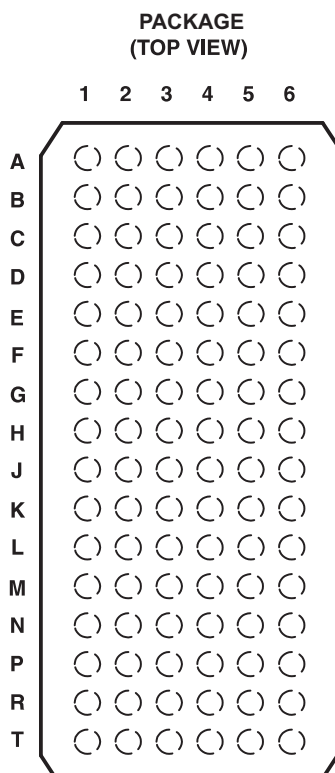
Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU - Do not use

NC - No internal connection

Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0





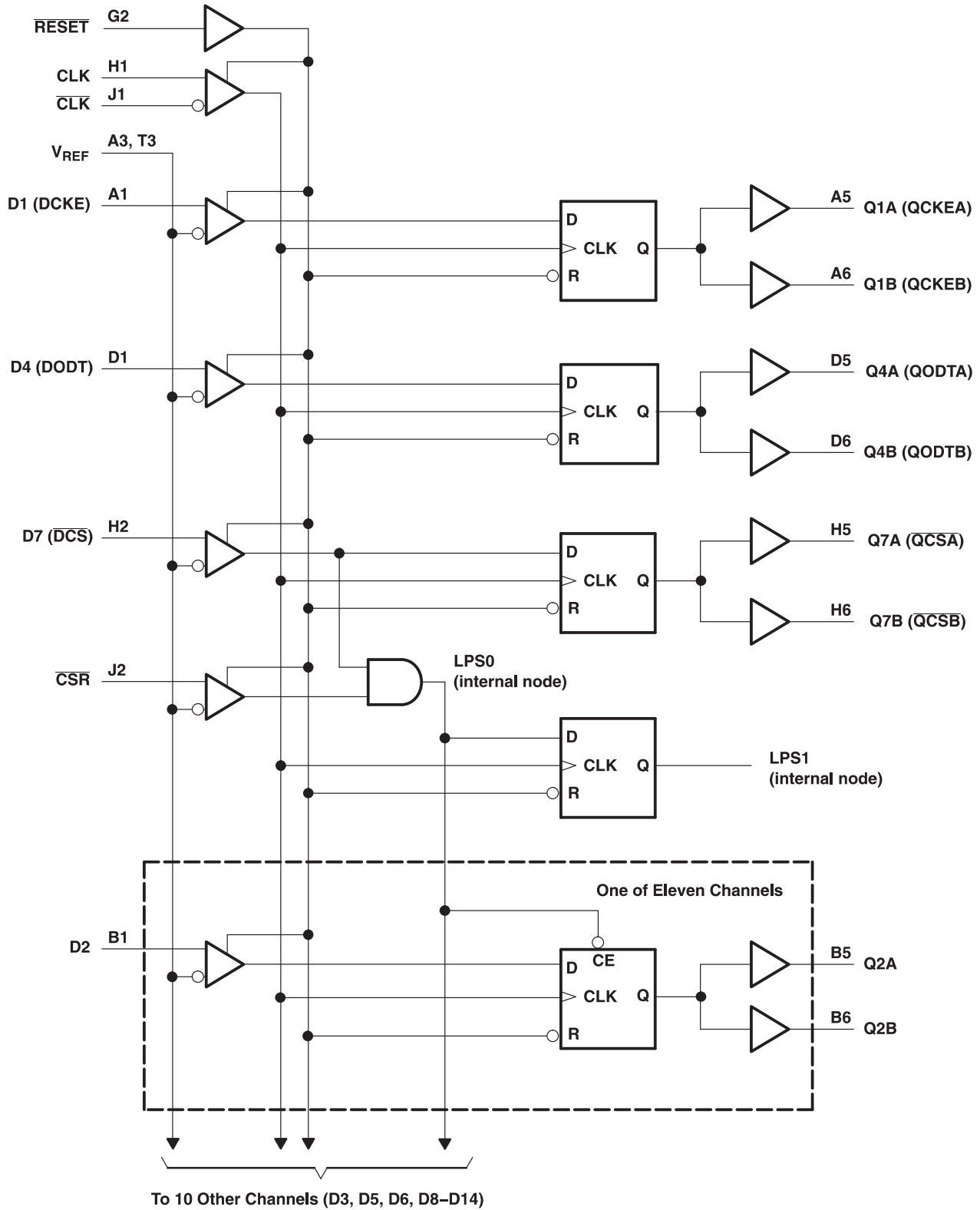
	1	2	3	4	5	6
<b>A</b>	D1 (DCKE)	NC	V <sub>REF</sub>	V <sub>CC</sub>	Q1A (QCKEA)	Q1B (QCKEB)
<b>B</b>	D2	DNU	GND	GND	Q2A	Q2B
<b>S</b>	D3	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q3A	Q3B
<b>D</b>	D4 (DODT)	NC	GND	GND	Q4A (QODTA)	Q4B(QODTB)
<b>E</b>	D5	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q5A	Q5B
<b>F</b>	D6	DNU	GND	GND	Q6A	Q6B
<b>G</b>	NC	RESET	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
<b>H</b>	CLK	D7 ( $\overline{\text{DCS}}$ )	GND	GND	Q7A ( $\overline{\text{QCSA}}$ )	Q7B ( $\overline{\text{QCSB}}$ )
<b>J</b>	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
<b>K</b>	D8	DNU	GND	GND	Q8A	Q8B
<b>L</b>	D9	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q9A	Q9B
<b>M</b>	D10	DNU	GND	GND	Q10A	Q10B
<b>N</b>	D11	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q11A	Q11B
<b>P</b>	D12	DNU	GND	GND	Q12A	Q12B
<b>R</b>	D13	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q13A	Q13B
<b>T</b>	D14	DNU	V <sub>REF</sub>	V <sub>CC</sub>	Q14A	Q14B

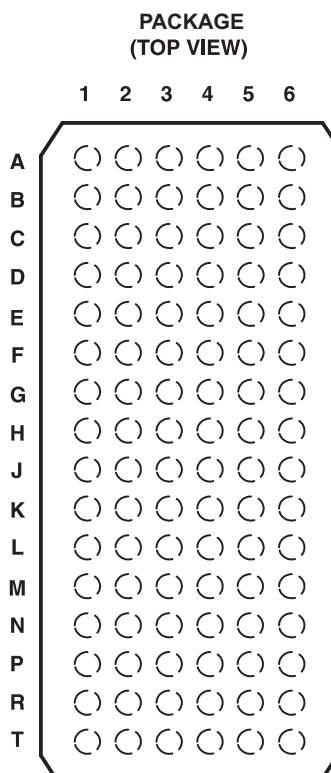
Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU - Do not use

NC - No internal connection

Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0 = 0, C1 = 1





**Terminal Assignments for 1:2 Register-b (C0 = 1, C1 = 1)**

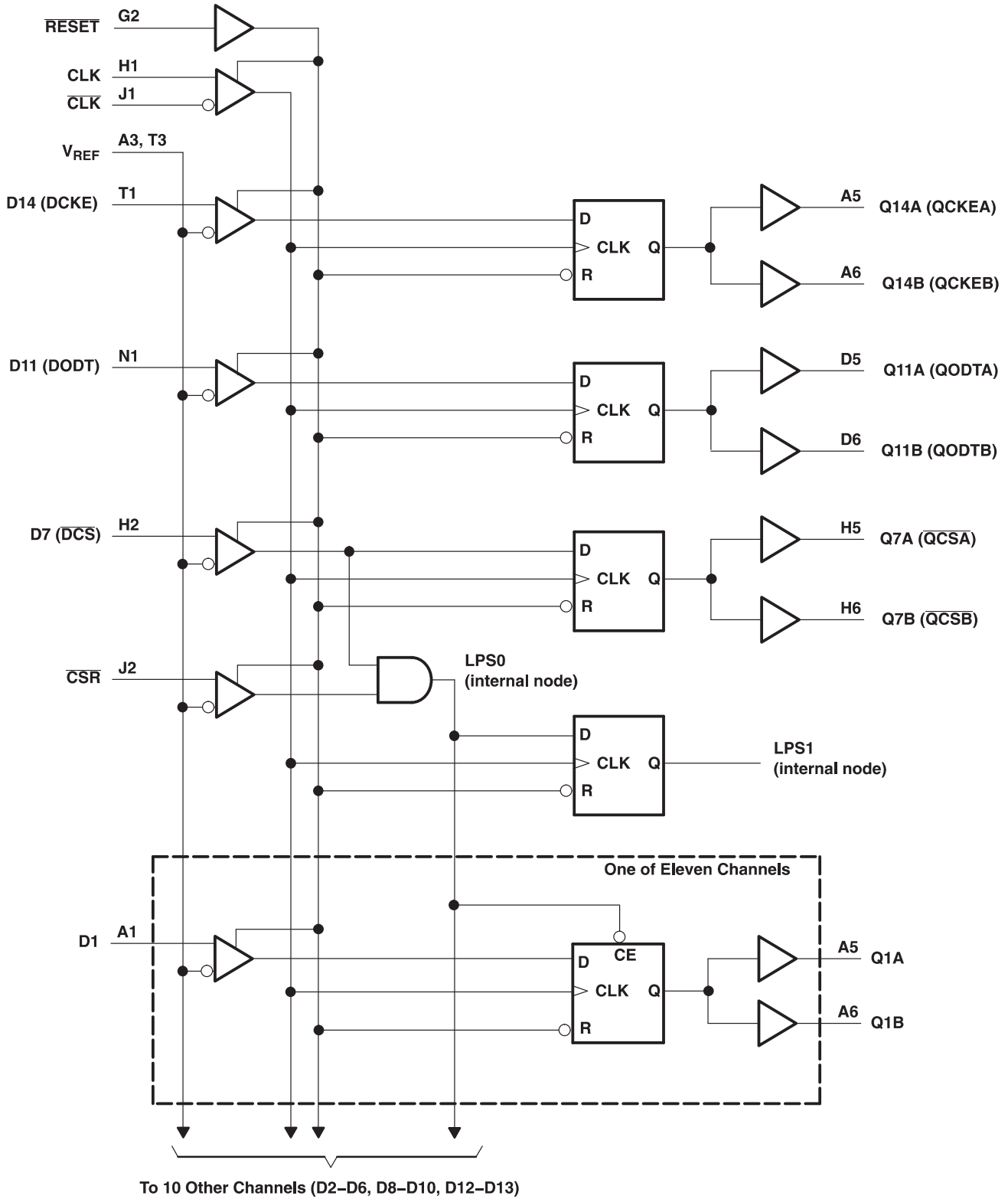
	1	2	3	4	5	6
<b>A</b>	D1	NC	V <sub>REF</sub>	V <sub>CC</sub>	Q1A	Q1B
<b>B</b>	D2	DNU	GND	GND	Q2A	Q2B
<b>S</b>	D3	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q3A	Q3B
<b>D</b>	D4	NC	GND	GND	Q4A	Q4B
<b>E</b>	D5	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q5A	Q5B
<b>F</b>	D6	DNU	GND	GND	Q6A	Q6B
<b>G</b>	NC	$\overline{\text{RESET}}$	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
<b>H</b>	CLK	D7 ( $\overline{\text{DCS}}$ )	GND	GND	Q7A ( $\overline{\text{QCSA}}$ )	Q7B ( $\overline{\text{QCSB}}$ )
<b>J</b>	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
<b>K</b>	D8	DNU	GND	GND	Q8A	Q8B
<b>L</b>	D9	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q9A	Q9B
<b>M</b>	D10	DNU	GND	GND	Q10A	Q10B
<b>N</b>	D11 (DODT)	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q11A (QODTA)	Q11B (QODTB)
<b>P</b>	D12	DNU	GND	GND	Q12A	Q12B
<b>R</b>	D13	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q13A	Q13B
<b>T</b>	D14 (DCKE)	DNU	V <sub>REF</sub>	V <sub>CC</sub>	Q14A (QCKEA)	Q14B (QCKEB)

Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU - Do not use

NC - No internal connection

Logic Diagram for 1:2 Register-B Configuration C0 = 1, C1 = 1



**TERMINAL FUNCTIONS**

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V <sub>CC</sub>	Power-supply voltage	1.8 V nominal
V <sub>REF</sub>	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{\text{CLK}}$	Negative master clock input	Differential input
C0, C1	Configuration control input. Register A or Register B and 1:1 mode or 1:2 mode select.	LVC MOS inputs
$\overline{\text{RESET}}$	Asynchronous reset input. Resets registers and disables V <sub>REF</sub> , data, and clock differential-input receivers. When $\overline{\text{RESET}}$ is low, all Q outputs are forced low and the $\overline{\text{QERR}}$ output is forced high.	LVC MOS input
D1-D25	Data input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$ .	SSTL <sub>18</sub> inputs
$\overline{\text{CSR}}$ , $\overline{\text{DCS}}$	Chip select inputs. Disables D1–D25 <sup>(1)</sup> outputs switching when both inputs are high	SSTL <sub>18</sub> inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL <sub>18</sub> input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL <sub>18</sub> input
Q1–Q25 <sup>(2)</sup>	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	1.8 V CMOS outputs
$\overline{\text{QCS}}$	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS output
QODT	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS output
QCKE	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS output
NC	No internal connection	
DNU	Do not use. Inputs are in standby-equivalent mode, and outputs are driven low.	

- (1) Data inputs = D2, D3, D5, D6, D8-D25 when C0 = 0 and C1 = 0  
 Data inputs = D2, D3, D5, D6, D8-D14 when C0 = 0 and C1 = 1  
 Data inputs = D1-D6, D8-D10, D12, D13 when C0 = 1 and C1 = 1.D
- (2) Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0 = 0 and C1 = 0  
 Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0 = 0 and C1 = 1  
 Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0 = 1 and C1 = 1.

**FUNCTION TABLE**

INPUTS						OUTPUTS
RESET	DCS	$\overline{\text{CSR}}$	CLK	$\overline{\text{CLK}}$	Dn	Qn
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q <sub>0</sub>
H	X	X	L or H	L or H	X	Q <sub>0</sub>
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L

**FUNCTION TABLE**

INPUTS				OUTPUTS
RESET	CLK	$\overline{\text{CLK}}$	DCKE, $\overline{\text{DCS}}$ , DODT	QCKE, $\overline{\text{QCS}}$ , QODT
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q <sub>0</sub>
L	X or Floating	X or Floating	X or Floating	L

**ABSOLUTE MAXIMUM RATINGS**over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE	UNIT	
V <sub>CC</sub>	Supply voltage range	–0.5 to 2.5	V	
V <sub>I</sub>	Input voltage range <sup>(2)</sup> <sup>(3)</sup>	–0.5 to V <sub>CC</sub> + 0.5	V	
V <sub>O</sub>	Output voltage range <sup>(2)</sup> <sup>(3)</sup>	–0.5 to V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current, (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	±50	mA	
I <sub>OK</sub>	Output clamp current, (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±50	mA	
I <sub>O</sub>	Continuous output current (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±50	mA	
I <sub>CC</sub>	Continuous current through each V <sub>CC</sub> or GND	±100	mA	
R <sub>θJA</sub>	Thermal impedance, junction-to-ambient <sup>(4)</sup>	No airflow	39.8	K/W
		Airflow 150 ft/min	34.1	
		Airflow 250 ft/min	33.6	
		Airflow 500 ft/min	32.5	
R <sub>θJB</sub>	Thermal resistance, junction-to-board <sup>(4)</sup>	No airflow	14.5	
T <sub>stg</sub>	Storage temperature range	–65 to 150	°C	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This value is limited to 2.5 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	NOM	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	1.7		1.9	V	
V <sub>REF</sub>	Reference voltage	0.49 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.51 × V <sub>CC</sub>	V	
V <sub>TT</sub>	Termination voltage	V <sub>REF</sub> –40 mV	V <sub>REF</sub>	V <sub>REF</sub> + 40 mV	V	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V	
V <sub>IH</sub>	AC high-level input voltage	Data inputs, $\overline{\text{CSR}}$		V <sub>REF</sub> + 250 mV	V	
V <sub>IL</sub>	AC low-level input voltage	Data inputs, $\overline{\text{CSR}}$		V <sub>REF</sub> –250 mV	V	
V <sub>IH</sub>	DC high-level input voltage	Data inputs, $\overline{\text{CSR}}$		V <sub>REF</sub> + 125 mV	V	
V <sub>IL</sub>	DC low-level input voltage	Data inputs, $\overline{\text{CSR}}$		V <sub>REF</sub> –125 mV	V	
V <sub>IH</sub>	High-level input voltage	$\overline{\text{RESET}}$ , C <sub>n</sub>		0.65 × V <sub>CC</sub>	V	
V <sub>IL</sub>	Low-level input voltage	$\overline{\text{RESET}}$ , C <sub>n</sub>		0.35 × V <sub>CC</sub>	V	
V <sub>ICR</sub>	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$		0.675	1.125	V
V <sub>I(PP)</sub>	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$		600		mV
I <sub>OH</sub>	High-level output current	Q outputs		–8		mA
I <sub>OL</sub>	Low-level output current	Q outputs		8		mA
T <sub>A</sub>	Operating free-air temperature			–40	85	°C

(1) The  $\overline{\text{RESET}}$  and C<sub>n</sub> inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless  $\overline{\text{RESET}}$  is low. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	Q outputs	I <sub>OH</sub> = -100 μA	1.7V to 1.9V	V <sub>CC</sub> -0.2			V
		I <sub>OH</sub> = -6 mA	1.7V	1.3			
V <sub>OL</sub>	Q outputs	I <sub>OL</sub> = 100 μA	1.7V to 1.9V	0.2			V
		I <sub>OL</sub> = 6 mA	1.7V	0.4			
I <sub>I</sub>	All inputs <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND	1.9V	±5			μA
I <sub>CC</sub>	Static standby	RESET = GND	1.9V	200			μA
	Static operating	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub>		I <sub>O</sub> = 0 40			
I <sub>CCD</sub>	Dynamic operating – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ; CLK and CLK switching 50% duty cycle	I <sub>O</sub> = 0 1.8V	45			μA/MHz  μA clock MHz/ D input
	Dynamic operating – per each data input, 1:1 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ; CLK and CLK switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle		43			
	Dynamic operating – per each data input, 1:2 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ; CLK and CLK switching 50% duty cycle		60			
I <sub>CCDLP</sub>	Chip-select-enabled low-power active mode – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ; CLK and CLK switching 50% duty cycle	I <sub>O</sub> = 0 1.8V	45			μA/MHz  μA clock MHz/ D input
	Chip-select-enabled low-power active mode - 1:1 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ; CLK and CLK switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle		2			
	Chip-select-enabled low-power active mode – 1:2 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> ; CLK and CLK switching 50% duty cycle		3			
C <sub>i</sub>	Data inputs, CSR	V <sub>I</sub> = V <sub>REF</sub> ± 250 mV	1.8V	2.5	3	3.5	pF
	CLK, CLK	V <sub>ICR</sub> = 0.9 V, V <sub>I(PP)</sub> = 600 mV		2		3	
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND		4			

 (1) All typical values are at V<sub>CC</sub> = 1.8 V, T<sub>A</sub> = 25°C.

 (2) Each V<sub>REF</sub> pin (A3 or T3) should be tested independently, with the other (untested) pin open.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#) and <sup>(1)</sup>)

		$V_{CC} = 1.8\text{ V} \pm 0.1\text{ V}$		UNIT	
		MIN	MAX		
f <sub>clock</sub>	Clock frequency	410		MHz	
t <sub>w</sub>	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low	1		ns	
t <sub>act</sub>	Differential inputs active time <sup>(2)</sup>	10		ns	
t <sub>inact</sub>	Differential inputs inactive time <sup>(3)</sup>	15		ns	
t <sub>su</sub>	Setup time	$\overline{\text{DCS}}$ before CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$ , $\overline{\text{CSR}}$ high; $\overline{\text{CSR}}$ before CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$ , $\overline{\text{DCS}}$ high		600	ps
		$\overline{\text{DCS}}$ before CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$ , $\overline{\text{CSR}}$ low		500	
		DODT, DCKE, and Data before CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$		500	
t <sub>h</sub>	Hold time	$\overline{\text{DCS}}$ , DODT, DCKE, and Data after CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$		400	ps

(1) All inputs slew rate is 1 V/ns  $\pm$  20%.

(2) V<sub>REF</sub> must be held at a valid input level, and data inputs must be held low for a minimum time of t<sub>act</sub> max, after  $\overline{\text{RESET}}$  is taken high.

(3) V<sub>REF</sub>, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t<sub>inact</sub> max, after  $\overline{\text{RESET}}$  is taken low.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.1\text{ V}$		UNIT
				MIN	MAX	
f <sub>max</sub>	See <a href="#">Figure 2</a>			410		MHz
t <sub>pdm</sub>	Production test, See <a href="#">Figure 1</a>	CLK and $\overline{\text{CLK}}$	Q	0.4	0.8	ns
t <sub>RPHL</sub> <sup>(1)</sup>	See <a href="#">Figure 2</a>	$\overline{\text{RESET}}$	Q	3		ns

(1) Includes 350-ps test-load transmission-line delay.

## OUTPUT SLEW RATES

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM	TO	$V_{CC} = 1.8\text{ V} \pm 0.1\text{ V}$		UNIT
			MIN	MAX	
dV/dt <sub>r</sub>	20%	80%	1	4	V/ns
dV/dt <sub>f</sub>	80%	20%	1	4	V/ns
dV/dt $\Delta$ <sup>(1)</sup>	20% or 80%	80% or 20%	1		V/ns

(1) Difference between dV/dt<sub>r</sub> (rising edge rate) and dV/dt<sub>f</sub> (falling edge rate).

PARAMETER MEASUREMENT INFORMATION

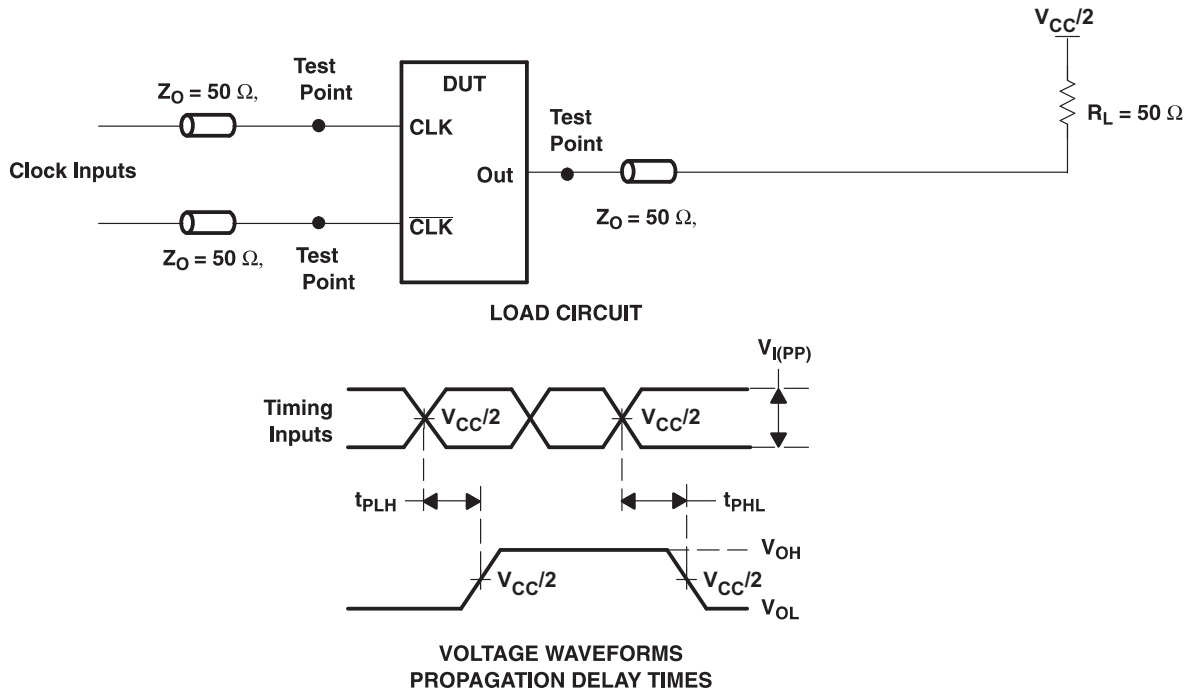
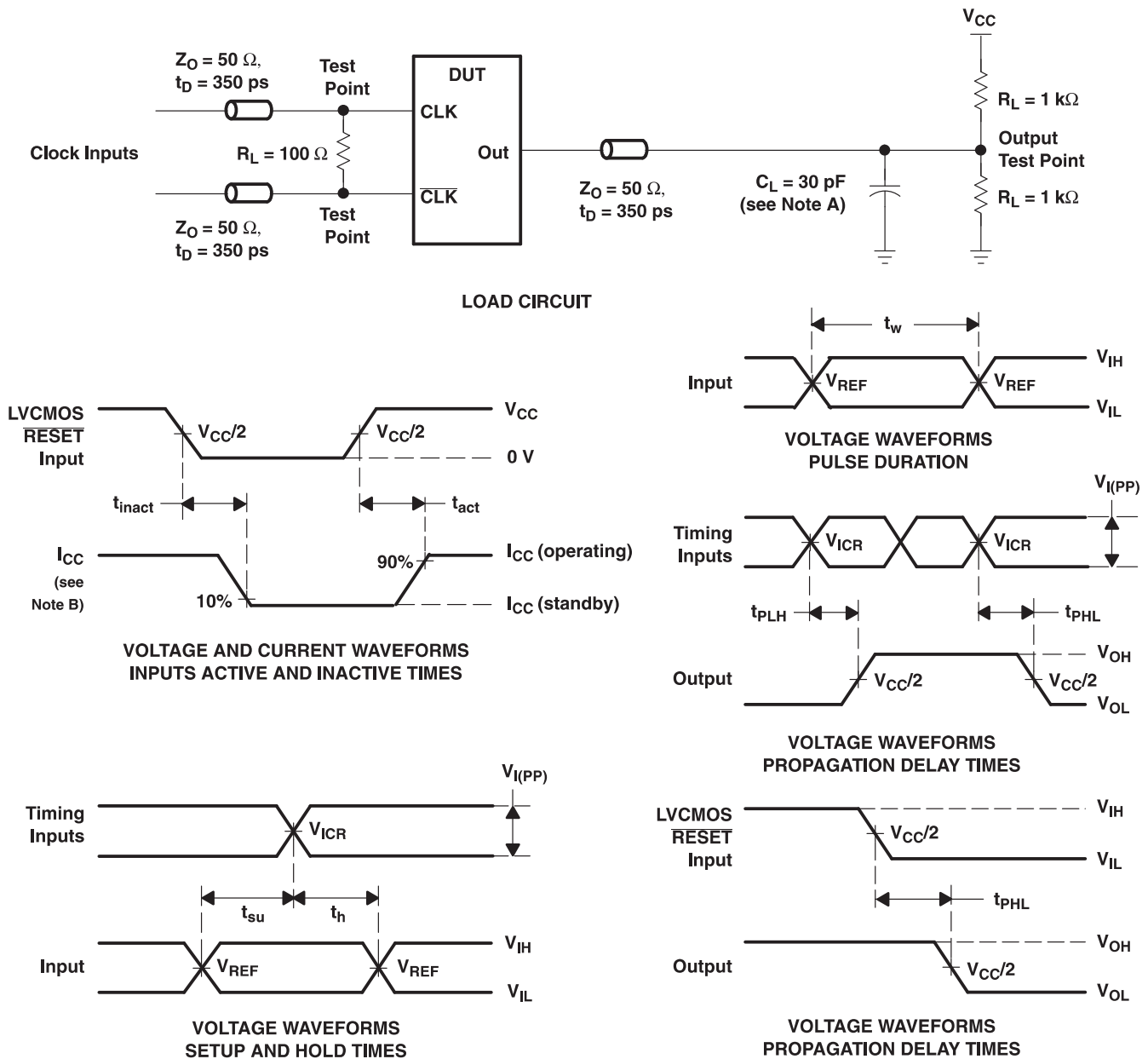


Figure 1. Output Load For Production Test

PROPAGATION DELAY (Design Goal as per JEDEC Specification)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 V \pm 0.1 V$		UNIT
			MIN	MAX	
$t_{pdm}^{(1)}$	CLK and $\overline{CLK}$	Q	1.1	1.5	ns
$t_{pdmss}^{(2)}$	CLK and $\overline{CLK}$	Q		1.6	ns

- (1) Includes 350 psi test-load transmission delay line
- (2) Includes 350 psi test-load transmission delay line



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B.  $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0 \text{ mA}$ .
  - C. All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise noted).
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $V_{REF} = V_{TT} = V_{CC}/2$
  - F.  $V_{IH} = V_{REF} + 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVC MOS input.
  - G.  $V_{IL} = V_{REF} - 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.
  - H.  $V_{I(PP)} = 600 \text{ mV}$
  - I.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Data Output Load Circuit and Voltage Waveforms

## APPLICATION INFORMATION

The typical values below are for standard raw cards. Test equipment used was the JEDEC register validation board using pattern 0x43, 0x4F, and 0x5A.

**Table 1. Raw Card Values** <sup>(1)</sup> <sup>(2)</sup>

RAW CARD	$t_{pdms}$		OVERSHOOT
	MIN	MAX	
A/F	1.2 ns	1.6 ns	140 mV
B/G	1.3 ns	2.0 ns	430 mV
C/H	1.3 ns	2.0 ns	430 mV

- (1) All values are valid under nominal conditions and minimum/maximum of typical signals on one typical DIMM.  
(2) Measurements include all jitter and ISI effects.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74SSTUB32864ZKER	ACTIVE	LFPGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

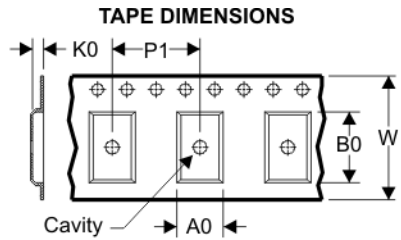
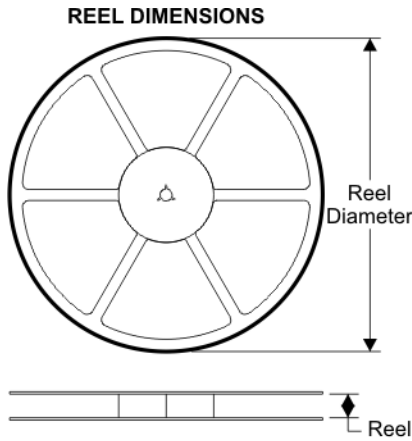
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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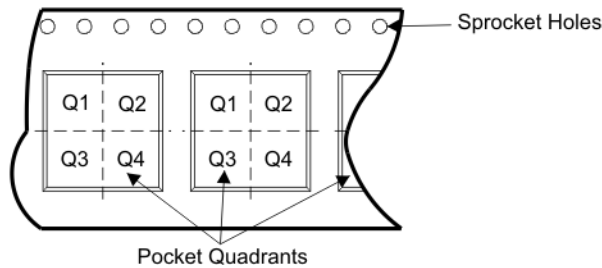
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**TAPE AND REEL BOX INFORMATION**



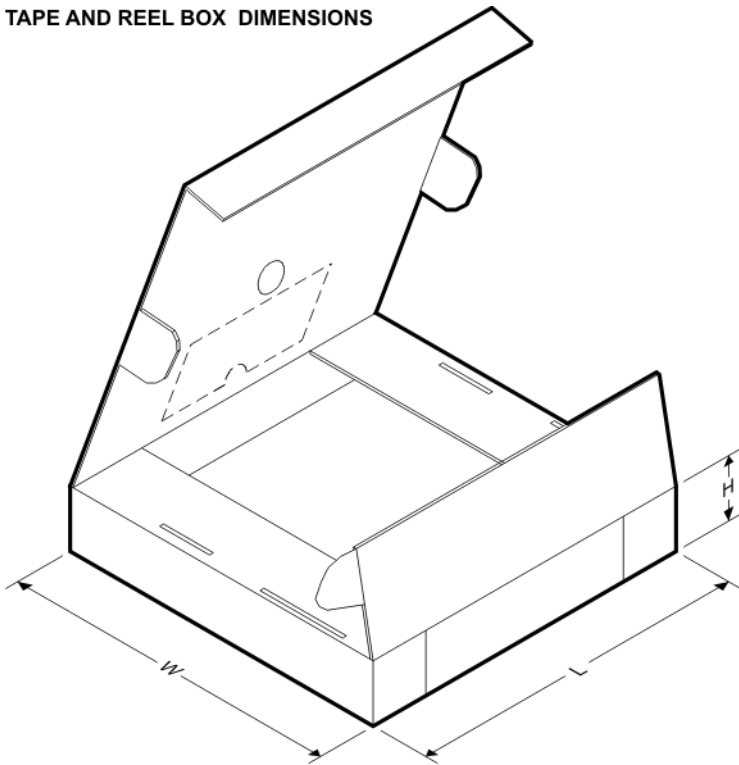
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTUB32864ZKER	ZKE	96	SITE 60	330	24	5.7	13.7	2.0	8	24	Q1

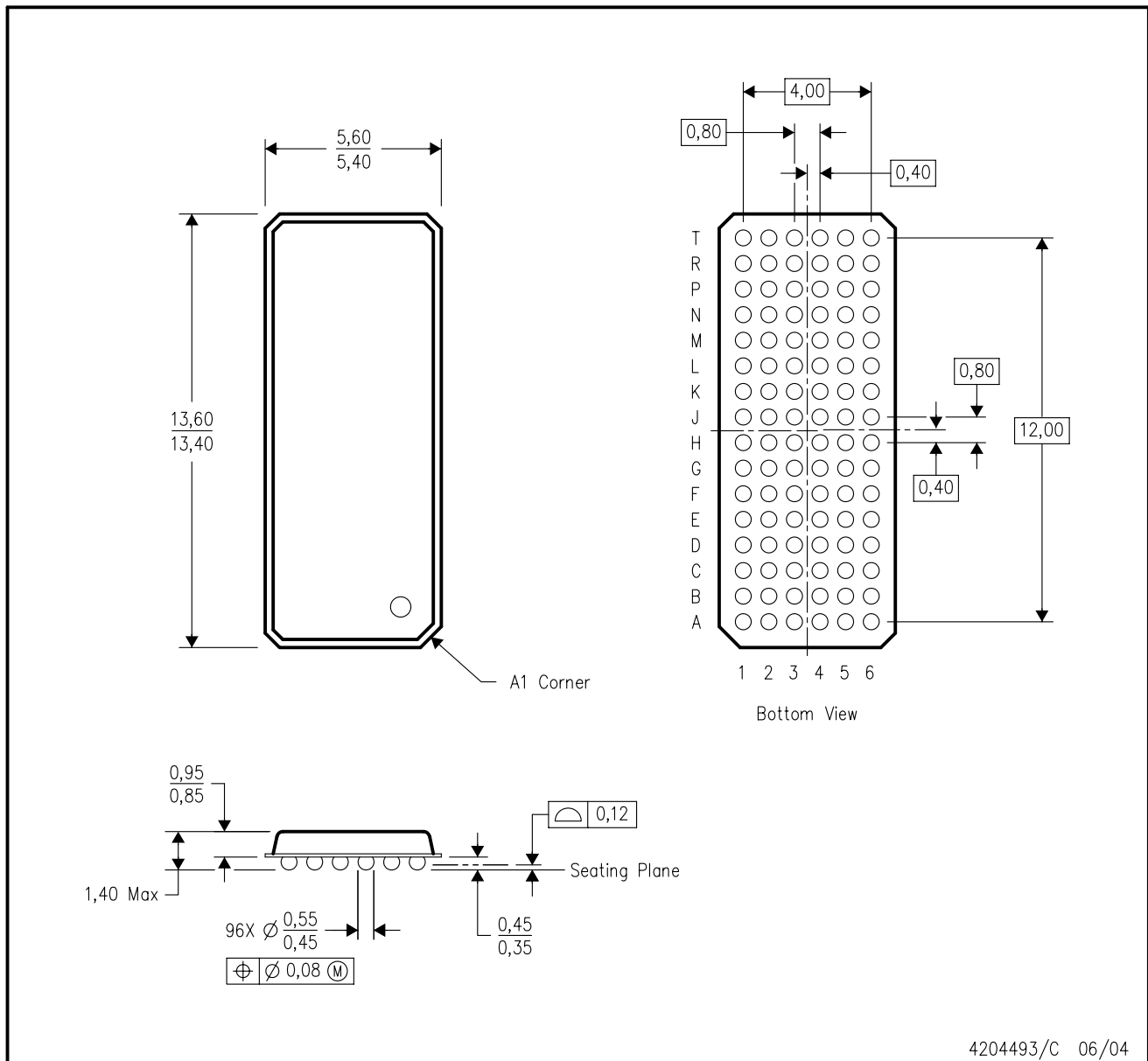
**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74SSTUB32864ZKER	ZKE	96	SITE 60	342.9	336.0	31.7

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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