

# SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS144B – APRIL 1985 – REVISED FEBRUARY 2002

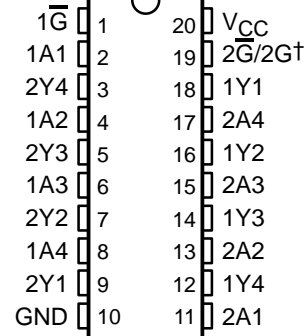
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control ( $\overline{G}$ ) inputs, and complementary output-control ( $G$  and  $\overline{G}$ ) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133  $\Omega$ .

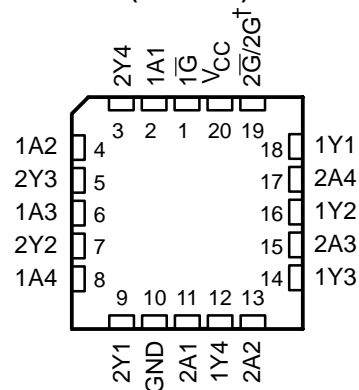
SN54LS', SN54S' . . . J OR W PACKAGE  
SN74LS240, SN74LS244 . . . DB, DW, N, OR NS PACKAGE  
SN74LS241 . . . DW, N, OR NS PACKAGE  
SN74S' . . . DW OR N PACKAGE

(TOP VIEW)



† 2G for 'LS241 and 'S241 or  $\overline{2G}$  for all other drivers.

SN54LS', SN54S' . . . FK PACKAGE  
(TOP VIEW)



† 2G for 'LS241 and 'S241 or  $\overline{2G}$  for all other drivers.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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**ORDERING INFORMATION**

<b>T<sub>A</sub></b>	<b>PACKAGE†</b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
0°C to 70°C	PDIP – N	Tube	SN74LS240N	SN74LS240N
			SN74LS241N	SN74LS241N
			SN74LS244N	SN74LS244N
			SN74S240N	SN74S240N
			SN74S241N	SN74S241N
			SN74S244N	SN74S244N
	SOIC – DW	Tube	SN74LS240DW	LS240
		Tape and reel	SN74LS240DWR	
		Tube	SN74LS241DW	LS241
		Tape and reel	SN74LS241DWR	
		Tube	SN74LS244DW	LS244
		Tape and reel	SN74LS244DWR	
		Tube	SN74S240DW	S240
		Tape and reel	SN74S240DWR	
		Tube	SN74S241DW	S241
		Tape and reel	SN74S241DWR	
		Tube	SN74S244DW	S244
		Tape and reel	SN74S244DWR	
	SOP – NS	Tube	SN74LS240NSR	74LS240
			SN74LS241NSR	74LS241
			SN74LS244NSR	74LS244
	SSOP – DB	Tape and reel	SN74LS240DBR	LS240
			SN74LS244DBR	LS244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244  
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**ORDERING INFORMATION (CONTINUED)**

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – J	Tube	SN54LS240J	SN54LS240J
			SNJ54LS240J	SNJ54LS240J
			SN54LS241J	SN54LS241J
			SNJ54LS241J	SNJ54LS241J
			SN54LS244J	SN54LS244J
			SNJ54LS244J	SNJ54LS244J
			SN54S240J	SN54S240J
			SNJ54S240J	SNJ54S240J
			SN54S241J	SN54S241J
			SNJ54S241J	SNJ54S241J
			SN54S244J	SN54S244J
			SNJ54S244J	SNJ54S244J
	CFP – W	Tube	SNJ54LS240W	SNJ54LS240W
	SNJ54LS241W	SNJ54LS241W		
	SNJ54LS244W	SNJ54LS244W		
	SNJ54S240W	SNJ54S240W		
	SNJ54S241W	SNJ54S241W		
	SNJ54S244W	SNJ54S244W		
	LCCC – FK	Tube	SNJ54LS240FK	SNJ54LS240FK
	SNJ54LS241FK	SNJ54LS241FK		
	SNJ54LS244FK	SNJ54LS244FK		
	SNJ54S240FK	SNJ54S240FK		
	SNJ54S241FK	SNJ54S241FK		
	SNJ54S244FK	SNJ54S244FK		

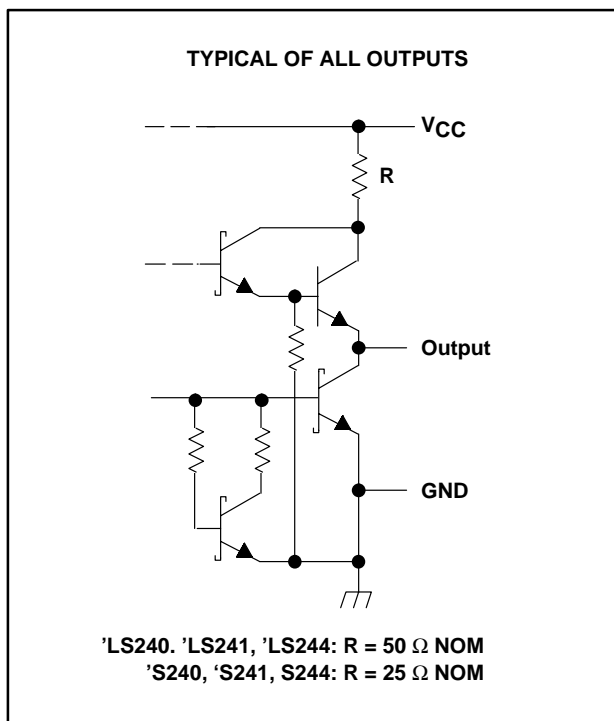
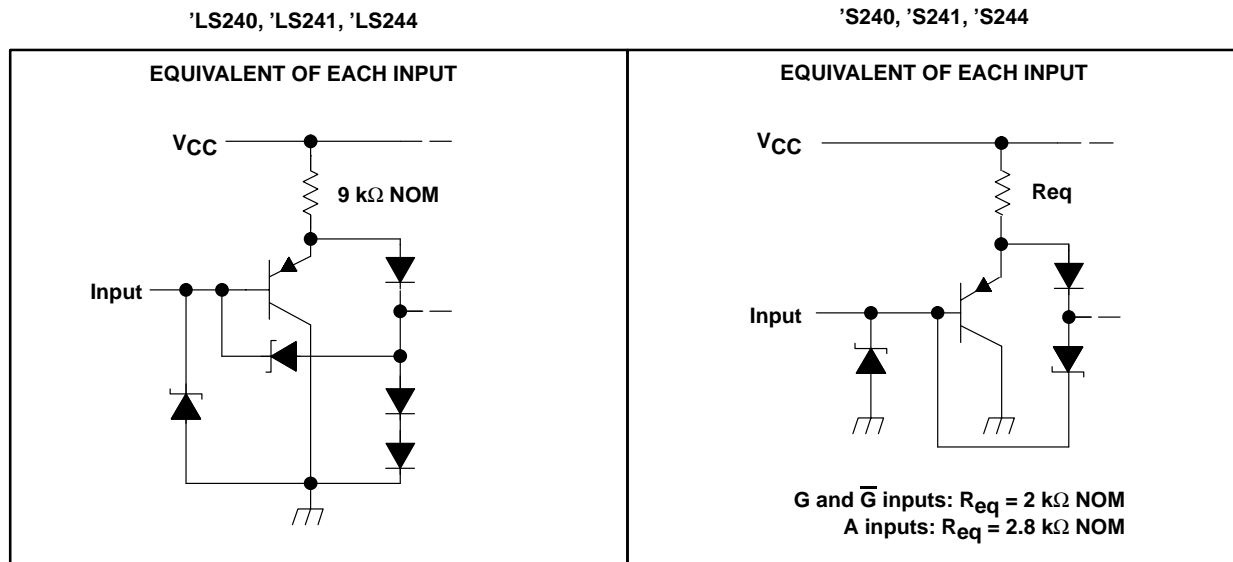
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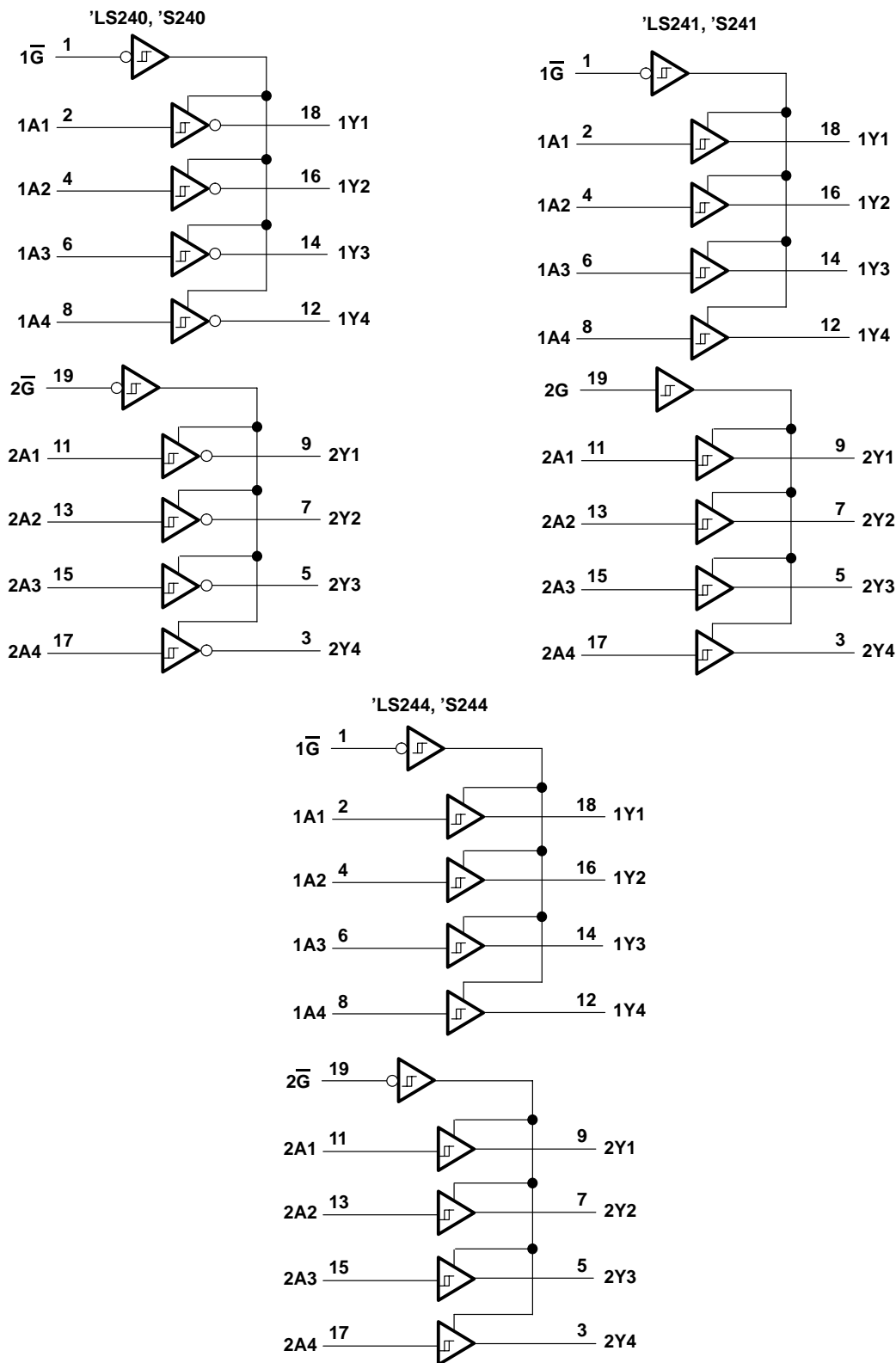
**schematics of inputs and outputs**



SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244  
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logic diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages.



