

SN54S124, SN74S124 DUAL VOLTAGE-CONTROLLED OSCILLATORS

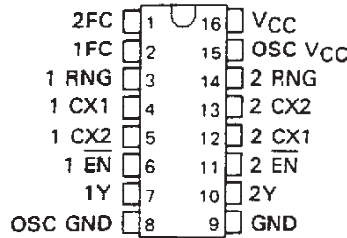
SDLS201A – DECEMBER 1983 – REVISED APRIL 2004

- Two independent VCOs in a 16-Pin Package
- Output Frequency Set by Single External Component:
Capacitor for Fixed- or Variable-Frequency Operation
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges
- Typical f_{max} 85 MHz
Typical Power Dissipation 525 mW
- Frequency Spectrum . . . 1 Hz to 60 MHz

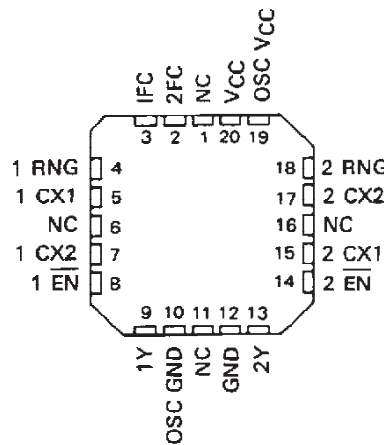
description

The 'S124 features two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by an external capacitor in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. 1

SN54S124 . . . J OR W PACKAGE
SN74S124 . . . D OR N PACKAGE
(TOP VIEW)



SN54S124 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

While the enable input is low, the output is enabled.
While the enable input is high, the output is high.

These devices can operate from a single 5-volt supply. However, one set of supply-voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set ($\ominus V_{CC}$ and $\ominus GND$) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system.

The enable input of these devices starts or stops the output pulses when it is low or high, respectively. The internal oscillator of the 'S124 is started and stopped by the enable input. The enable input is one standard load; it and the buffered output operate at standard Schottky-clamped TTL levels.

The pulse synchronization-gating section ensures that the first output pulse is neither clipped nor extended. Duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54S124 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74S124 is characterized for operation from 0°C to 70°C .



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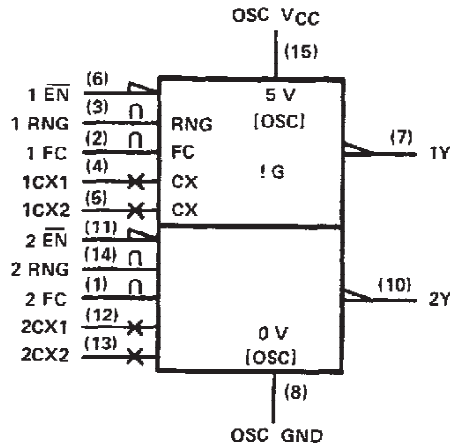
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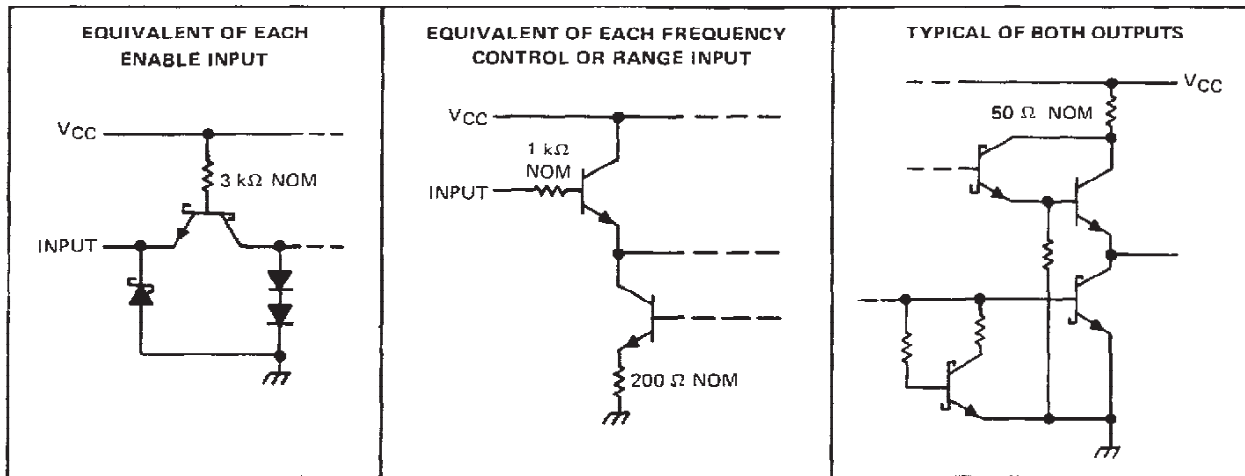
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Notes 1 and 2)	7V
Input voltage	5.5 V
Operating free-air temperature range: SN54S124	-55°C to 125°C
SN74S124	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to the appropriate ground terminal.

2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and $\odot V_{CC}$ terminals, unless otherwise noted.

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recommended operating conditions

	SN54S124			SN74S124			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	6.25	V
Input voltage at frequency control or range input, $V_I(\text{freq})$ or $V_I(\text{rng})$	1		5	1		5	V
High-level output current, I_{OH}			-1			-1	mA
Low-level output current, I_{OL}			20			20	mA
Output frequency (enabled), f_o	1			1			Hz
			60			60	MHz
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT	
V_{IH}	High-level input voltage at enable		2			V	
V_{IL}	Low-level input voltage at enable				0.8	V	
V_{IK}	Input clamp voltage at enable	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S'	2.5	3.4	V	
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V	
I_I	Input current	Freq control or range	$V_{CC} = \text{MAX}$	$V_I = 5 \text{ V}$	10	50	μA
				$V_I = 1 \text{ V}$	1	15	
I_I	Input current at maximum input voltage	Enable	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1	mA	
I_{IH}	High-level input current	Enable	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		50	μA	
I_{IL}	Low-level input current	Enable	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$		-2	mA	
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	-40		-100	mA	
I_{CC}	Supply current, total into V_{CC} and $\ominus V_{CC}$	$V_{CC} = \text{MAX}, \text{ See Note 3}$		105	150	mA	
		$V_{CC} = \text{MAX}, T_A = 125^{\circ}\text{C}, \text{ W package only}$ See Note 3			110		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the outputs disabled and open.

switching characteristics, $V_{CC} = 5 \text{ V}, R_L = 280 \Omega, C_L = 15 \text{ pF}, T_A = 25^{\circ}\text{C}$ (see note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_o	Output frequency	$C_{\text{ext}} = 2 \text{ pF}$	$V_I(\text{freq}) = 4 \text{ V}, V_I(\text{rng}) = 1 \text{ V}$	60	85	MHz
			$V_I(\text{freq}) = 1 \text{ V}, V_I(\text{rng}) = 5 \text{ V}$	25	40	
	Output duty cycle	$C_{\text{ext}} = 8.3 \text{ pF}$ to $500 \mu\text{F}$		50%		
t_{PHL}	Propagation delay time, high-to-low-level output from enable	$f_o = 1 \text{ Hz}$ to 20 MHz		$\frac{1.4}{f_o(\text{Hz})}$		s
		$f_o > 20 \text{ MHz}$		70		ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



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TYPICAL CHARACTERISTICS

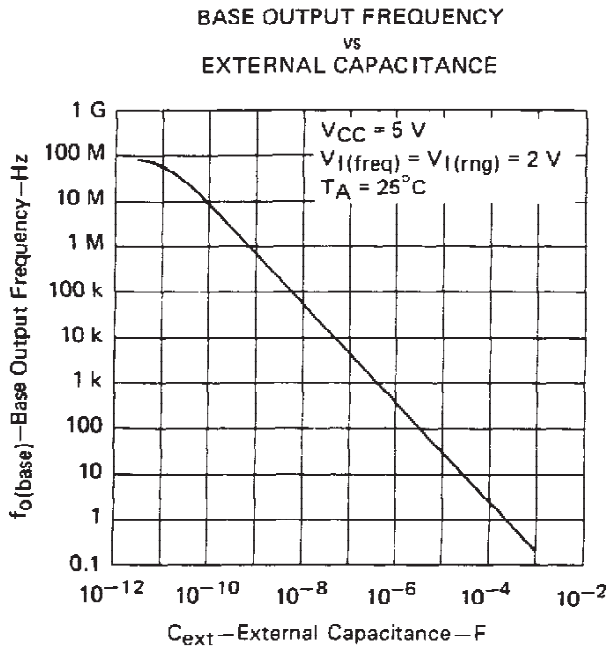


FIGURE 1

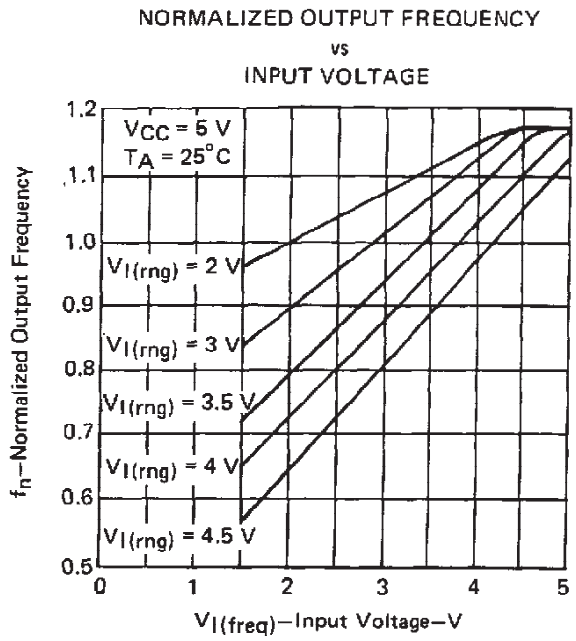


FIGURE 2

NOTE: $f_o = f_n \times f_{o(\text{base})}$

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54S124J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SN74S124D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S124DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S124DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S124DRE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
SN74S124DRG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
SN74S124N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S124N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74S124NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54S124J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SNJ54S124W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

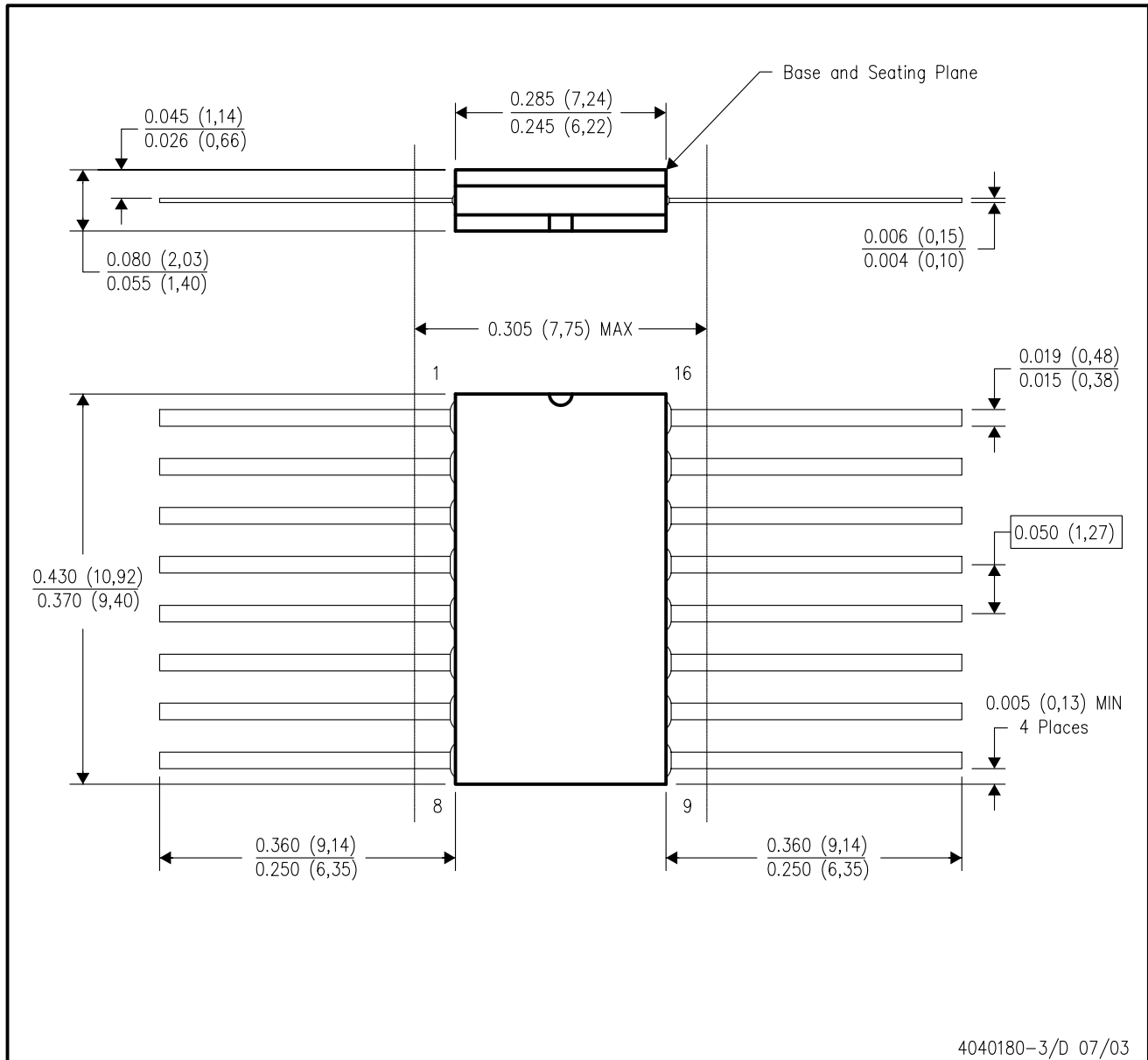


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

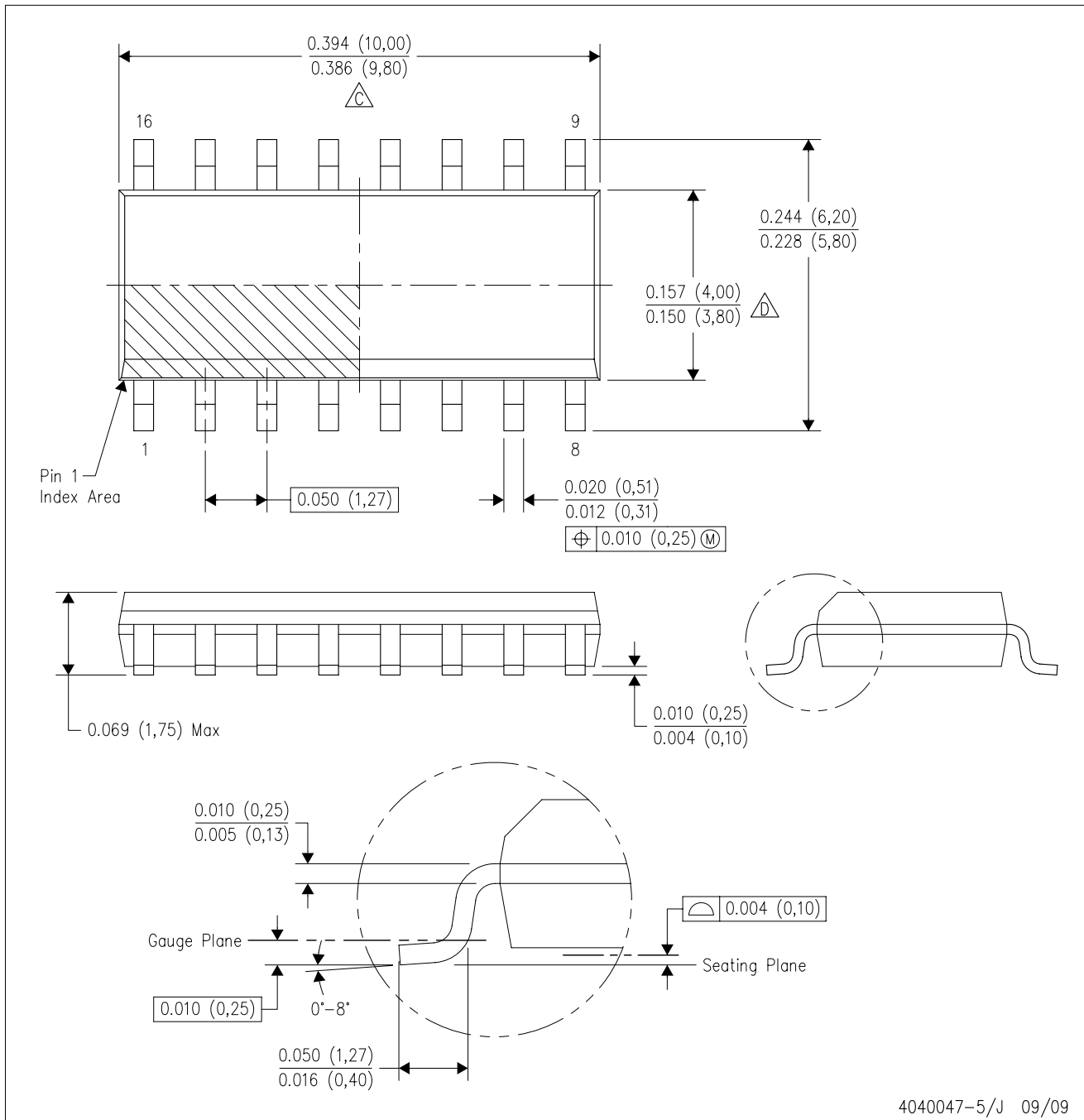
CERAMIC DUAL FLATPACK





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

D (R-PDSO-G16)

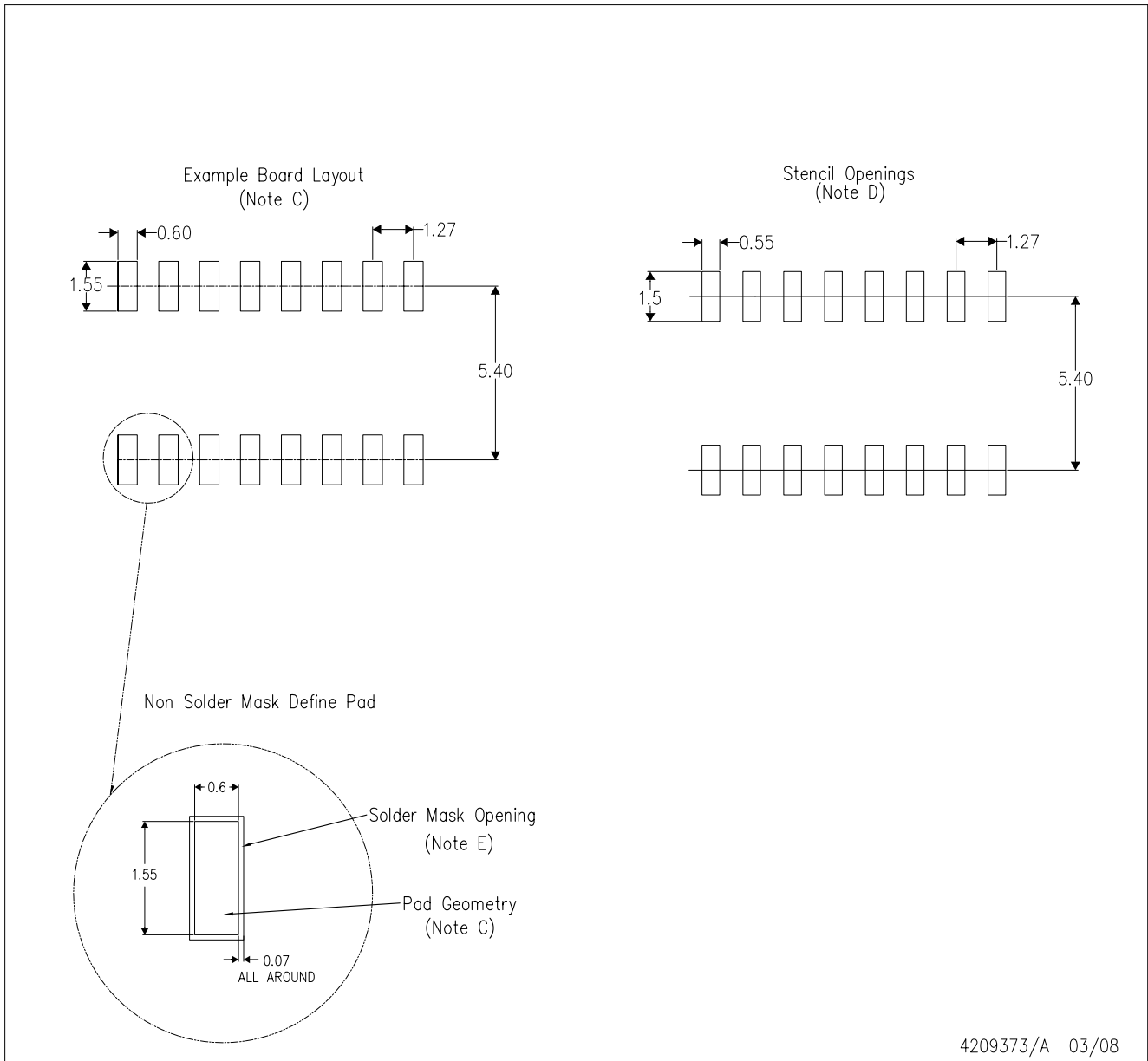
PLASTIC SMALL-OUTLINE PACKAGE



4040047-5/J 09/09

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.