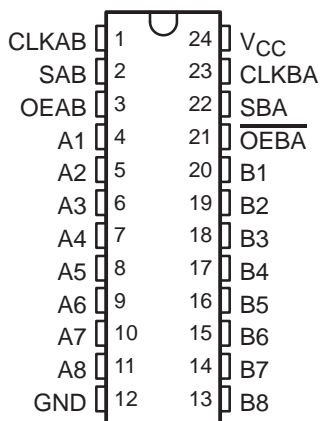


SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

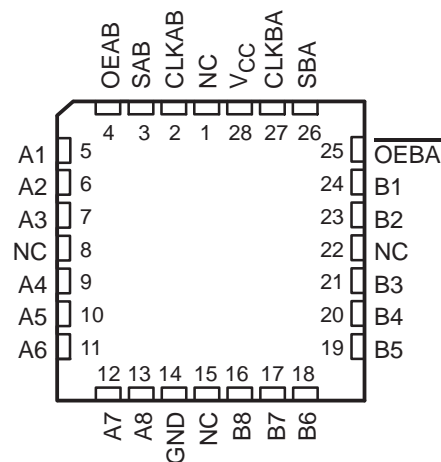
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH652 . . . JT OR W PACKAGE
SN74LVTH652 . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH652 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVTH652DW	LVTH652
		Tape and reel	SN74LVTH652DWR	
	SOP – NS	Tape and reel	SN74LVTH652NSR	LVTH652
	SSOP – DB	Tape and reel	SN74LVTH652DBR	LXH652
	TSSOP – PW	Tube	SN74LVTH652PW	LXH652
		Tape and reel	SN74LVTH652PWR	
	TVSOP – DGV	Tape and reel	SN74LVTH652DGVR	LXH652
–55°C to 125°C	CDIP – JT	Tube	SNJ54LVTH652JT	SNJ54LVTH652JT
	CFP – W	Tube	SNJ54LVTH652W	SNJ54LVTH652W
	LCCC – FK	Tube	SNJ54LVTH652FK	SNJ54LVTH652FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54LVTH652, SN74LVTH652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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description/ordering information (continued)

The 'LVTH652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH652 devices.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

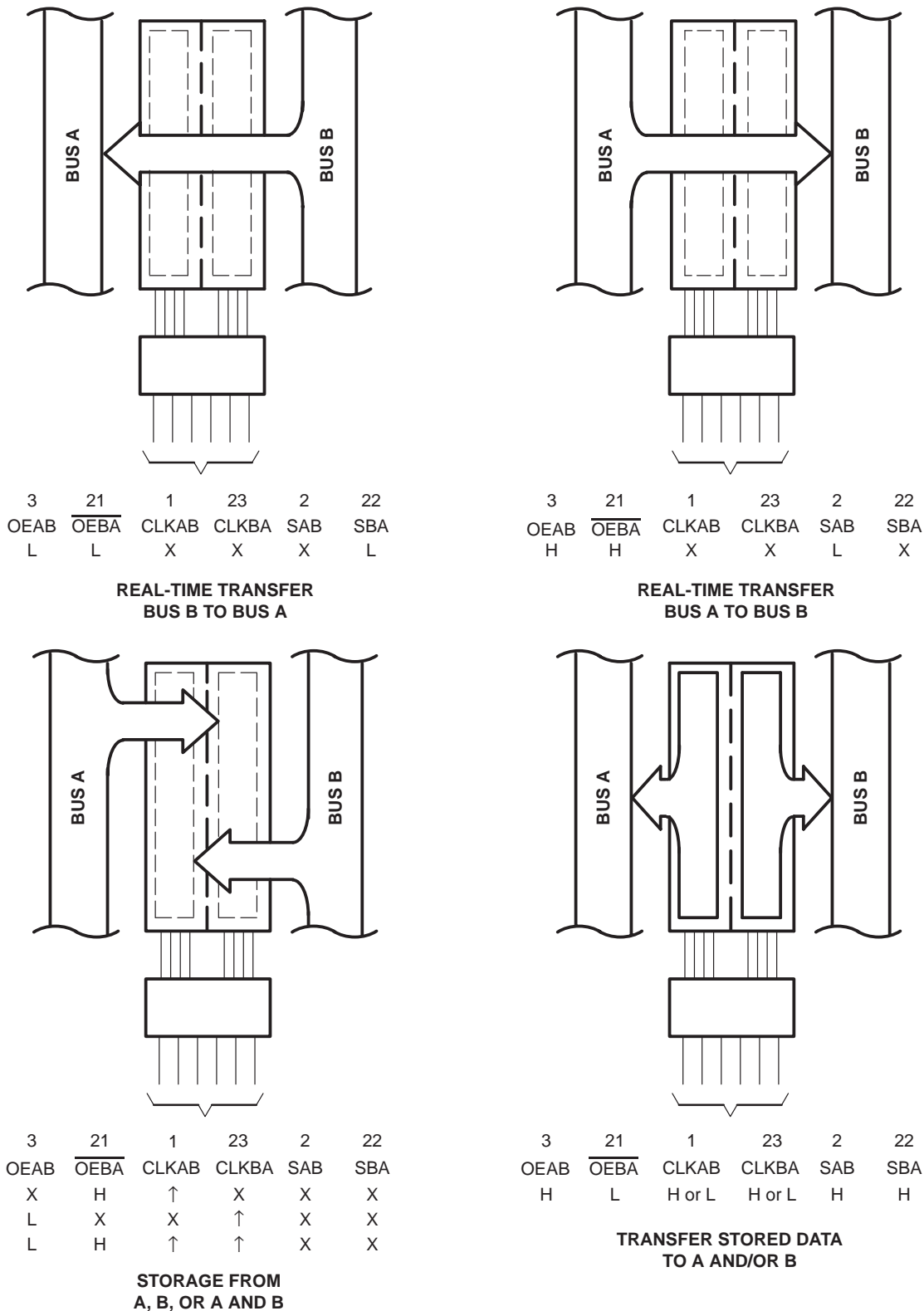
‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.



SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS706F – AUGUST 1997 – REVISED OCTOBER 2003



Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

Figure 1. Bus-Management Functions

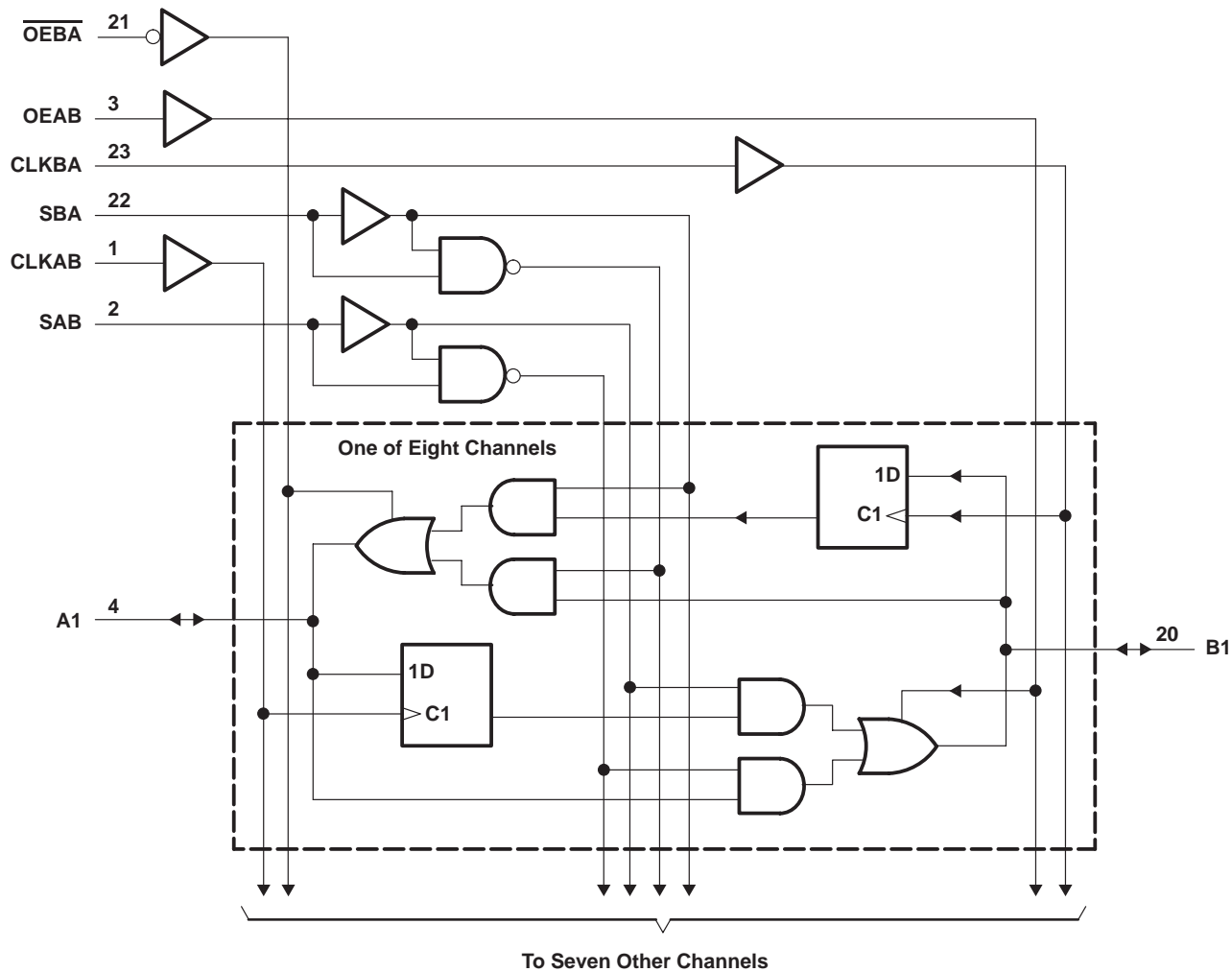
SN54LVTH652, SN74LVTH652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS706F – AUGUST 1997 – REVISED OCTOBER 2003

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

SN54LVTH652, SN74LVTH652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS706F – AUGUST 1997 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH652			SN74LVTH652			UNIT		
			MIN	TYP†	MAX	MIN	TYP†	MAX			
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V		
V_{OH}	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V		
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4					
	$V_{CC} = 3\text{ V}$		2			2					
V_{OL}	$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2			
			$I_{OL} = 24\text{ mA}$		0.5			0.5			
	$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4			0.4			
			$I_{OL} = 32\text{ mA}$		0.5			0.5			
			$I_{OL} = 48\text{ mA}$		0.55			0.55			
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1				
		$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10				
	A or B ports‡	$V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$		20			20		
				$V_I = 0$		-5			-5		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					± 100			μA		
$I_{I(\text{hold})}$	A or B ports	$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75			75		
		$V_{CC} = 3.6\text{ V}^{\S}$		$V_I = 2\text{ V}$		-75			-75		
		$V_{CC} = 3.6\text{ V}^{\S}$		$V_I = 0\text{ to }3.6\text{ V}$					± 500		
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ to }3\text{ V}$, OE/OE = don't care		$\pm 100^*$			± 100			μA		
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ to }3\text{ V}$, OE/OE = don't care		$\pm 100^*$			± 100			μA		
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$		Outputs high		0.19			0.19			
			Outputs low		5			5			
			Outputs disabled		0.19			0.19			
$\Delta I_{CC}^{\parallel}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA		
C_i	$V_I = 3\text{ V or }0$		4			4			pF		
C_{io}	$V_O = 3\text{ V or }0$		9			9			pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS706F – AUGUST 1997 – REVISED OCTOBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN54LVTH652				SN74LVTH652				UNIT
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	150		150		150		150		MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.3	1.6	1.2	1.5			ns	
		Data low	1.9	2.6	1.6	2.2				
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑	1.2		1.2		0.8		0.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH652				SN74LVTH652				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150			150	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	1.7	5	5.9		1.8	3.1	4.7	5.6		ns
t _{PHL}			1.7	5	5.9		1.8	3.1	4.7	5.6		
t _{PLH}	A or B	B or A	1.2	3.7	4.3		1.3	2.3	3.5	4.1		ns
t _{PHL}			1.2	3.7	4.3		1.3	2.4	3.5	4.1		
t _{PLH}	SBA or SAB‡	A or B	1.4	5.2	6.3		1.5	3.1	4.9	6		ns
t _{PHL}			1.4	5.2	6.3		1.5	3.4	4.9	6		
t _{PZH}	$\overline{\text{OEBA}}$	A	1	5.4	6.7		1.1	2.9	5.2	6.5		ns
t _{PZL}			1	5.4	6.7		1.1	3.1	5.2	6.5		
t _{PHZ}	$\overline{\text{OEBA}}$	A	2.2	5.9	6.5		2.3	3.5	5.5	6.1		ns
t _{PLZ}			2.2	5.9	6.3		2.3	3.7	5.5	5.9		
t _{PZH}	OEAB	B	1.2	4.9	5.9		1.3	3	4.7	5.7		ns
t _{PZL}			1.2	4.9	5.9		1.3	3.3	4.7	5.7		
t _{PHZ}	OEAB	B	1.4	5.8	7		1.5	3.6	5.6	6.7		ns
t _{PLZ}			1.4	5.9	6.6		1.5	3.7	5.6	6.3		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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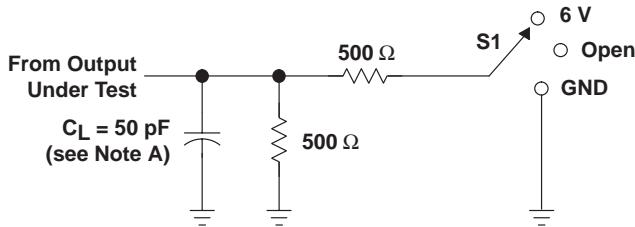
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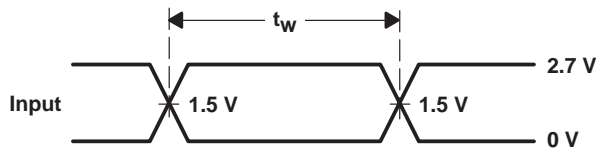
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SCBS706F – AUGUST 1997 – REVISED OCTOBER 2003

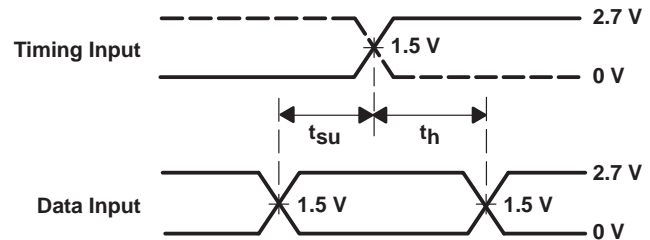
PARAMETER MEASUREMENT INFORMATION



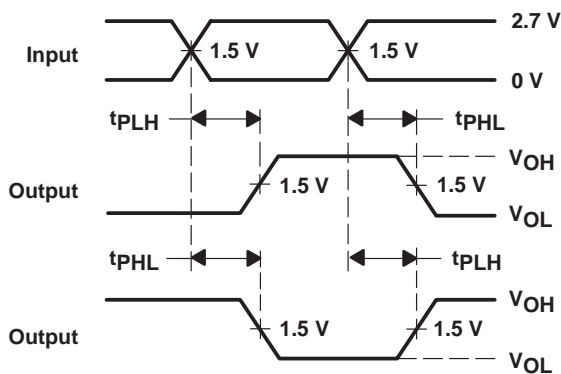
LOAD CIRCUIT



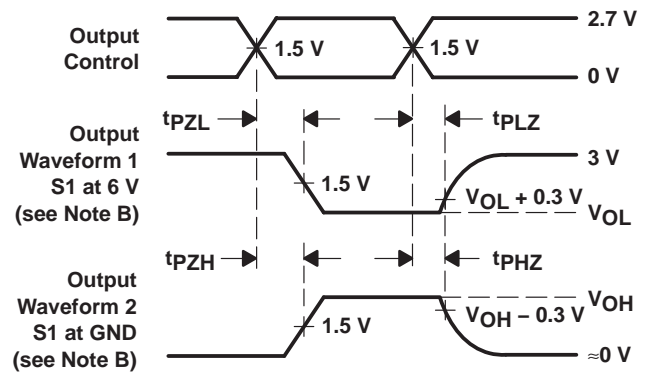
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265