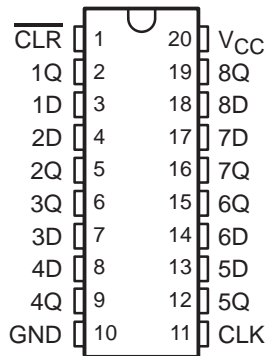


SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

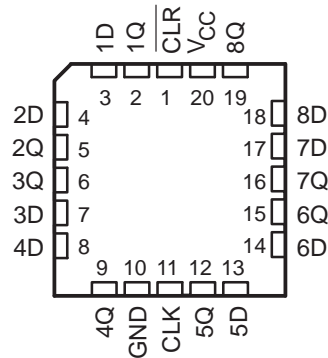
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down To 2.7 V
- Buffered Clock and Direct-Clear Inputs
- Individual Data Input to Each Flip-Flop
- I_{off} Supports Partial-Power-Down-Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH273 . . . J PACKAGE
SN74LVTH273 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH273 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH273 devices are positive-edge-triggered flip-flops with a direct-clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74LVTH273DW	LVTH273
		Tape and reel	SN74LVTH273DWR	
	SOP – NS	Tape and reel	SN74LVTH273NSR	LVTH273
	SSOP – DB	Tape and reel	SN74LVTH273DBR	LXH273
-55°C to 125°C	TSSOP – PW	Tube	SN74LVTH273PW	LXH273
		Tape and reel	SN74LVTH273PWR	
	CDIP – J	Tube	SNJ54LVTH273J	SNJ54LVTH273J
		LCCC – FK	Tube	SNJ54LVTH273FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54LVTH273, SN74LVTH273

3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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description/ordering information (continued)

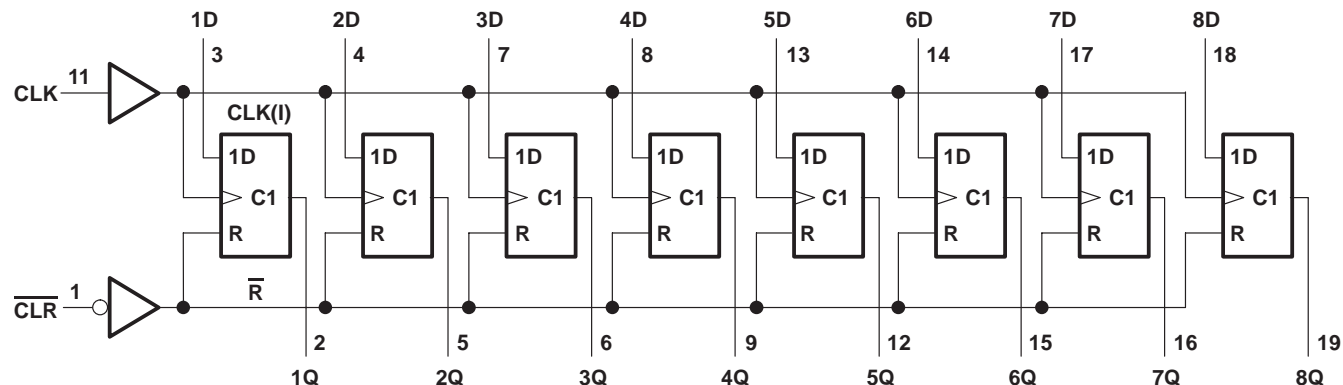
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q_0

logic diagram (positive logic)



SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH273	96 mA
SN74LVTH273	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH273	48 mA
SN74LVTH273	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
DW package	58°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

	SN54LVTH273		SN74LVTH273		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10		10	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH273, SN74LVTH273

3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH273			SN74LVTH273			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$			$V_{CC}-0.2$			$V_{CC}-0.2$	V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$			2.4			2.4	
	$V_{CC} = 3\text{ V}$			2			2	
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$					0.2	0.2
		$I_{OL} = 24\text{ mA}$					0.5	0.5
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$					0.4	0.4
		$I_{OL} = 32\text{ mA}$					0.5	0.5
		$I_{OL} = 48\text{ mA}$					0.55	
		$I_{OL} = 64\text{ mA}$						0.55
I_I	$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$					10	10	μA
	Control inputs $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$					± 1	± 1	
	Data inputs $V_{CC} = 3.6\text{ V}$					1	1	
		$V_I = 0$				-5	-5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						± 100	μA
$I_{I(\text{hold})}$	Data inputs $V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75		75		μA
		$V_I = 2\text{ V}$		-75		-75		
	$V_{CC} = 3.6\text{ V}^\ddagger$, $V_I = 0\text{ to }3.6\text{ V}$						500 -750	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high				0.19	0.19	mA
		Outputs low				5	5	
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$					0.2	0.2	mA
C_i	$V_I = 3\text{ V or }0$			4		4		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH273				SN74LVTH273				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150				150				MHz
t_w	Pulse duration	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	Data high or low before CLK↑	2.3		2.7		2.3		2.7	ns
		CLR high before CLK↑	2.3		2.7		2.3		2.7	
t_h	Hold time, data high or low after CLK↑	0		0		0		0		ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH273				SN74LVTH273				UNIT	
			$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 2.7$ V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150				150				MHz	
t_{PLH}	CLK	Any Q	1.6	5	5.6		1.7	3.2	4.9	5.5		ns
t_{PHL}			1.8	4.9	5.2		1.9	3.2	4.8	5.1		
t_{PHL}	\overline{CLR}	Any Q	1.5	4.4	4.8		1.6	2.7	4.3	4.7		ns

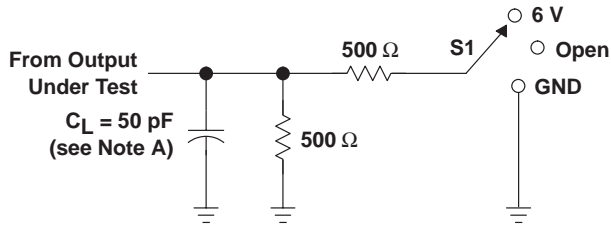
† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

SN54LVTH273, SN74LVTH273

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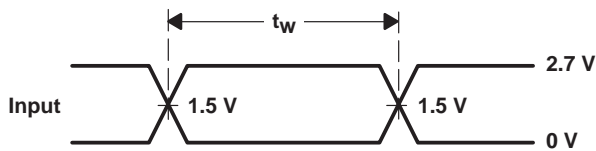
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PARAMETER MEASUREMENT INFORMATION

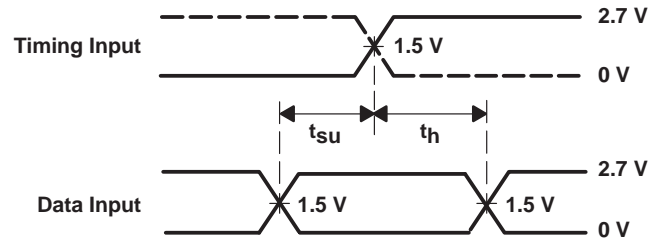


LOAD CIRCUIT

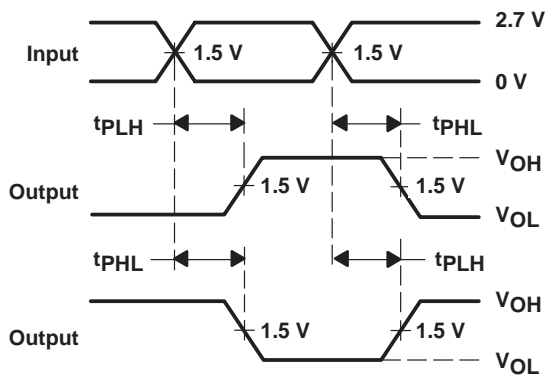
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



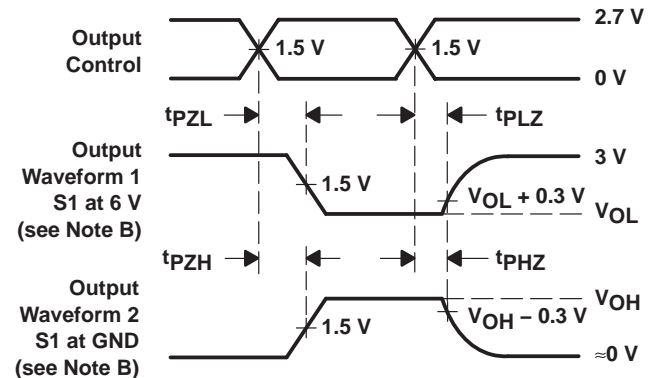
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



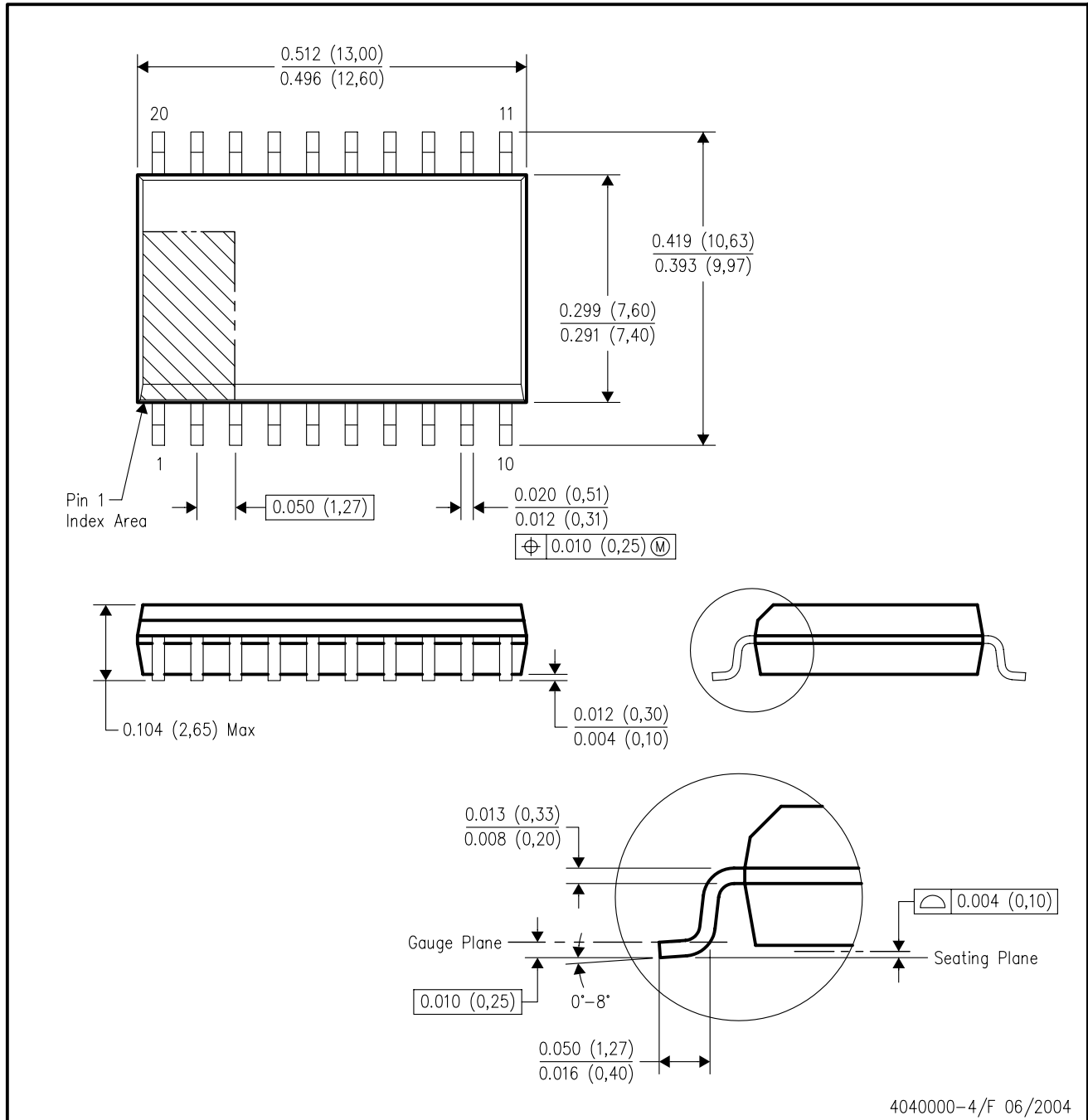
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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