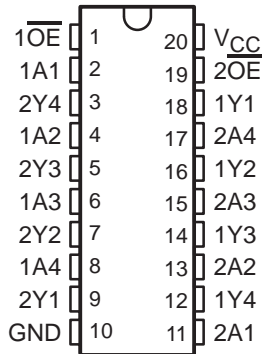


SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

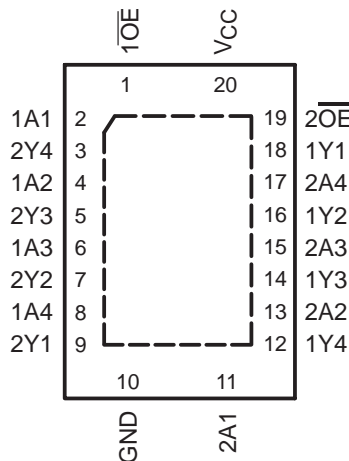
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

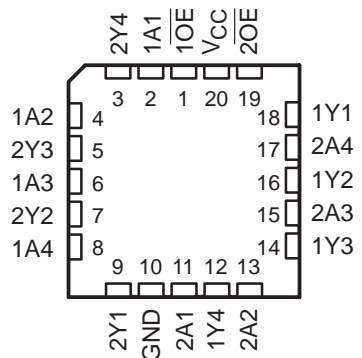
SN54LVTH244A . . . J OR W PACKAGE
SN74LVTH244A . . . DB, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVTH244A . . . RGY PACKAGE
(TOP VIEW)



SN54LVTH244A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74LVTH244ARGYR	LXH244A
	SOIC – DW	Tube	SN74LVTH244ADW	LVTH244A
		Tape and reel	SN74LVTH244ADWR	
	SOP – NS	Tape and reel	SN74LVTH244ANSR	LVTH244A
	SSOP – DB	Tape and reel	SN74LVTH244ADBR	LXH244A
	TSSOP – PW	Tape and reel	SN74LVTH244APWR	LXH244A
	VFBGA – GQN	Tape and reel	SN74LVTH244AGQNR	LXH244A
SN74LVTH244AZQNR				
-55°C to 125°C	CDIP – J	Tube	SNJ54LVTH244AJ	SNJ54LVTH244AJ
	CFP – W	Tube	SNJ54LVTH244AW	SNJ54LVTH244AW
	LCCC – FK	Tube	SNJ54LVTH244AFK	SNJ54LVTH244AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH244A, SN74LVTH244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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description/ordering information (continued)

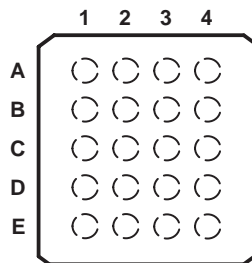
The 'LVTH244A devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the devices pass data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74LVTH244A . . . GQN OR ZQN PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4
A	1A1	$\overline{1OE}$	V_{CC}	$\overline{2OE}$
B	1A2	2A4	2Y4	1Y1
C	1A3	2Y3	2A3	1Y2
D	1A4	2A2	2Y2	1Y3
E	GND	2Y1	2A1	1Y4

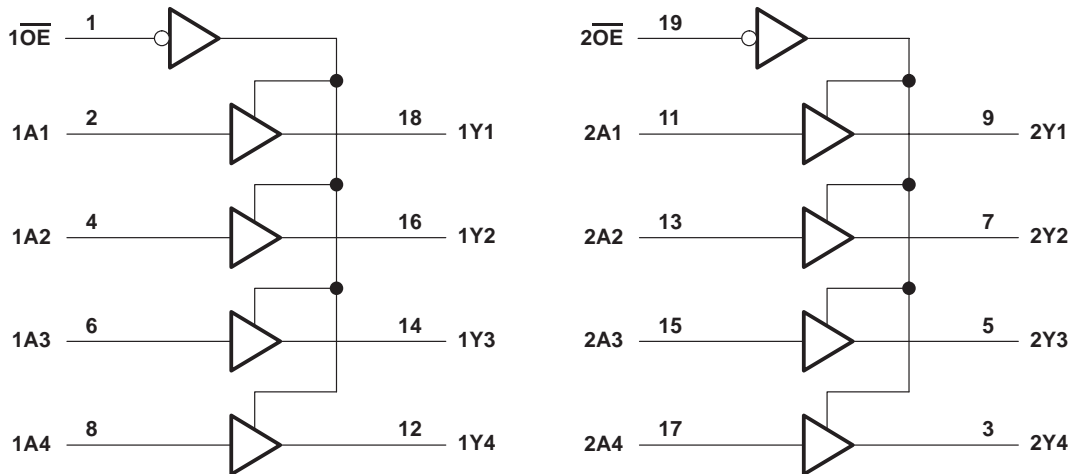
FUNCTION TABLE (each buffer)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH244A	96 mA
SN74LVTH244A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH244A	48 mA
SN74LVTH244A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN/ZQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LVTH244A, SN74LVTH244A
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 5)

		SN54LVTH244A		SN74LVTH244A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH244A		SN74LVTH244A		UNIT
			MIN	TYP†	MAX	MIN	
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$	-1.2		-1.2		V
V_{OH}		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$		$V_{CC}-0.2$		V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4		2.4		
		$V_{CC} = 3\text{ V}$	2		2		
V_{OL}		$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2		V
			$I_{OL} = 24\text{ mA}$		0.5		
		$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4		
			$I_{OL} = 32\text{ mA}$		0.5		
			$I_{OL} = 48\text{ mA}$		0.55		
			$I_{OL} = 64\text{ mA}$		0.55		
I_I		Control inputs $V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$	50		10		μA
			± 1		± 1		
I_I		Data inputs $V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$		1		μA
			$V_I = 0$		-5		
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$			± 100		μA
$I_I(\text{hold})$		$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75		μA
			$V_I = 2\text{ V}$		-75		
		$V_{CC} = 3.6\text{ V}\ddagger$, $V_I = 0\text{ to }3.6\text{ V}$				500 -750	
I_{OZH}		$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$	5		5		μA
I_{OZL}		$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$	-5		-5		μA
I_{OZPU}		$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, OE = don't care	$\pm 100^*$		± 100		μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, OE = don't care	$\pm 100^*$		± 100		μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.39		mA
			Outputs low		14		
			Outputs disabled		0.39		
$\Delta I_{CC}\S$		$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	0.2		0.2		mA
C_i		$V_I = 3\text{ V or }0$	3		3		pF
C_o		$V_O = 3\text{ V or }0$	7		7		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



SN54LVTH244A, SN74LVTH244A
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

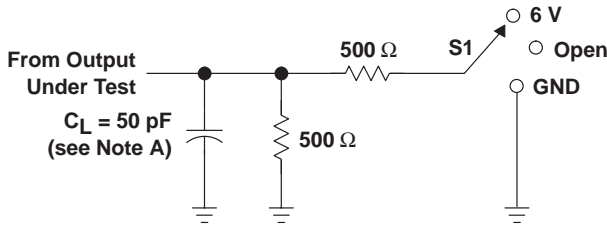
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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

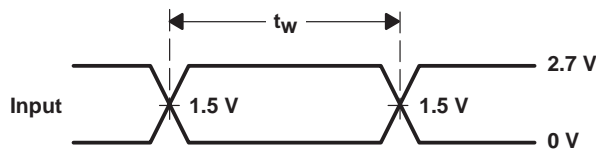
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH244A				SN74LVTH244A				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
tPLH	A	Y	0.5	3.8	4.1		1.1	2.3	3.5	3.8		ns
tPHL			0.5	3.8	3.9		1.3	2.1	3.3	3.6		
tPZH	\overline{OE}	Y	0.8	5	6		1.1	2.5	4.5	5.3		ns
tPZL			0.8	5	5.4		1.4	2.7	4.4	4.9		
tPHZ	\overline{OE}	Y	1.3	5.5	5.8		1.9	2.8	4.4	4.5		ns
tPLZ			1.2	4.7	4.8		1.8	2.9	4.4	4.4		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

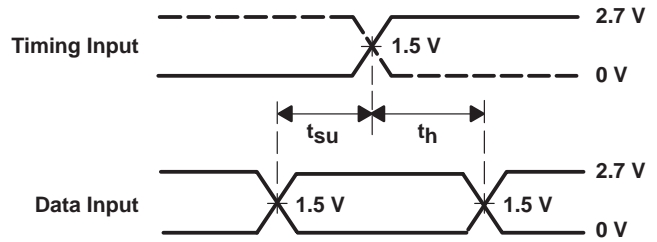


LOAD CIRCUIT

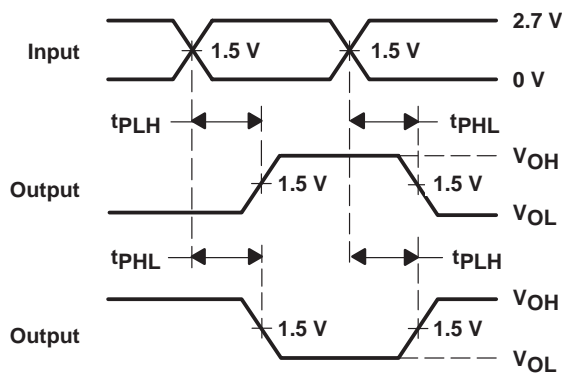


VOLTAGE WAVEFORMS
PULSE DURATION

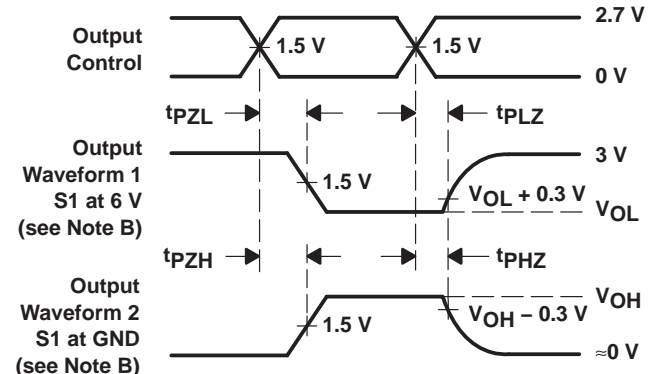
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



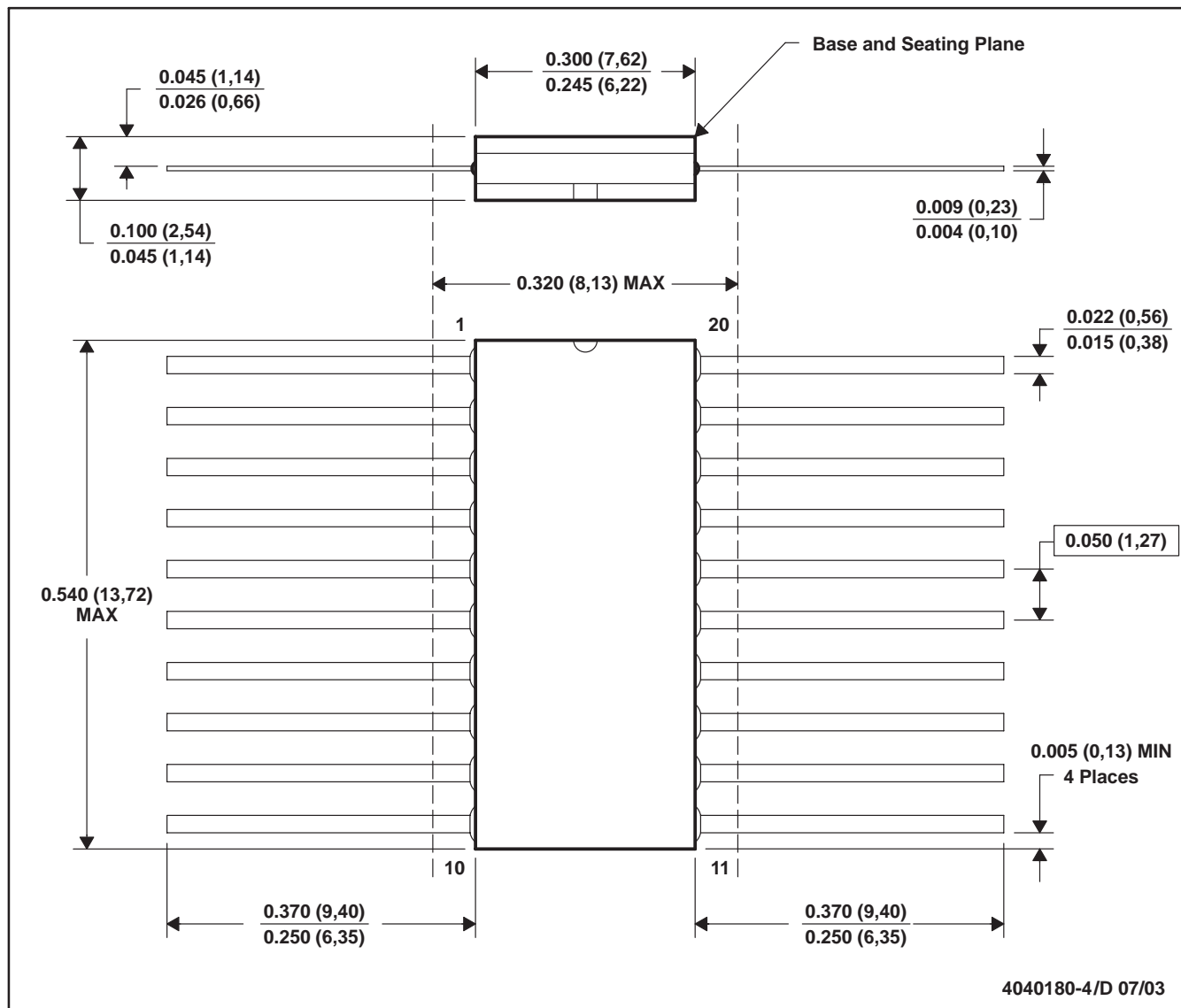
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

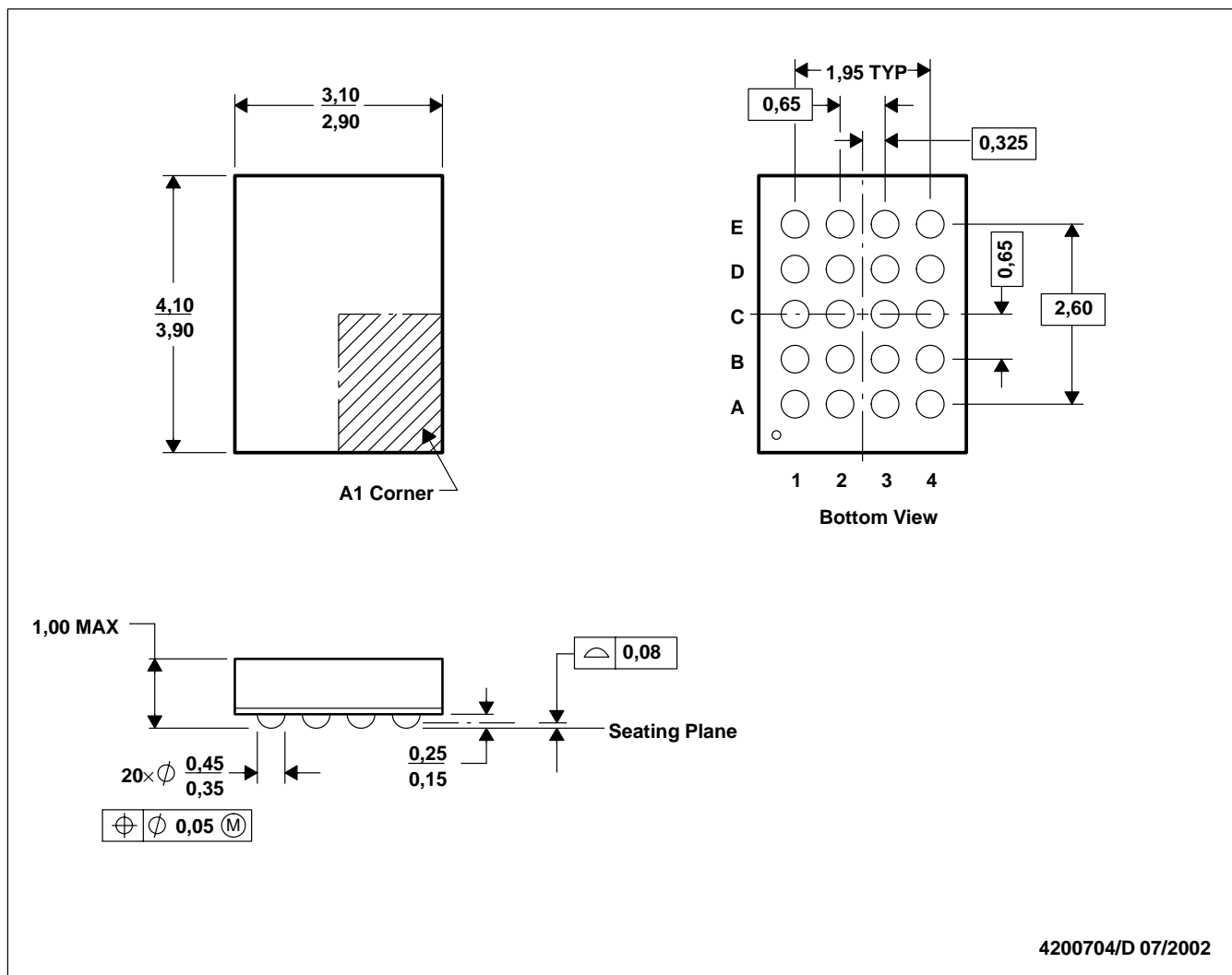
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

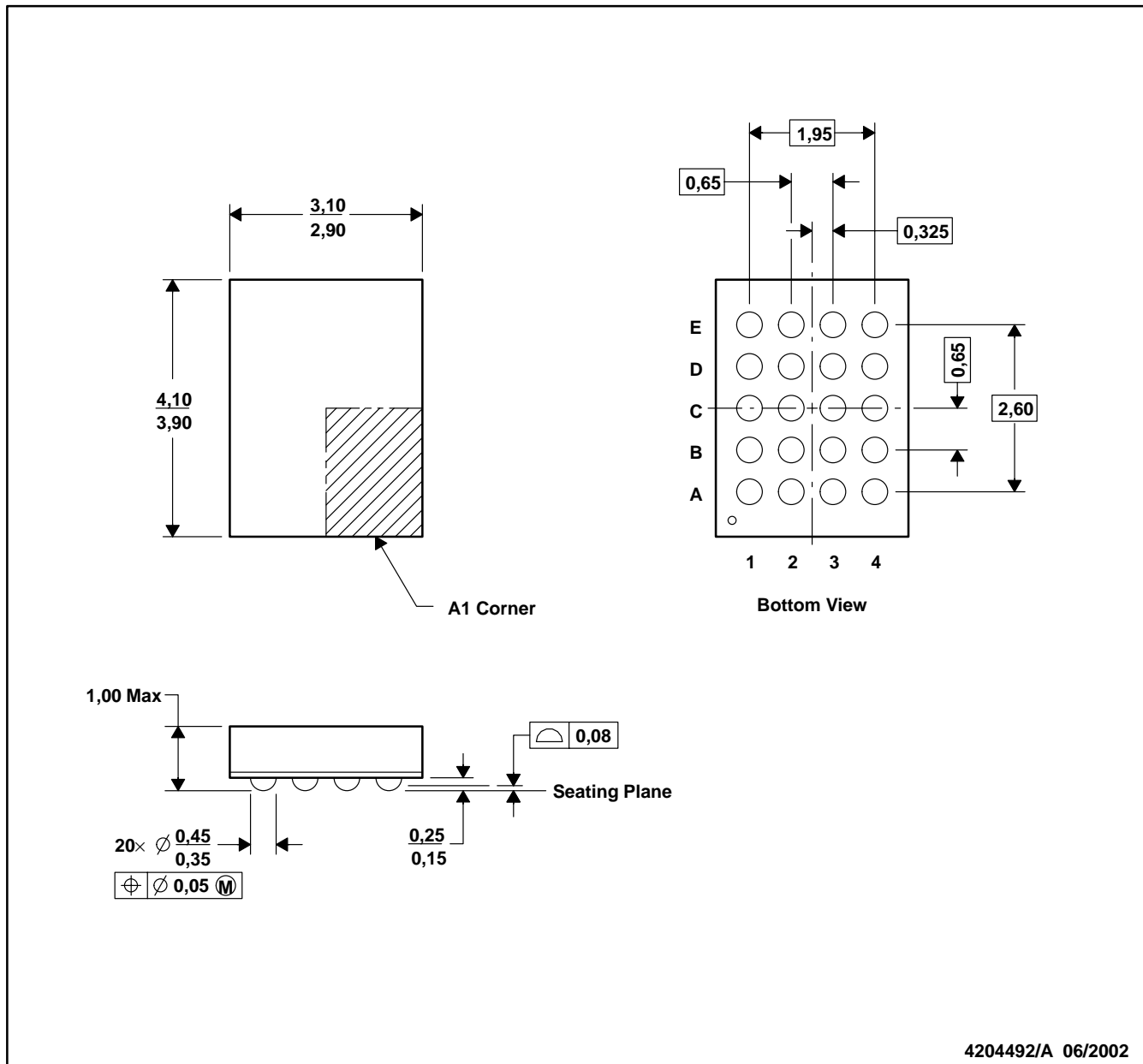


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - MicroStar Junior™ configuration
 - Falls within JEDEC MO-225 variation BC.
 - This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



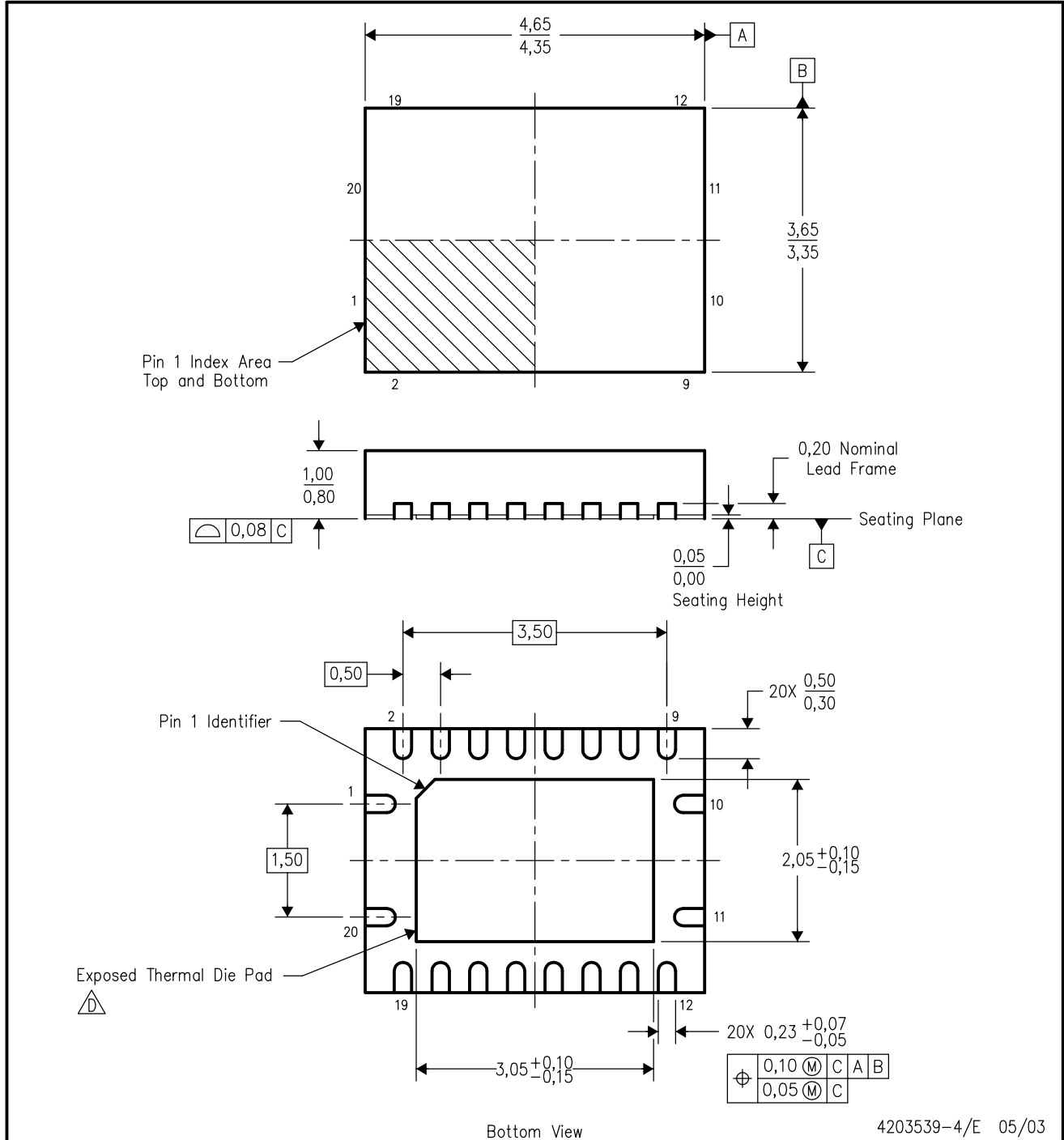
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ configuration.
 - D. Fall within JEDEC MO-225 variation BC.
 - E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.



RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



Bottom View

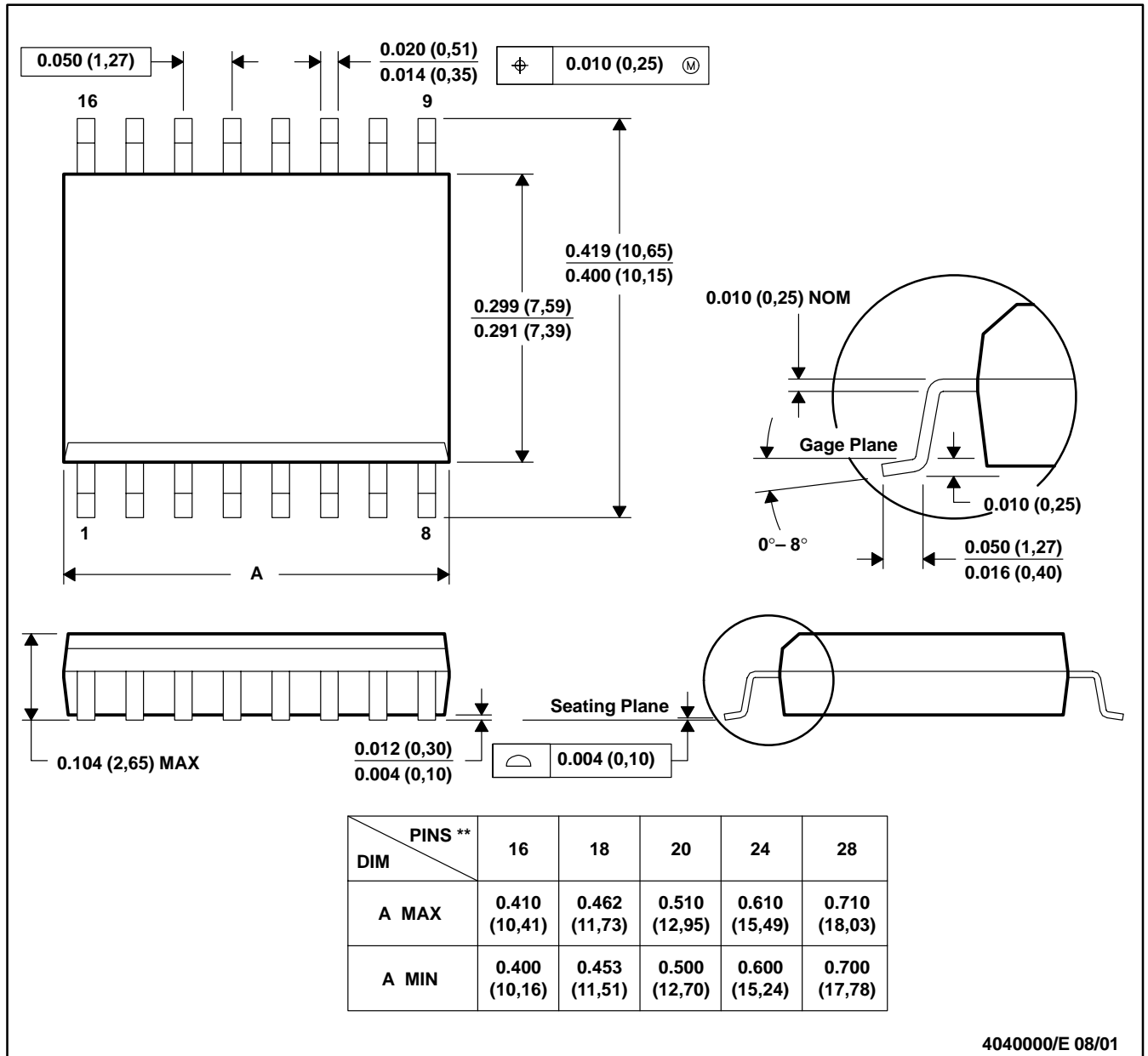
4203539-4/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

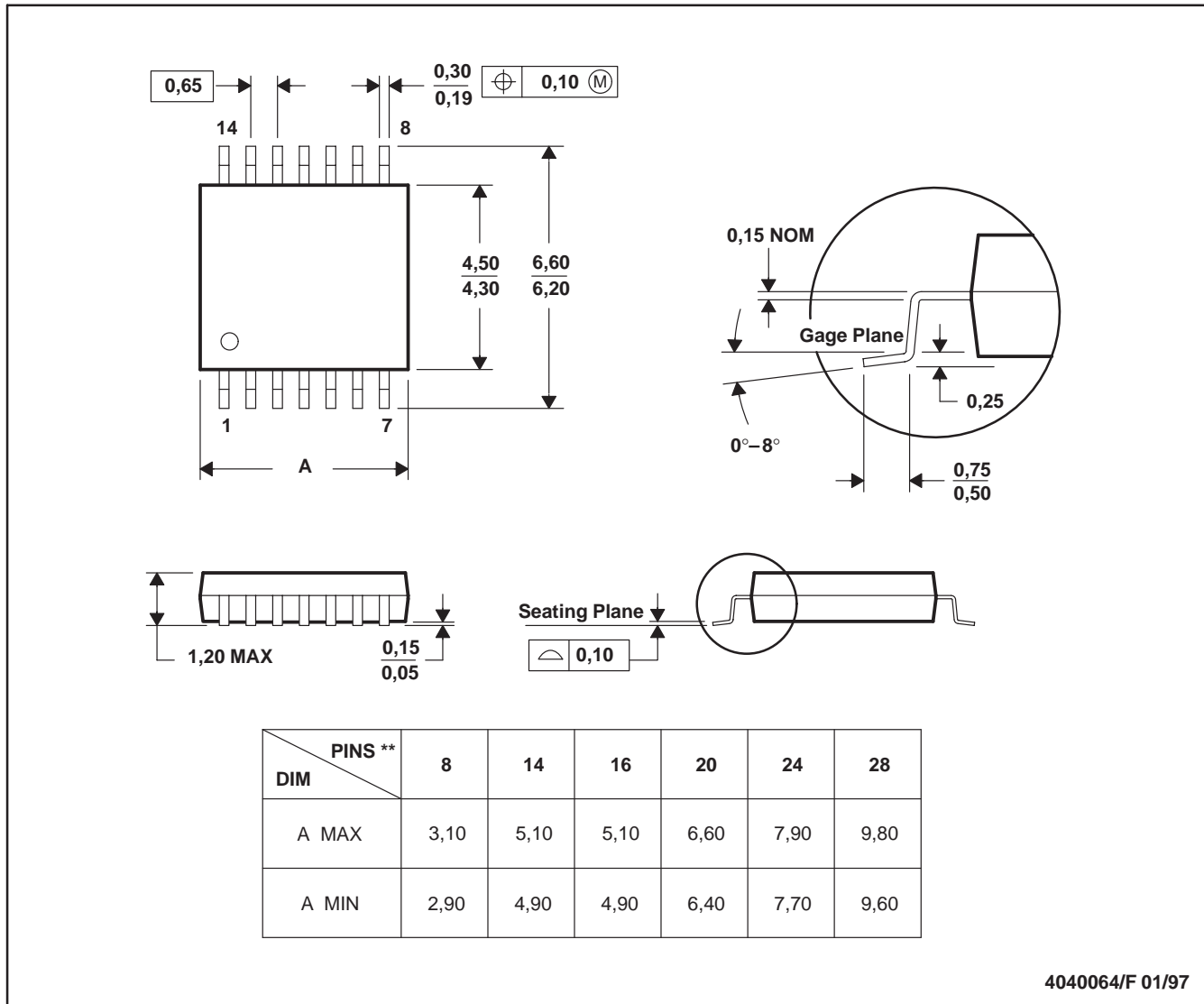


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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