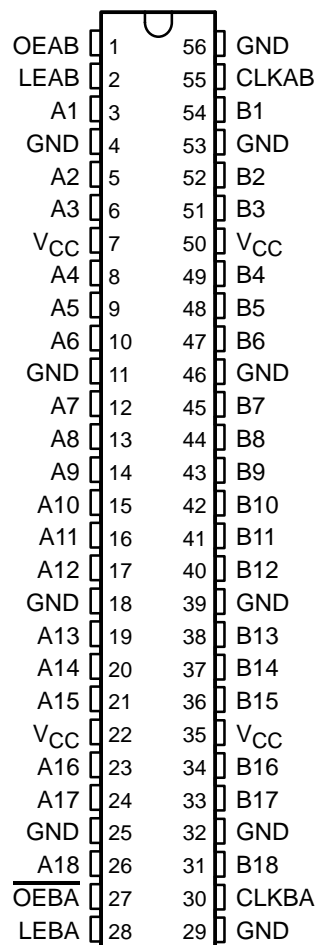


# SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700E – JULY 1997 – REVISED NOVEMBER 2002

- Members of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH16501 . . . WD PACKAGE  
SN74LVTH16501 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description/ordering information

The 'LVTH16501 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH16501DL	LVTH16501
		Tape and reel	SN74LVTH16501DLR	
–55°C to 125°C	TSSOP – DGG	Tape and reel	SN74LVTH16501DGGR	LVTH16501
	CFP – WD	Tube	SNJ54LVTH16501WD	SNJ54LVTH16501WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVTH16501, SN74LVTH16501

## 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### description/ordering information (continued)

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, and CLKBA. The output enables are complementary (OEAB is active high and  $\overline{OEBA}$  is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	$B_0^\ddagger$
H	L	L	X	$B_0^\S$

† A-to-B data flow is shown; B-to-A flow is similar, but uses  $\overline{OEBA}$ , LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

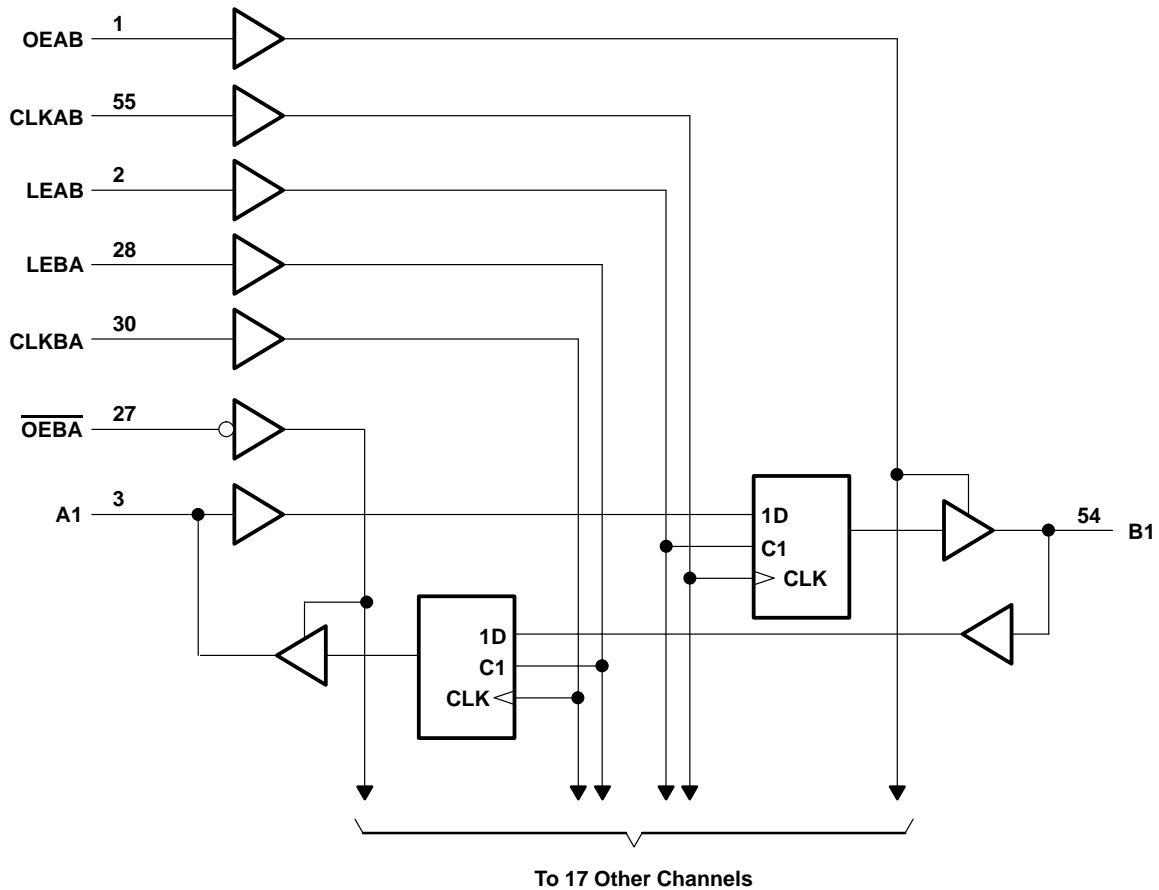
§ Output level before the indicated steady-state input conditions were established



**SN54LVTH16501, SN74LVTH16501**  
**3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH16501 .....	96 mA
SN74LVTH16501 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH16501 .....	48 mA
SN74LVTH16501 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	64°C/W
DL package .....	56°C/W
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



**SN54LVTH16501, SN74LVTH16501**  
**3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 4)**

		SN54LVTH16501		SN74LVTH16501		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54LVTH16501		SN74LVTH16501		UNIT
			MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA	-1.2		-1.2		V
V <sub>OH</sub>		V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V
		V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = -8 mA	2.4		2.4		
		V <sub>CC</sub> = 3 V	2		2		
V <sub>OL</sub>		V <sub>CC</sub> = 2.7 V	0.2		0.2		V
			0.5		0.5		
		V <sub>CC</sub> = 3 V	0.4		0.4		
			0.5		0.5		
			0.55		0.55		
			0.55		0.55		
I <sub>I</sub>		Control inputs	±1		±1		μA
			10		10		
		A or B ports‡	20		20		
			-5		-5		
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V			±100		μA
I <sub>I</sub> (hold)		A or B ports	75		75		μA
			-75		-75		
		V <sub>CC</sub> = 3.6 V§, V <sub>I</sub> = 0 to 3.6 V			±500		
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE/OE = don't care	±100*		±100		μA
I <sub>OZPD</sub>		V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE/OE = don't care	±100*		±100		μA
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	0.19		0.19		mA
			5		5		
			0.19		0.19		
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	0.2		0.2		mA
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0	4		4		pF
C <sub>io</sub>		V <sub>O</sub> = 3 V or 0	10		10		pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ Unused pins at V<sub>CC</sub> or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**SN54LVTH16501, SN74LVTH16501**  
**3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH16501				SN74LVTH16501				UNIT	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$f_{\text{clock}}$	Clock frequency	150		150		150		150		MHz	
$t_w$	Pulse duration	LE high		3.3		3.3		3.3		ns	
		CLK high or low		3.3		3.3		3.3			
$t_{\text{su}}$	Setup time	A before CLKAB $\uparrow$		2.5		2.8		2.1		ns	
		B before CLKBA $\uparrow$		2.5		2.8		2.1			
		A or B before LE $\downarrow$	CLK high		3.4		2.8		2.4		
			CLK low		2.2		1.3		1.4		
$t_h$	Hold time	A or B after CLK $\uparrow$		2.2		1.5		1		ns	
		A or B after LE $\downarrow$		2.1		1.9		1.7			

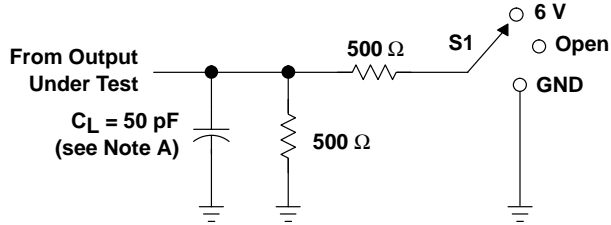
switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16501				SN74LVTH16501				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	
			MIN	MAX	MIN	MAX	MIN	TYP $\dagger$	MAX	MIN	
$f_{\text{max}}$			150		150		150			150	MHz
$t_{\text{PLH}}$	B or A	A or B	1.2 4.3		4.7		1.3 2.7 3.7			4	ns
$t_{\text{PHL}}$			1.2 4.3		4.6		1.3 2.4 3.7			4	
$t_{\text{PLH}}$	LEBA or LEAB	A or B	1.4 6.2		6.6		1.5 3.4 5.1			5.7	ns
$t_{\text{PHL}}$			1.4 5.9		6.5		1.5 3.5 5.1			5.7	
$t_{\text{PLH}}$	CLKBA or CLKAB	A or B	1.2 6		6.7		1.3 3.5 5.1			5.7	ns
$t_{\text{PHL}}$			1.2 5.9		6.6		1.3 3.4 5.1			5.7	
$t_{\text{PZH}}$	$\overline{\text{OEBA}}$ or OEAB	A or B	1.2 5.5		5.9		1.3 3.4 4.8			5.5	ns
$t_{\text{PZL}}$			1.2 5.5		5.9		1.3 3.4 4.8			5.5	
$t_{\text{PHZ}}$	$\overline{\text{OEBA}}$ or OEAB	A or B	1.6 6.3		6.7		1.7 4.2 5.8			6.3	ns
$t_{\text{PLZ}}$			1.6 6.1		6.6		1.7 3.8 5.8			6.3	

$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

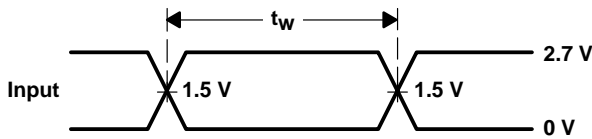


PARAMETER MEASUREMENT INFORMATION

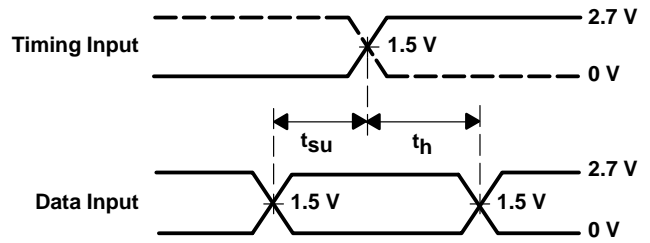


LOAD CIRCUIT

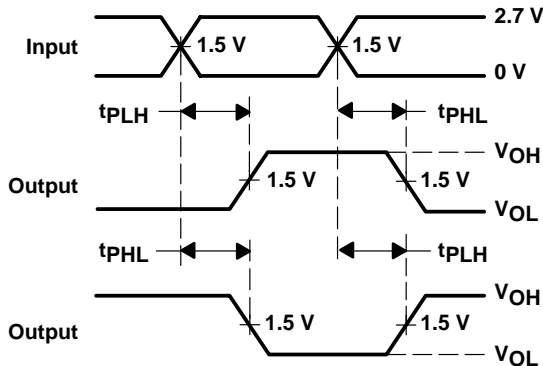
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



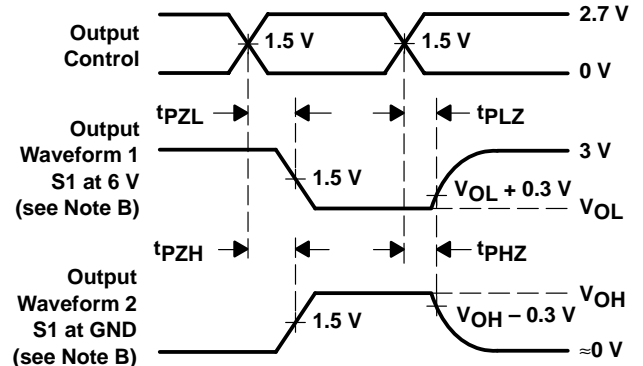
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

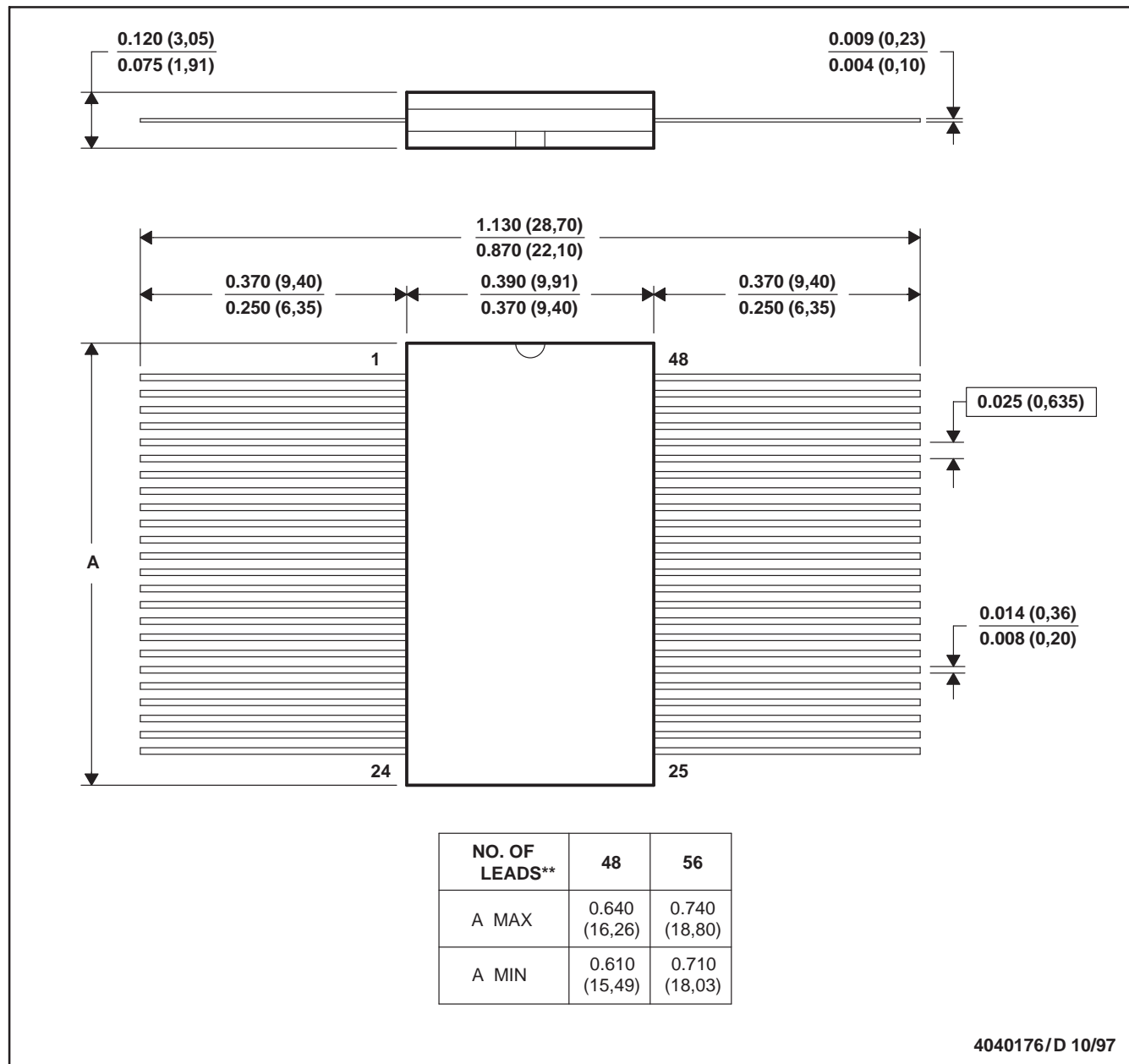
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265