

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

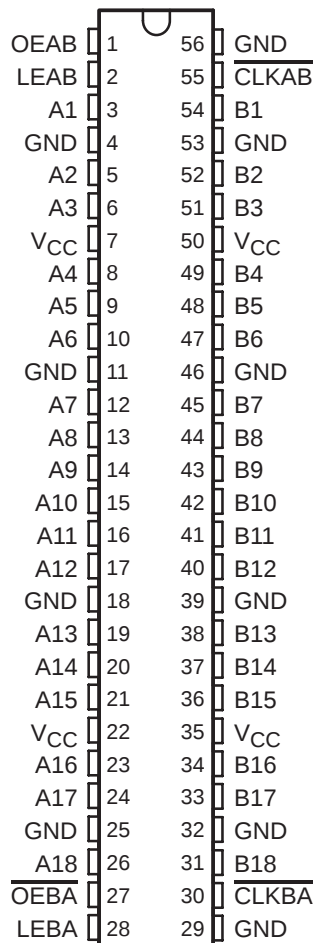
SCBS701F – JULY 1997 – REVISED SEPTEMBER 2003

- Members of the Texas Instruments Widebus™ Family
- UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH16500 . . . WD PACKAGE
SN74LVTH16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74LVTH16500DL	LVTH16500
		Tape and reel	SN74LVTH16500DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH16500DGGR	LVTH16500
	VFBGA – GQL	Tape and reel	SN74LVTH16500GQLR	LL500
	VFBGA – ZQL (Pb-free)		SN74LVTH16500ZQLR	
-55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16500WD	SNJ54LVTH16500WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. $\overline{\text{OEAB}}$ is active high. When $\overline{\text{OEAB}}$ is high, the B-port outputs are active. When $\overline{\text{OEAB}}$ is low, the B-port outputs are in the high-impedance state.

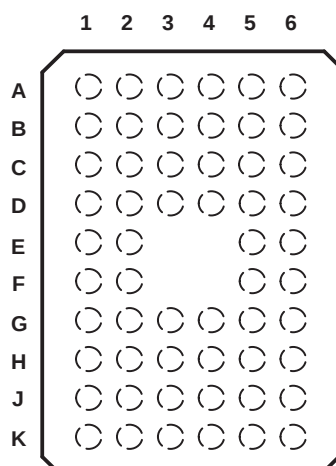
Data flow for B to A is similar to that of A to B, but uses $\overline{\text{OEBA}}$, LEBA , and $\overline{\text{CLKBA}}$. The output enables are complementary ($\overline{\text{OEAB}}$ is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

These devices are fully specified for hot-insertion applications using I_{OFF} and power-up 3-state. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	A1	LEAB	OEAB	GND	$\overline{\text{CLKAB}}$	B1
B	A3	A2	GND	GND	B2	B3
C	A5	A4	V_{CC}	V_{CC}	B4	B5
D	A7	A6	GND	GND	B6	B7
E	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
H	A14	A15	V_{CC}	V_{CC}	B15	B14
J	A16	A17	GND	GND	B17	B16
K	A18	$\overline{\text{OEBA}}$	LEBA	GND	$\overline{\text{CLKBA}}$	B18

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FUNCTION TABLE[†]

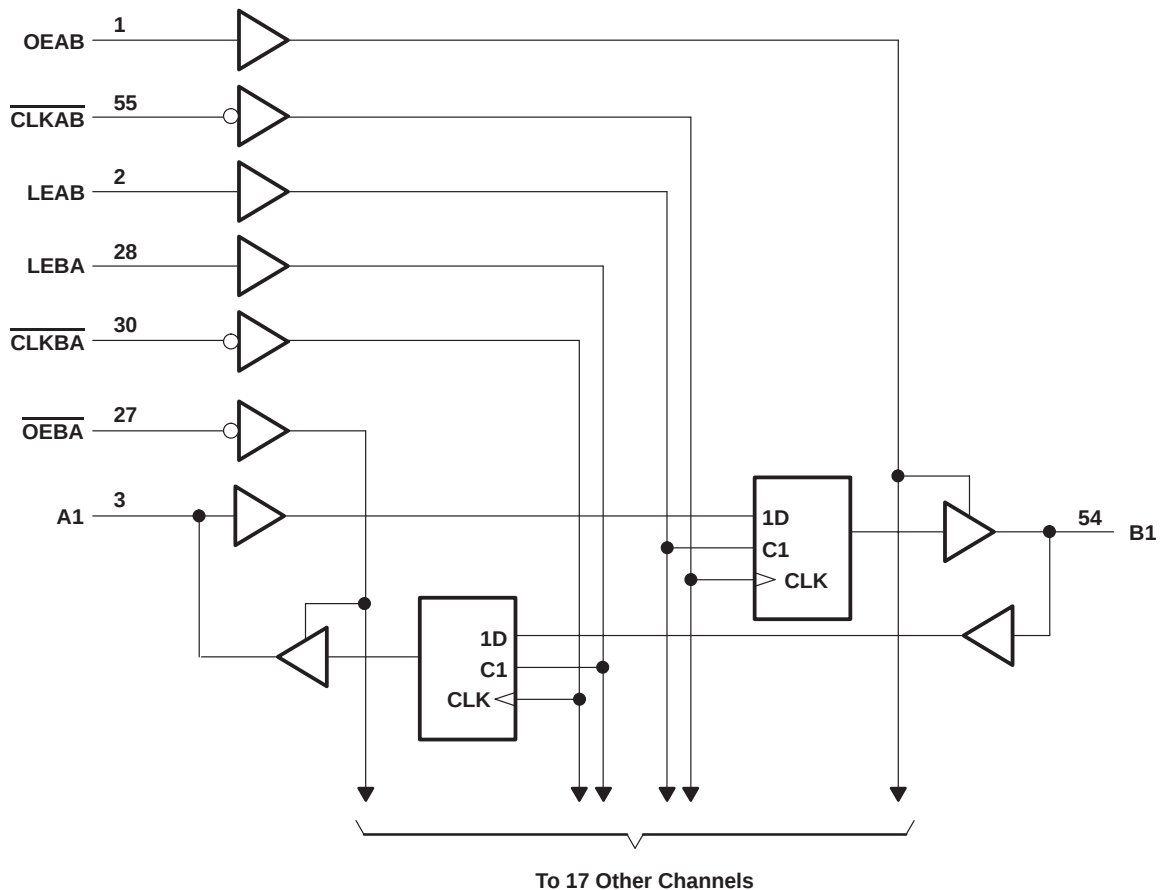
INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ [‡]
H	L	L	X	B ₀ [§]

[†] A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16500	96 mA
SN74LVTH16500	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16500	48 mA
SN74LVTH16500	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH16500		SN74LVTH16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16500		SN74LVTH16500		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA		-1.2		-1.2		V	
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2		V _{CC} -0.2		V	
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4		2.4			
		V _{CC} = 3 V	I _{OH} = -24 mA	2					
			I _{OH} = -32 mA			2			
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2		0.2		V	
			I _{OL} = 24 mA	0.5		0.5			
		V _{CC} = 3 V	I _{OL} = 16 mA	0.4		0.4			
			I _{OL} = 32 mA	0.5		0.5			
			I _{OL} = 48 mA	0.55					
			I _{OL} = 64 mA			0.55			
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1		μA	
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10		10			
	A or B ports‡	V _{CC} = 3.6 V	V _I = 5.5 V		20		20		
			V _I = V _{CC}		1		1		
			V _I = 0		-5		-5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA	
I _I (hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V		75		75		μA
			V _I = 2 V		-75		-75		
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V				±500		±500	
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		μA	
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		μA	
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19		0.19		mA
			Outputs low		5		5		
			Outputs disabled		0.19		0.19		
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA	
C _i		V _I = 3 V or 0		4		4		pF	
C _{io}		V _O = 3 V or 0		10		10		pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVTH16500				SN74LVTH16500				UNIT
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150		MHz
t_w	Pulse duration	LE high		3.3		3.3		3.3		3.3		ns
		CLK high or low		3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before $\overline{\text{CLKAB}}\downarrow$		3.1		3.1		2.9		2.9		ns
		B before $\overline{\text{CLKBA}}\downarrow$		3.1		3.1		2.9		2.9		
		A or B before LE $\downarrow$	$\overline{\text{CLK}}$ high	1.5		0.6		1.4		0.5		
			$\overline{\text{CLK}}$ low	3.1		2.5		2.9		2.3		
t_h	Hold time	A or B after $\overline{\text{CLK}}\downarrow$		0.4		0.4		0.4		0.4		ns
		A or B after LE $\downarrow$		1.7		1.7		1.6		1.6		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

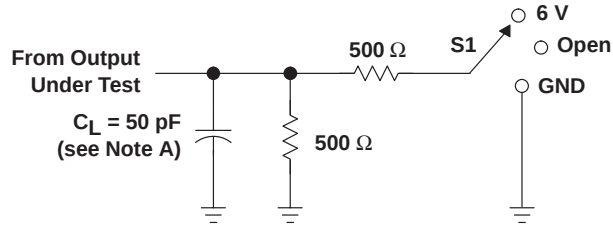
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16500				SN74LVTH16500				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP [†]	MAX	MIN		MAX
f _{max}			150		150		150			150		MHz
t _{PLH}	B or A	A or B	1.2	3.9	4.1		1.3	2.8	3.7	4		ns
t _{PHL}			1.2	3.9	4.1		1.3	2.6	3.7	4		
t _{PLH}	LEBA or LEAB	A or B	1.4	5.5	5.9		1.5	3.8	5.1	5.7		ns
t _{PHL}			1.4	5.5	5.9		1.5	3.8	5.1	5.7		
t _{PLH}	$\overline{\text{CLKBA}}$ or $\overline{\text{CLKAB}}$	A or B	1.2	5.3	6.1		1.3	3.6	5	5.9		ns
t _{PHL}			1.2	5.3	6.1		1.3	3.5	5	5.9		
t _{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1.2	5.1	5.8		1.3	3.6	4.8	5.5		ns
t _{PZL}			1.2	5.1	5.8		1.3	3.6	4.8	5.5		
t _{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1.6	6.1	6.6		1.7	4.5	5.8	6.3		ns
t _{PLZ}			1.6	6.1	6.6		1.7	4.1	5.8	6.3		

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

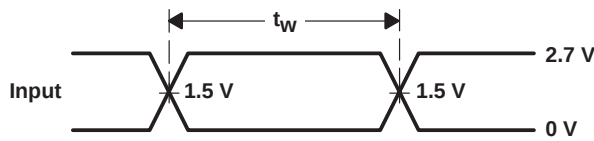
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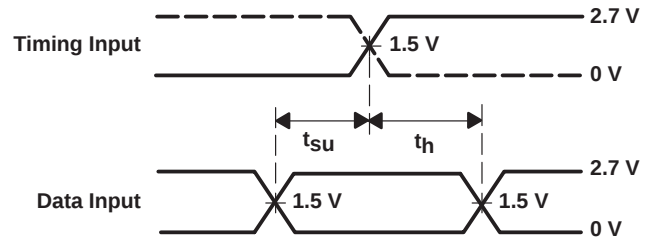
PARAMETER MEASUREMENT INFORMATION



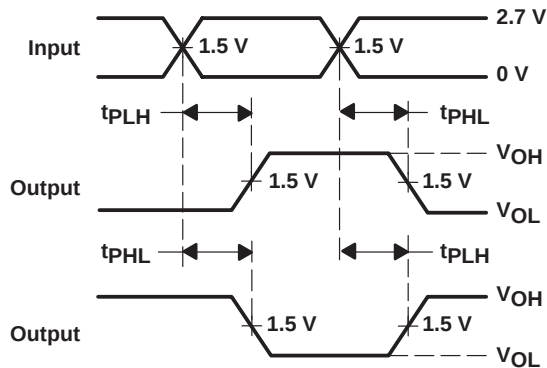
LOAD CIRCUIT



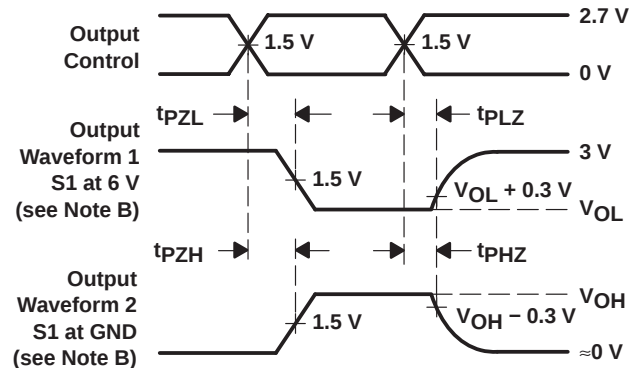
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



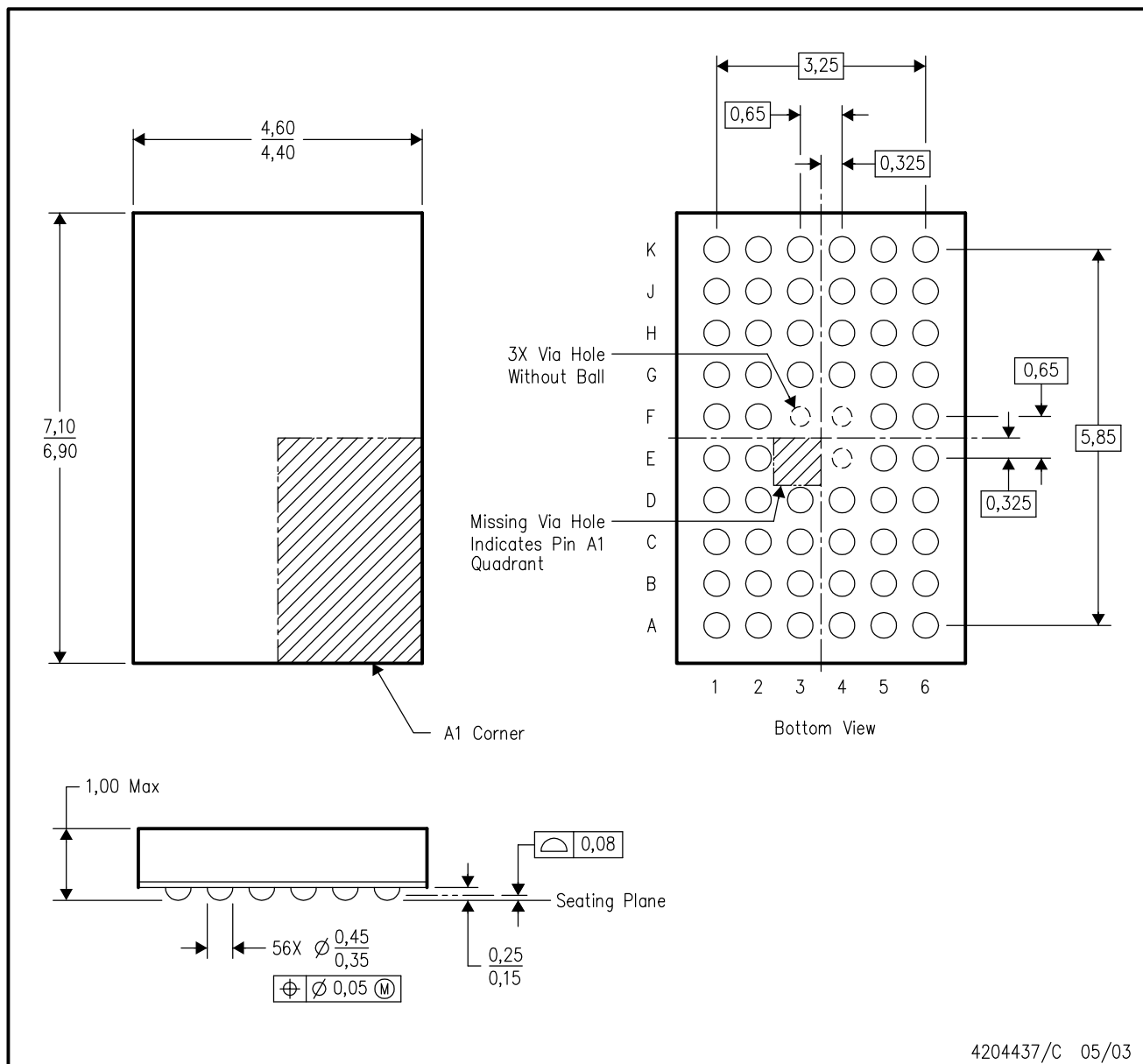
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

ZQL (R-PBGA-N56)

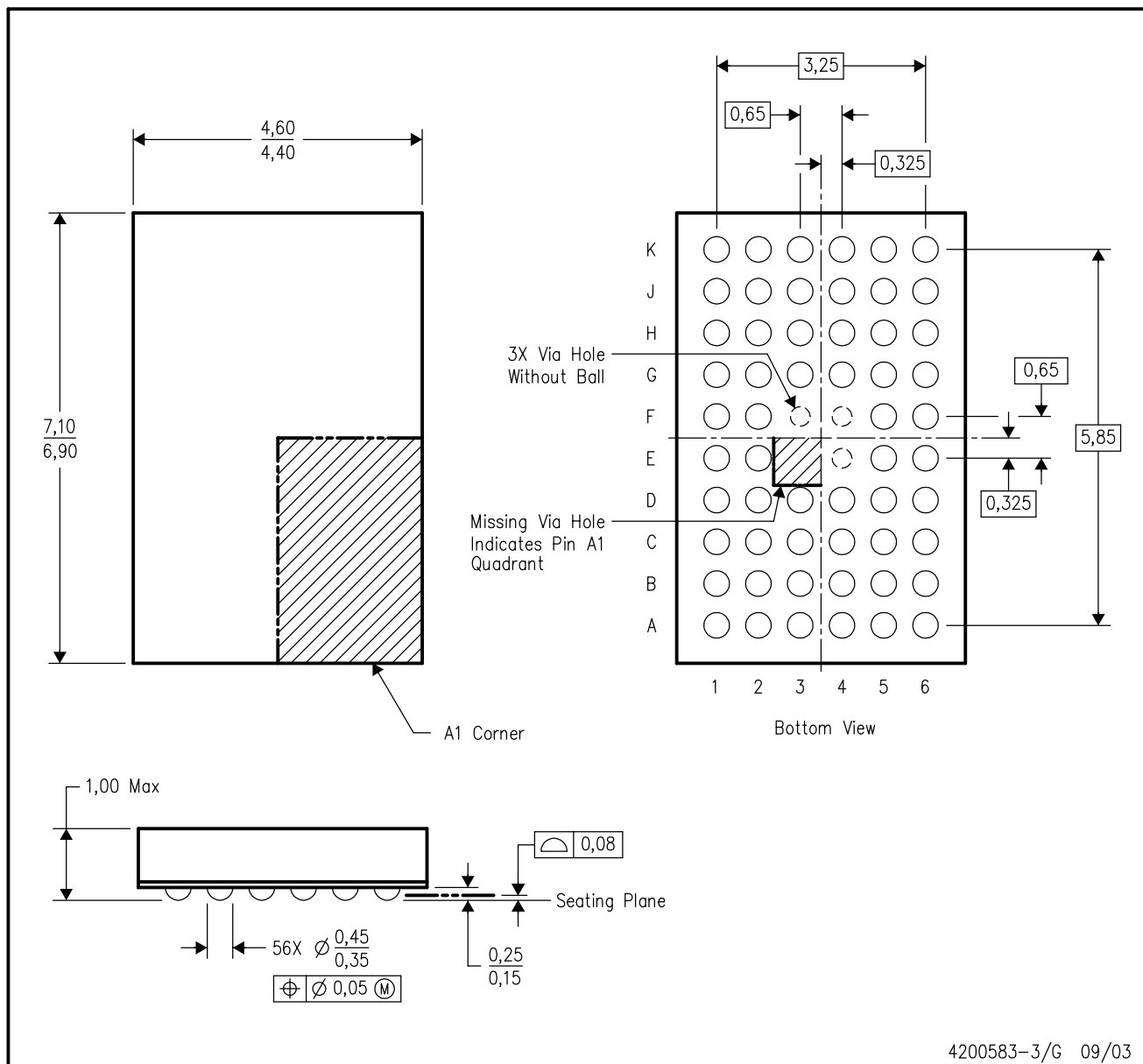
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ BGA configuration.
 - D. Falls within JEDEC MO-225 variation BA.
 - E. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

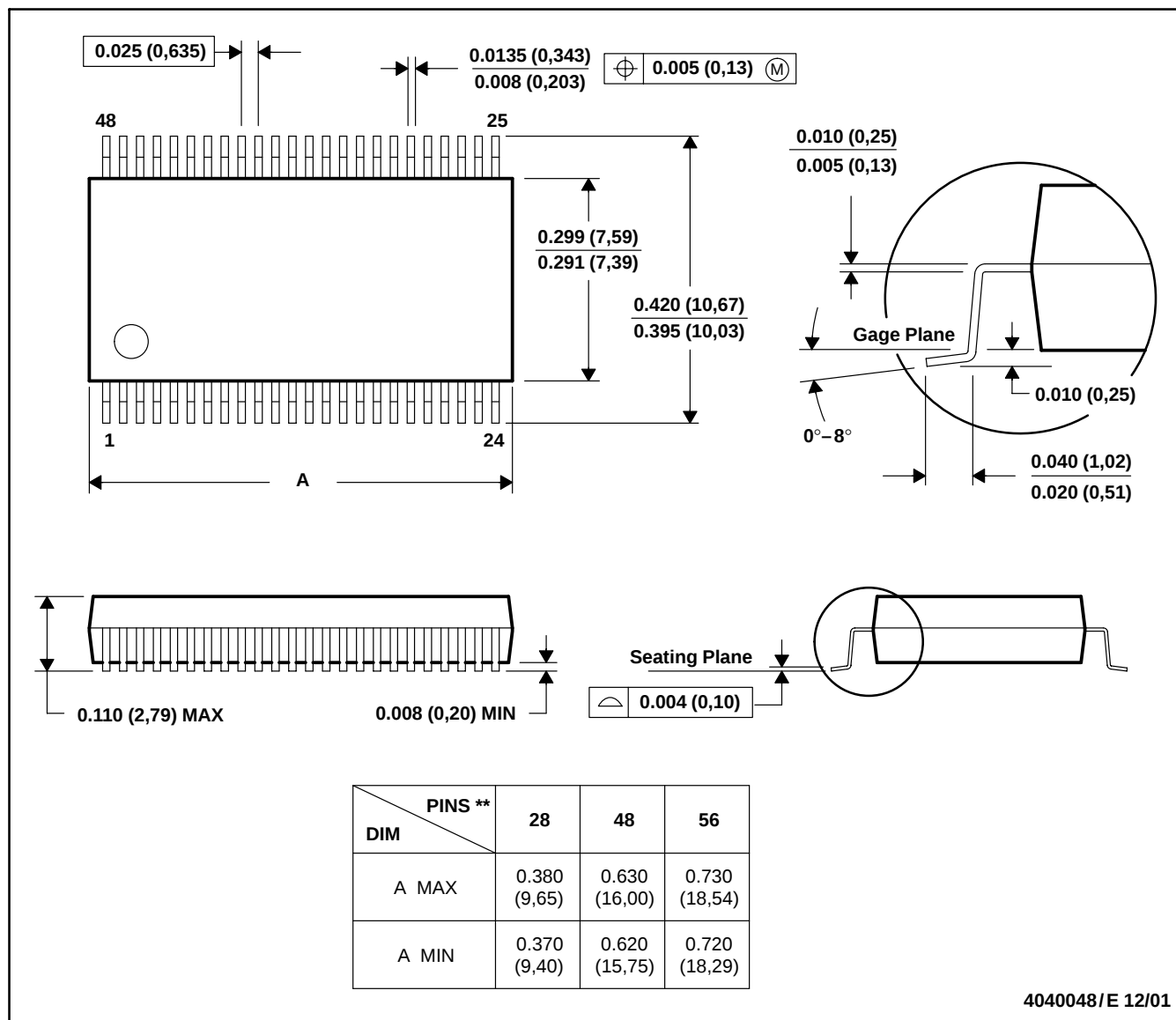


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - MicroStar Junior™ BGA configuration.
 - Falls within JEDEC MO-225 variation BA.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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