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Jameco Part Number 1047396

FEATURES

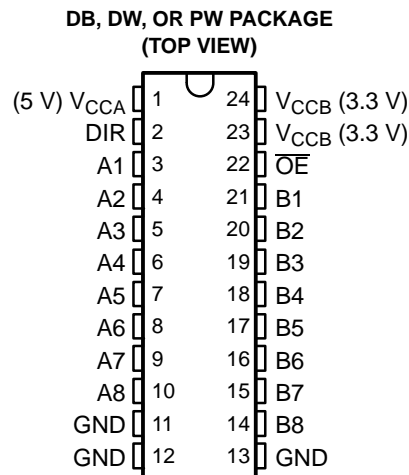
- Bidirectional Voltage Translator
- 5.5 V on A Port and 2.7 V to 3.6 V on B Port
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} , which is set at 3.3 V, and A port has V_{CCA} , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, \overline{OE}) is powered by V_{CCA} .

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.



ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW | Tube of 25 | SN74LVC4245ADW | LVC4245A |
| | | Reel of 2000 | SN74LVC4245ADWR | |
| | SSOP – DB | Reel of 2000 | SN74LVC4245ADBR | LJ245A |
| | TSSOP – PW | Tube of 60 | SN74LVC4245APW | LJ245A |
| | | Reel of 2000 | SN74LVC4245APWR | |
| | | Reel of 250 | SN74LVC4245APWT | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

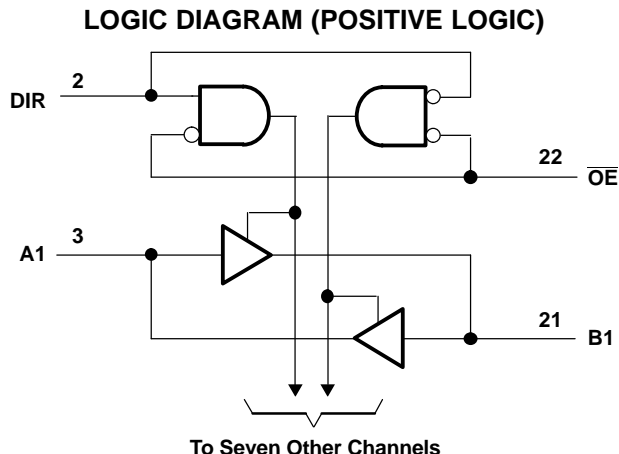
| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC4245A
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER
WITH 3-STATE OUTPUTS

SCAS375H—MARCH 1994—REVISED MARCH 2005



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$ (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|---------------|--|-----------------------|-----------------|-----------------|---|
| V_{CCA} | Supply voltage range | -0.5 | 6.5 | V | |
| V_I | Input voltage range | A port ⁽²⁾ | -0.5 | $V_{CCA} + 0.5$ | V |
| | | Control inputs | -0.5 | 6 | |
| V_O | Output voltage range | -0.5 | $V_{CCA} + 0.5$ | V | |
| I_{IK} | Input clamp current | | -50 | mA | |
| I_{OK} | Output clamp current | | -50 | mA | |
| I_O | Continuous output current | | ±50 | mA | |
| | Continuous current through each V_{CCA} or GND | | ±100 | mA | |
| θ_{JA} | Package thermal impedance ⁽³⁾ | DB package | 63 | °C/W | |
| | | DW package | 46 | | |
| | | PW package | 88 | | |
| T_{stg} | Storage temperature range | -65 | 150 | °C | |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 6 V maximum.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range for $V_{CCB} = 2.7\text{ V}$ to 3.6 V (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|------------|-----------------|------|
| V_{CCB} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range | -0.5 | $V_{CCB} + 0.5$ | V |
| V_O | Output voltage range | -0.5 | $V_{CCB} + 0.5$ | V |
| I_{IK} | Input clamp current | | -50 | mA |
| I_{OK} | Output clamp current | | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CCB} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | DB package | 63 | °C/W |
| | | DW package | 46 | |
| | | PW package | 88 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

for $V_{CCA} = 4.5\text{ V}$ to 5.5 V

| | | MIN | MAX | UNIT |
|-----------|--------------------------------|-----|-----------|------|
| V_{CCA} | Supply voltage | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_{IA} | Input voltage | 0 | V_{CCA} | V |
| V_{OA} | Output voltage | 0 | V_{CCA} | V |
| I_{OH} | High-level output current | | -24 | mA |
| I_{OL} | Low-level output current | | 24 | mA |
| T_A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾

for $V_{CCB} = 2.7\text{ V}$ to 3.6 V

| | | MIN | MAX | UNIT |
|-----------|--------------------------------|--|-----------|------|
| V_{CCB} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CCB} = 2.7\text{ V}$ to 3.6 V | 2 | V |
| V_{IL} | Low-level input voltage | $V_{CCB} = 2.7\text{ V}$ to 3.6 V | 0.8 | V |
| V_{IB} | Input voltage | 0 | V_{CCB} | V |
| V_{OB} | Output voltage | 0 | V_{CCB} | V |
| I_{OH} | High-level output current | $V_{CCB} = 2.7\text{ V}$ | -12 | mA |
| | | $V_{CCB} = 3\text{ V}$ | -24 | |
| I_{OL} | Low-level output current | $V_{CCB} = 2.7\text{ V}$ | 12 | mA |
| | | $V_{CCB} = 3\text{ V}$ | 24 | |
| T_A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC4245A

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS375H–MARCH 1994–REVISED MARCH 2005

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCA} | MIN | TYP ⁽²⁾ | MAX | UNIT |
|------------------------|----------------|--|-----------|-----|--------------------|---------|---------------|
| V_{OH} | | $I_{OH} = -100\ \mu\text{A}$ | 4.5 V | 4.3 | | | V |
| | | | 5.5 V | 5.3 | | | |
| | | $I_{OH} = -24\ \text{mA}$ | 4.5 V | 3.7 | | | |
| | | | 5.5 V | 4.7 | | | |
| V_{OL} | | $I_{OL} = 100\ \mu\text{A}$ | 4.5 V | | | 0.2 | V |
| | | | 5.5 V | | | 0.2 | |
| | | $I_{OL} = 24\ \text{mA}$ | 4.5 V | | | 0.55 | |
| | | | 5.5 V | | | 0.55 | |
| I_I | Control inputs | $V_I = V_{CCA}$ or GND | 5.5 V | | | ± 1 | μA |
| $I_{OZ}^{(3)}$ | A port | $V_O = V_{CCA}$ or GND | 5.5 V | | | ± 5 | μA |
| I_{CCA} | | $V_I = V_{CCA}$ or GND, $I_O = 0$ | 5.5 V | | | 80 | μA |
| $\Delta I_{CCA}^{(4)}$ | | One input at 3.4 V, Other inputs at V_{CCA} or GND | 5.5 V | | | 1.5 | mA |
| C_i | Control inputs | $V_I = V_{CCA}$ or GND | Open | | 5 | | pF |
| C_{io} | A port | $V_O = V_{CCA}$ or GND | 5 V | | 11 | | pF |

(1) $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$

(2) All typical values are measured at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC} .

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range for $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCB} | MIN | TYP ⁽²⁾ | MAX | UNIT |
|------------------------|--------|--|----------------|----------------|--------------------|---------|---------------|
| V_{OH} | | $I_{OH} = -100\ \mu\text{A}$ | 2.7 V to 3.6 V | $V_{CC} - 0.2$ | | | V |
| | | | 2.7 V | 2.2 | | | |
| | | $I_{OH} = -12\ \text{mA}$ | 3 V | 2.4 | | | |
| | | | 3 V | 2 | | | |
| V_{OL} | | $I_{OL} = 100\ \mu\text{A}$ | 2.7 V to 3.6 V | | | 0.2 | V |
| | | | 2.7 V | | | 0.4 | |
| | | $I_{OL} = 12\ \text{mA}$ | 3 V | | | 0.55 | |
| | | | | | | | |
| $I_{OZ}^{(3)}$ | B port | $V_O = V_{CCB}$ or GND | 3.6 V | | | ± 5 | μA |
| I_{CCB} | | $V_I = V_{CCB}$ or GND, $I_O = 0$ | 3.6 V | | | 50 | μA |
| $\Delta I_{CCB}^{(4)}$ | | One input at $V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCB} or GND | 2.7 V to 3.6 V | | | 0.5 | mA |
| C_{io} | B port | $V_O = V_{CCB}$ or GND | 3.3 V | | 11 | | pF |

(1) $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$

(2) All typical values are measured at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC} .

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1 and Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$, $V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|--|-----|------|
| | | | MIN | MAX | |
| t_{PHL} | A | B | 1 | 6.3 | ns |
| t_{PLH} | | | 1 | 6.7 | |
| t_{PHL} | B | A | 1 | 6.1 | ns |
| t_{PLH} | | | 1 | 5 | |
| t_{PZL} | \overline{OE} | A | 1 | 9 | ns |
| t_{PZH} | | | 1 | 8.1 | |
| t_{PZL} | \overline{OE} | B | 1 | 8.8 | ns |
| t_{PZH} | | | 1 | 9.8 | |
| t_{PLZ} | \overline{OE} | A | 1 | 7 | ns |
| t_{PHZ} | | | 1 | 5.8 | |
| t_{PLZ} | \overline{OE} | B | 1 | 7.7 | ns |
| t_{PHZ} | | | 1 | 7.8 | |

Operating Characteristics

$V_{CCA} = 4.5\text{ V to } 5.5\text{ V}$, $V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|------------------|------|------|
| C_{pd} | Power dissipation capacitance per transceiver | Outputs enabled | 39.5 | pF |
| | | Outputs disabled | 5 | |

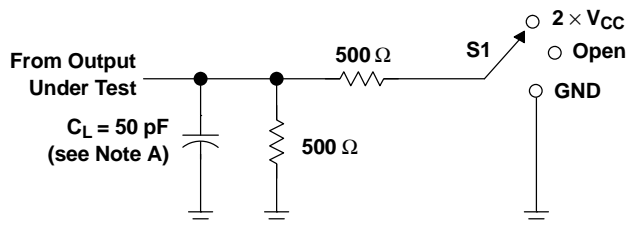
Power-Up Considerations⁽¹⁾

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

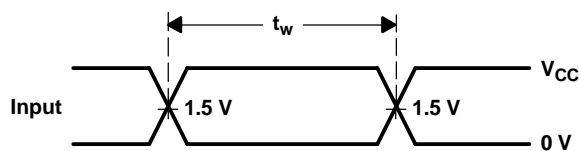
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION
A PORT

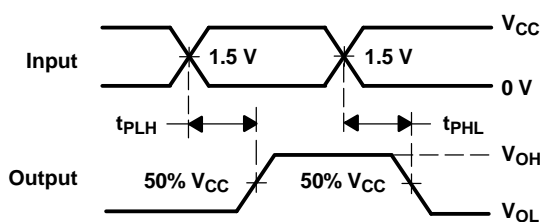


LOAD CIRCUIT

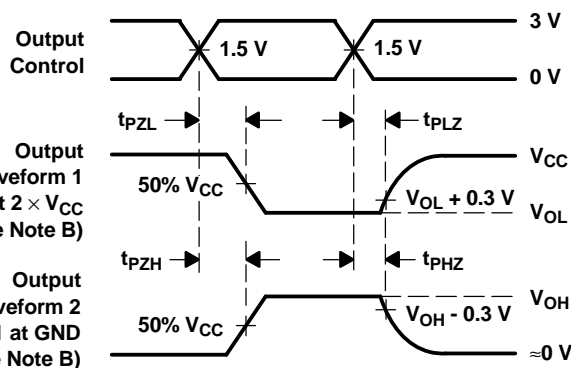
| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

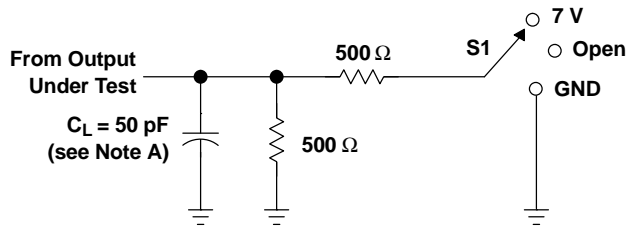


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

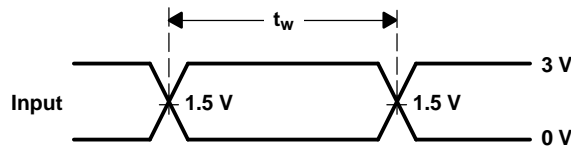
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
B PORT

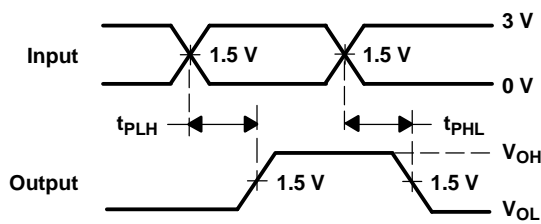


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | GND |

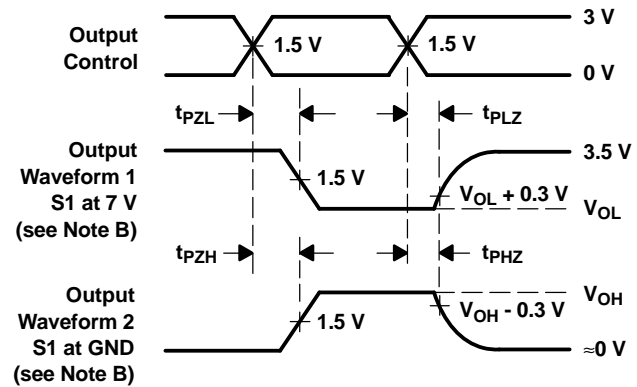
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVC4245ADBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245ADWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWE4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWT | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWTE4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC4245APWTG4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

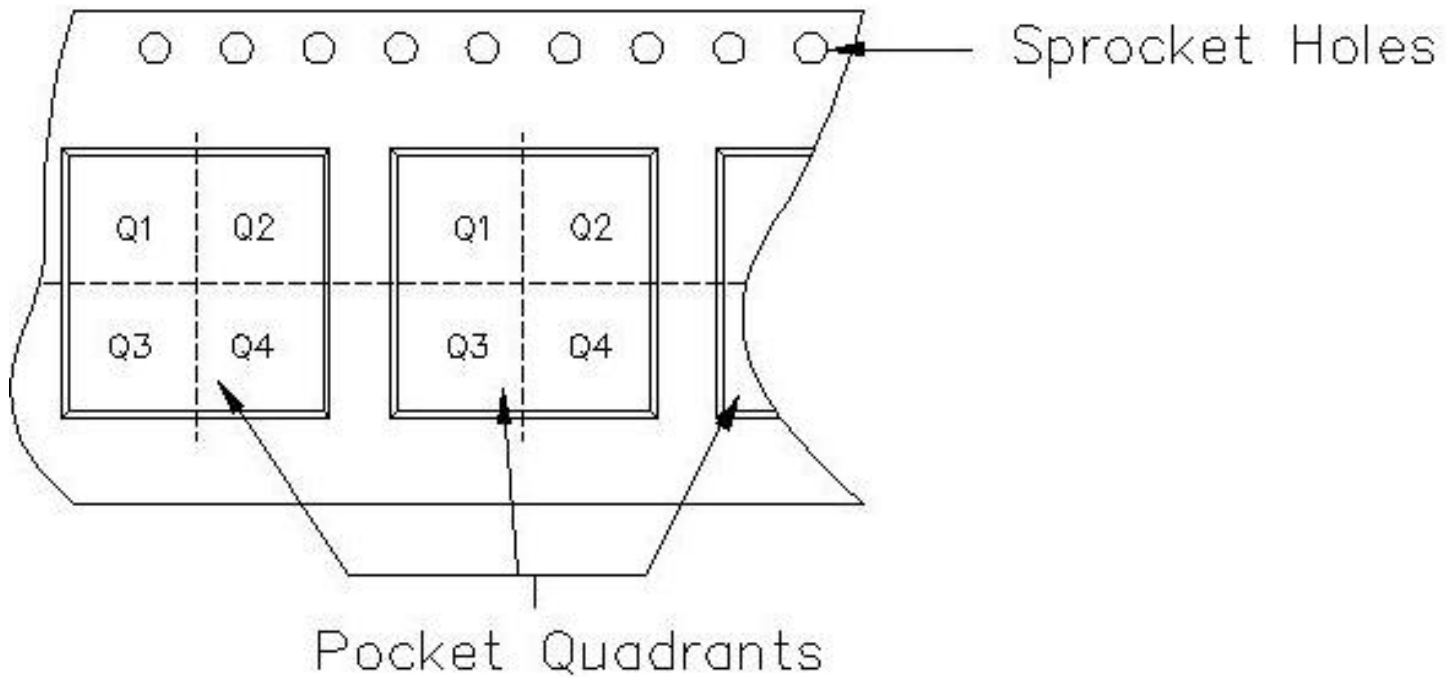
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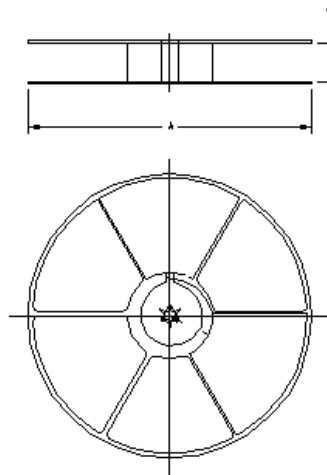
Carrier tape design is defined largely by the component length, width, and thickness.

| |
|--|
| A_o = Dimension designed to accommodate the component width. |
| B_o = Dimension designed to accommodate the component length. |
| K_o = Dimension designed to accommodate the component thickness. |
| W = Overall width of the carrier tape. |
| P = Pitch between successive cavity centers. |



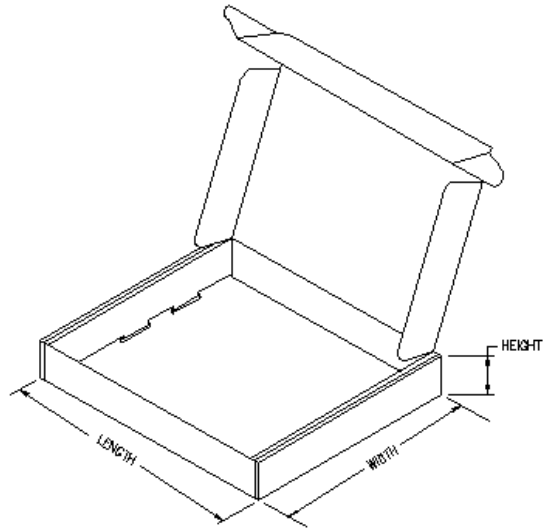
TAPE AND REEL INFORMATION

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|---------|------|------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC4245ADBR | DB | 24 | MLA | 330 | 16 | 8.2 | 8.8 | 2.5 | 12 | 16 | Q1 |
| SN74LVC4245ADWR | DW | 24 | TAI | 330 | 24 | 10.75 | 15.7 | 2.7 | 12 | 24 | Q1 |
| SN74LVC4245APWR | PW | 24 | MLA | 330 | 16 | 6.95 | 8.3 | 1.6 | 8 | 16 | Q1 |



TAPE AND REEL BOX INFORMATION

| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|-----------------|---------|------|------|-------------|------------|-------------|
| SN74LVC4245ADBR | DB | 24 | MLA | 346.0 | 346.0 | 33.0 |
| SN74LVC4245ADWR | DW | 24 | TAI | 346.0 | 346.0 | 41.0 |
| SN74LVC4245APWR | PW | 24 | MLA | 346.0 | 346.0 | 33.0 |



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

4040065 /E 12/01

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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