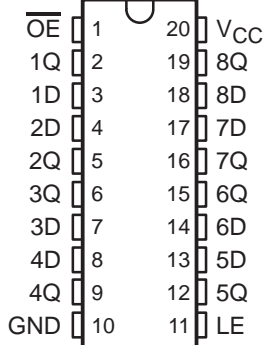


# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

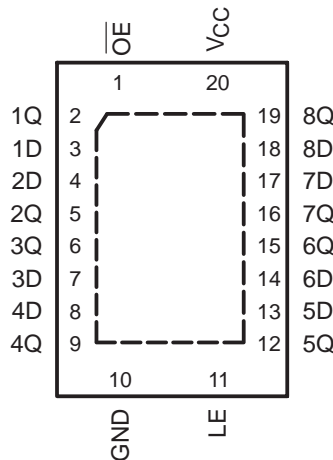
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.8 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

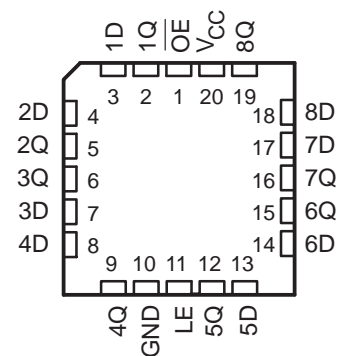
SN54LVC373A . . . J OR W PACKAGE  
SN74LVC373A . . . DB, DGV, DW, N,  
NS, OR PW PACKAGE  
(TOP VIEW)



SN74LVC373A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVC373A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

The SN54LVC373A octal transparent D-type latch is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC373A octal transparent D-type latch is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

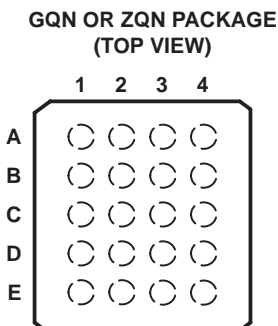
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## description/ordering information (continued)



## terminal assignments

	1	2	3	4
A	1Q	$\overline{OE}$	V <sub>CC</sub>	8Q
B	2D	7D	1D	8D
C	3Q	2Q	6Q	7Q
D	4D	5D	3D	6D
E	GND	4Q	LE	5Q

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74LVC373AN	SN74LVC373AN
	QFN – RGY	Reel of 1000	SN74LVC373ARGYR	LC373A
	SOIC – DW	Tube of 25	SN74LVC373ADW	LVC373A
		Reel of 2000	SN74LVC373ADWR	
	SOP – NS	Reel of 2000	SN74LVC373ANSR	LVC373A
	SSOP – DB	Reel of 2000	SN74LVC373ADBR	LC373A
	TSSOP – PW	Tube of 70	SN74LVC373APW	LC373A
		Reel of 2000	SN74LVC373APWR	
		Reel of 250	SN74LVC373APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC373ADGVR	LC373A
VFBGA – GQN	Reel of 1000	SN74LVC373AGQNR	LC373A	
VFBGA – ZQN (Pb-free)		SN74LVC373AZQNR		
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54LVC373AJ	SNJ54LVC373AJ
	CFP – W	Tube of 85	SNJ54LVC373AW	SNJ54LVC373AW
	LCCC – FK	Tube of 55	SNJ54LVC373AFK	SNJ54LVC373AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

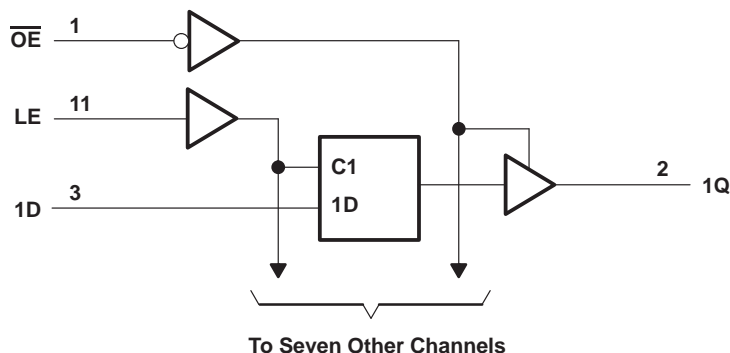
## FUNCTION TABLE (each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	70°C/W
(see Note 3): DGV package .....	92°C/W
(see Note 3): DW package .....	58°C/W
(see Note 3): GQN/ZQN package .....	78°C/W
(see Note 3): N package .....	69°C/W
(see Note 3): NS package .....	60°C/W
(see Note 3): PW package .....	83°C/W
(see Note 4): RGY package .....	37°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 5)

		SN54LVC373A		SN74LVC373A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5	1.5	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		2	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	0.8	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state		0	V <sub>CC</sub>	V
		3-state		0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4		mA
		V <sub>CC</sub> = 2.3 V		-8		
		V <sub>CC</sub> = 2.7 V		-12	-12	
		V <sub>CC</sub> = 3 V		-24	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4		mA
		V <sub>CC</sub> = 2.3 V		8		
		V <sub>CC</sub> = 2.7 V		12	12	
		V <sub>CC</sub> = 3 V		24	24	
Δt/Δv	Input transition rise or fall rate	10		10		ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC373A			SN74LVC373A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V				V <sub>CC</sub> - 0.2			V
		2.7 V to 3.6 V	V <sub>CC</sub> - 0.2						
	I <sub>OH</sub> = -4 mA	1.65 V			1.2				
	I <sub>OH</sub> = -8 mA	2.3 V			1.7				
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		2.2				
		3 V	2.4		2.4				
I <sub>OH</sub> = -24 mA	3 V	2.2		2.2					
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V			0.2				
	I <sub>OL</sub> = 4 mA	1.65 V			0.45				
	I <sub>OL</sub> = 8 mA	2.3 V			0.7				
	I <sub>OL</sub> = 12 mA	2.7 V		0.4	0.4				
	I <sub>OL</sub> = 24 mA	3 V		0.55	0.55				
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5		±5	μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0					±10	μA	
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V			±15		±10	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	I <sub>O</sub> = 0		10		10	μA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V‡				10		10		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500		500	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4	12		4	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5.5	12		5.5	pF	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		SN54LVC373A				UNIT
		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	2		2		ns
t <sub>h</sub>	Hold time, data after LE↓	2		2		ns



# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN74LVC373A								UNIT
		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	†		†		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE↓	†		†		2		2		ns
t <sub>h</sub>	Hold time, data after LE↓	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC373A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	8.5		1	7.5	ns
	LE		9.5		1	8.5	
t <sub>en</sub>	$\overline{OE}$	Q	8.7		1	7.7	ns
t <sub>dis</sub>	$\overline{OE}$	Q	8		0.5	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC373A								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	†	†	†	†	7.8		1.5	6.8	ns
	LE		†	†	†	†	8.2		2	7.6	
t <sub>en</sub>	$\overline{OE}$	Q	†	†	†	†	8.7		1.5	7.7	ns
t <sub>dis</sub>	$\overline{OE}$	Q	†	†	†	†	7.6		1.5	7	ns
t <sub>sk(o)</sub>										1	ns

† This information was not available at the time of publication.

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	†	†	46	pF
	per latch	Outputs disabled			3	

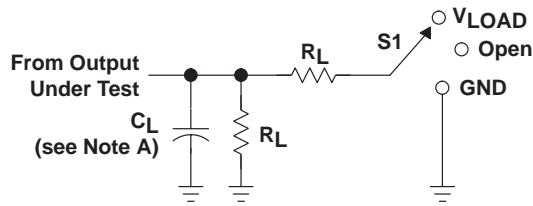
† This information was not available at the time of publication.



# SN54LVC373A, SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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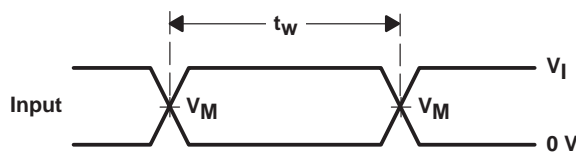
## PARAMETER MEASUREMENT INFORMATION



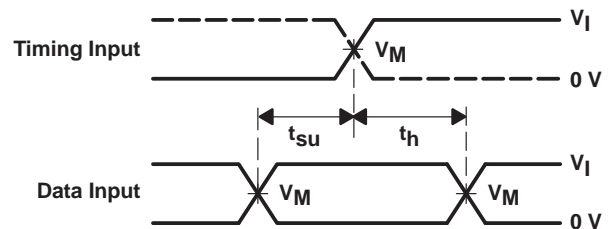
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

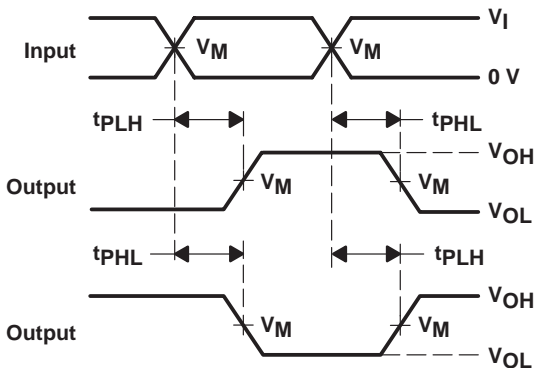
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



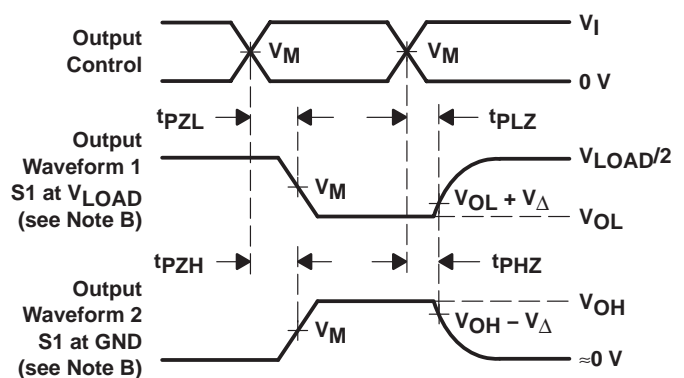
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

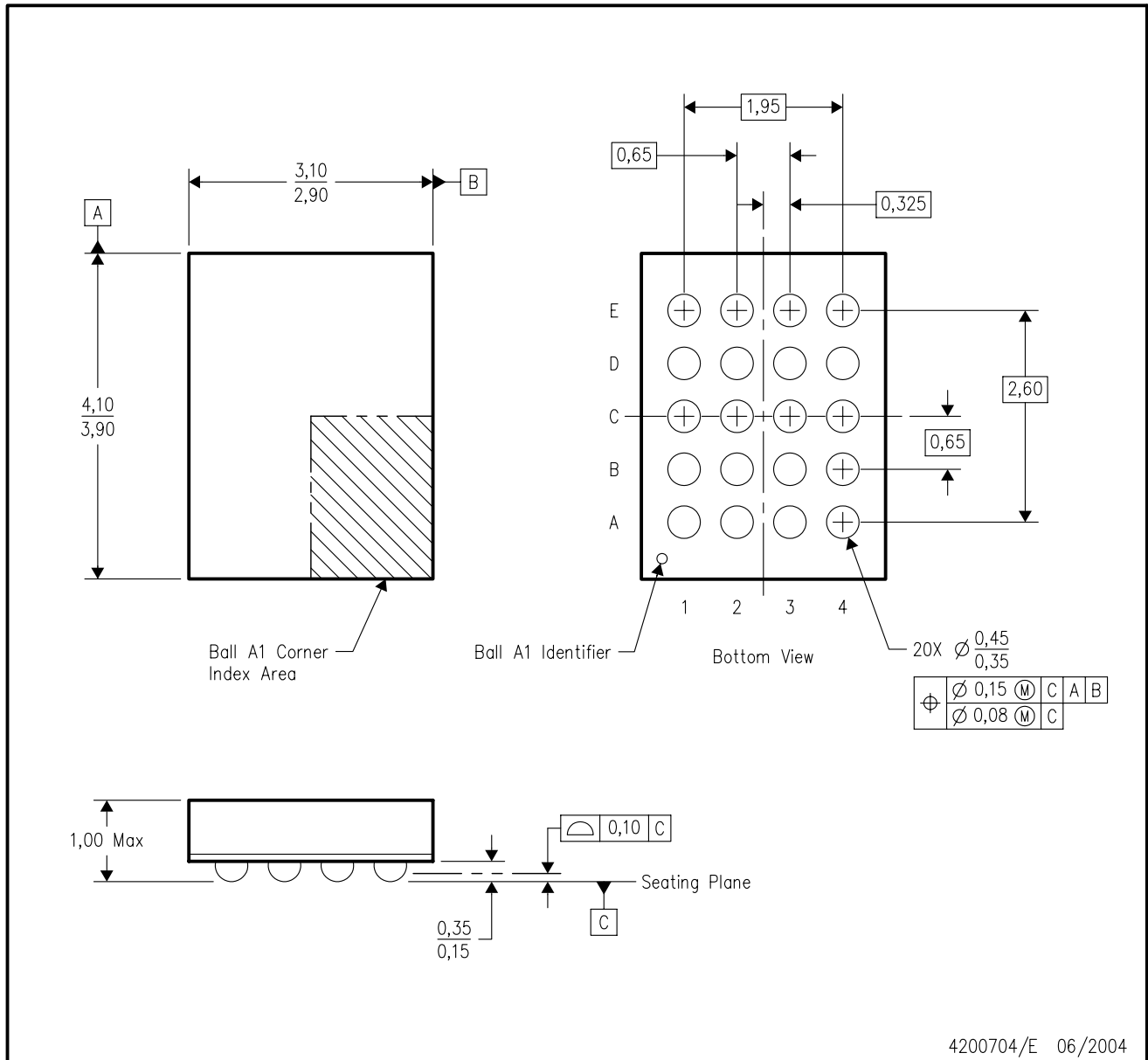
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

GQN (R-PBGA-N20)

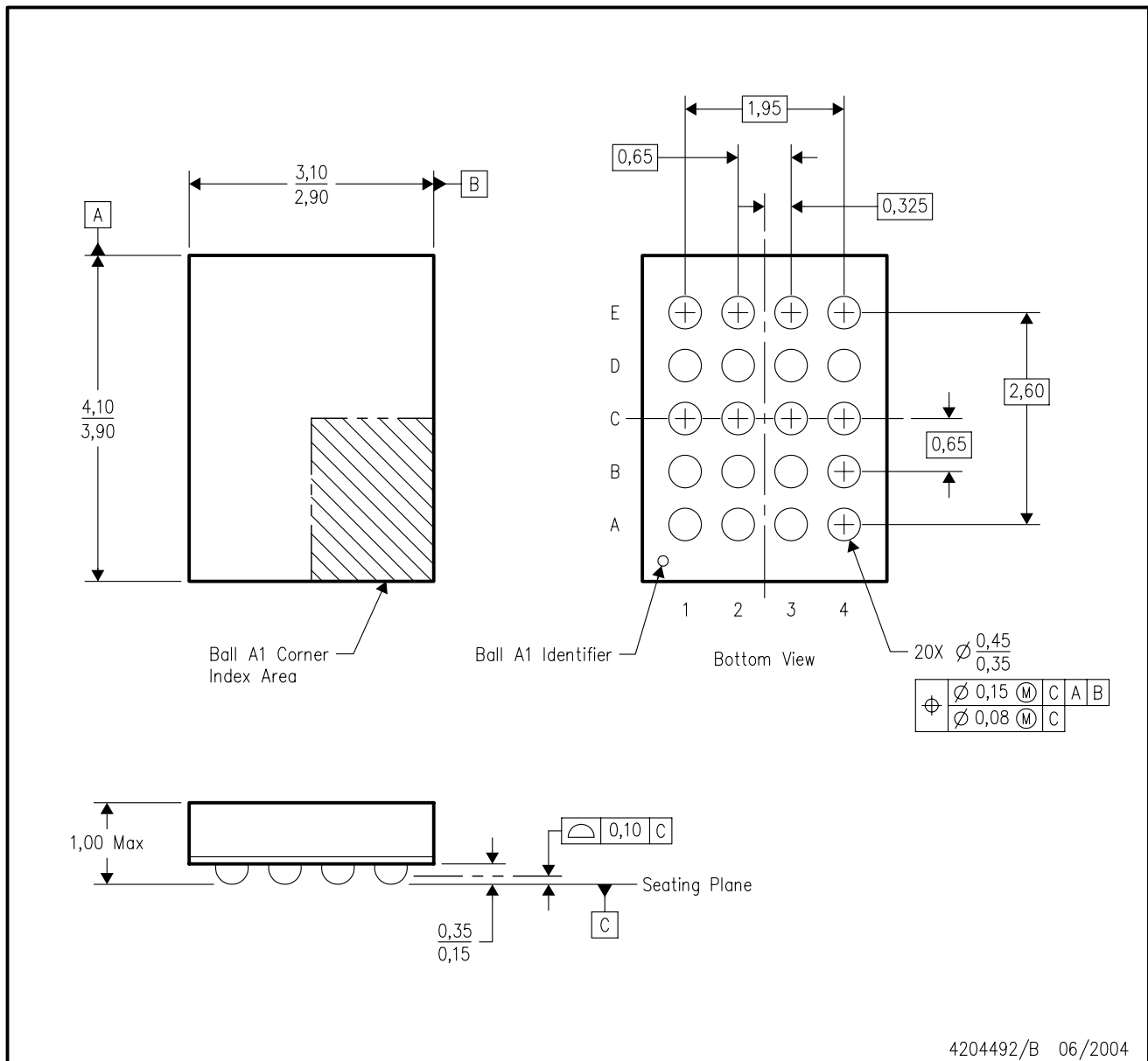
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

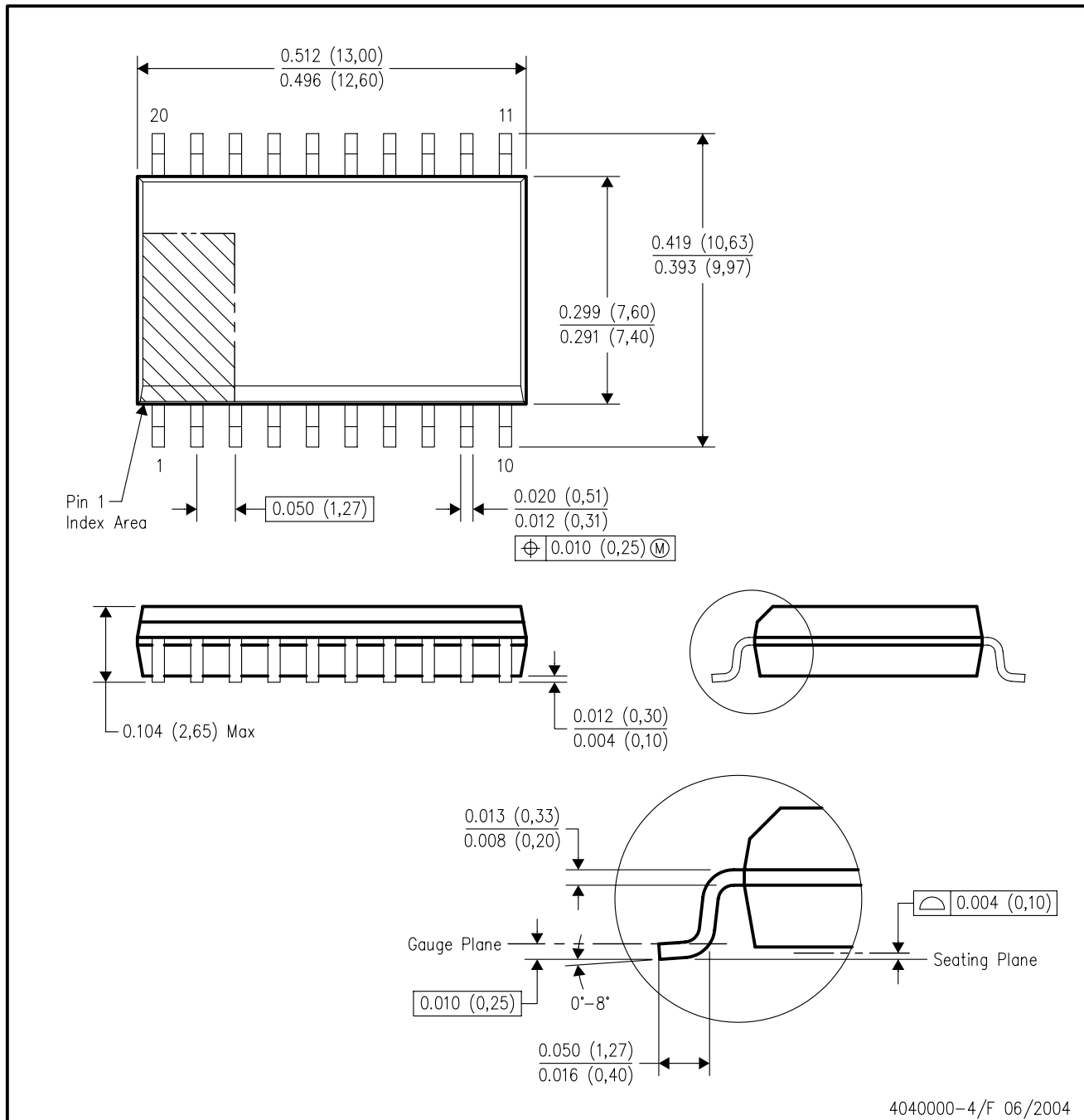


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

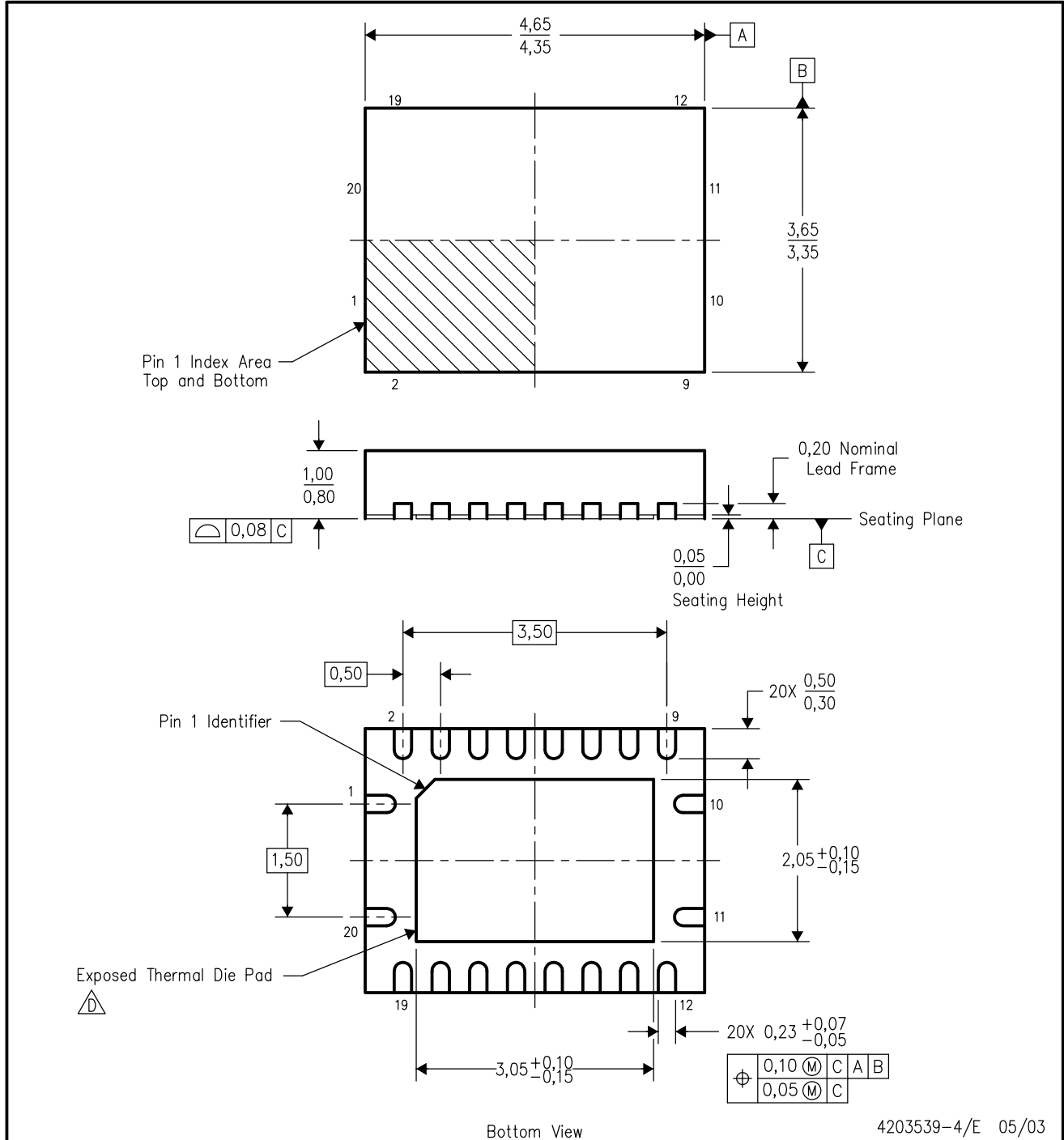
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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