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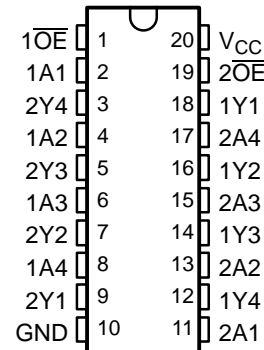
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Jameco Part Number 1045454

FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.5 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down-Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This octal buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC240A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device is organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC240ADW	LVC240A
		Reel of 2000	SN74LVC240ADWR	
	SOP – NS	Reel of 2000	SN74LVC240ANSR	LVC240A
	SSOP – DB	Reel of 2000	SN74LVC240ADBR	LC240A
	TSSOP – PW	Tube of 70	SN74LVC240APW	LC240A
		Reel of 2000	SN74LVC240APWR	
		Reel of 250	SN74LVC240APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC240ADGVR	LC240A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

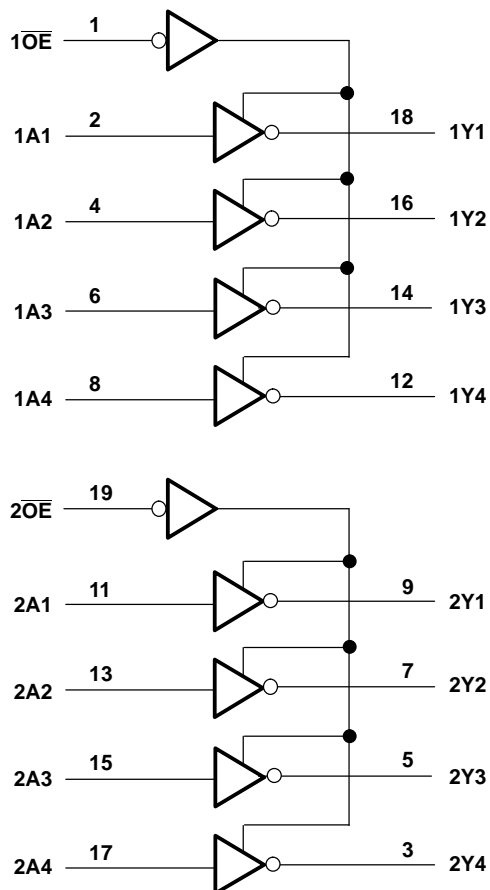


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FUNCTION TABLE
(EACH 4-BIT BUFFER)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	L
L	L	H
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	6.5	V
V _I	Input voltage range ⁽²⁾	–0.5	6.5	V
V _O	Voltage range, applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O	Voltage range, applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	–50	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DB package	70	°C/W
		DGV package	92	
		DW package	58	
		NS package	60	
		PW package	83	
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 2.7 V to 3.6 V		0.8	
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4	mA
		V _{CC} = 2.3 V		–8	
		V _{CC} = 2.7 V		–12	
		V _{CC} = 3 V		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			6	ns/V
T _A	Operating free-air temperature	–40	85	°C	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC240A

OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS293K–JANUARY 1993–REVISED FEBRUARY 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -8 mA	2.3 V	1.7			
	I _{OH} = -12 mA	2.7 V	2.2			
		3 V	2.4			
I _{OH} = -24 mA	3 V	2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 0 to 5.5 V	3.6 V			±5	μA
I _{off}	V _I or V _O = 5.5 V	0			±10	μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND	3.6 V	I _O = 0		10	μA
	3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾				10	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V		4		pF
C _o	V _O = V _{CC} or GND	3.3 V		5.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	(1)	(1)	(1)	(1)	7.5		1.3	6.5	ns
t _{en}	\overline{OE}	Y	(1)	(1)	(1)	(1)	9		1.1	8	ns
t _{dis}	\overline{OE}	Y	(1)	(1)	(1)	(1)	8		1.4	7	ns
t _{sk(o)}									1		ns

(1) This information was not available at the time of publication.

Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	Outputs enabled	(1)	(1)	32	pF
	Outputs disabled	(1)	(1)	3	

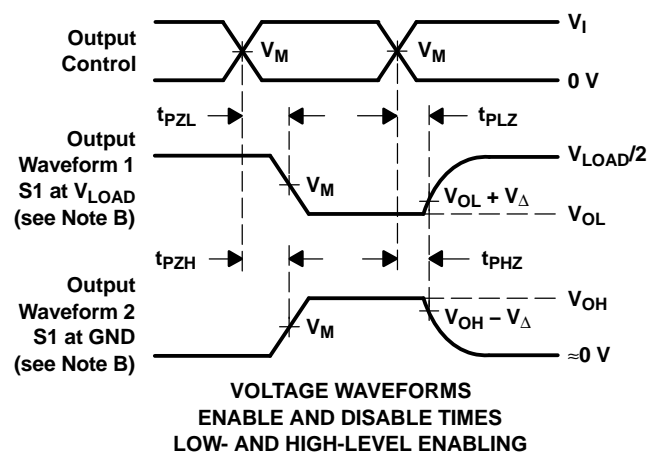
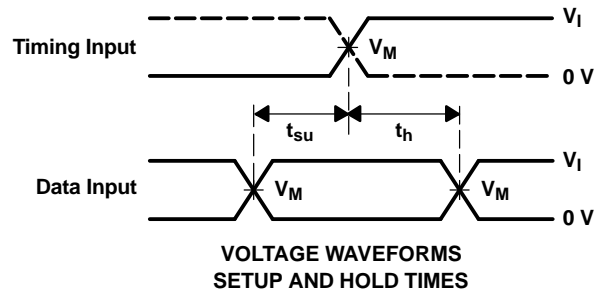
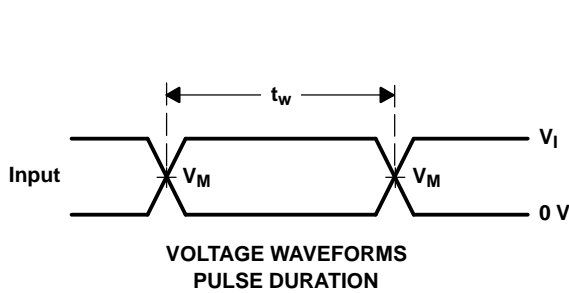
(1) This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC240ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LVC240ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74LVC240APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC240APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
no Sb/Br)								

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

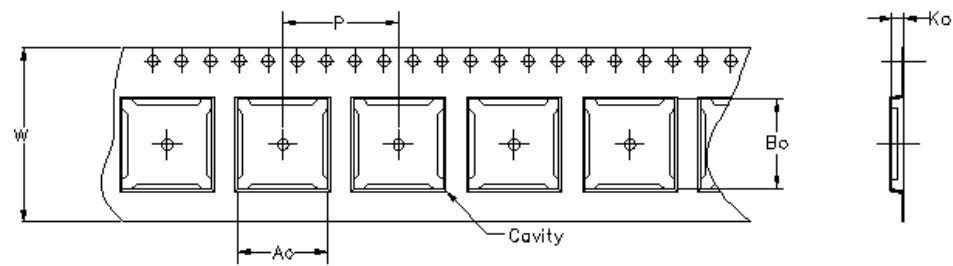
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

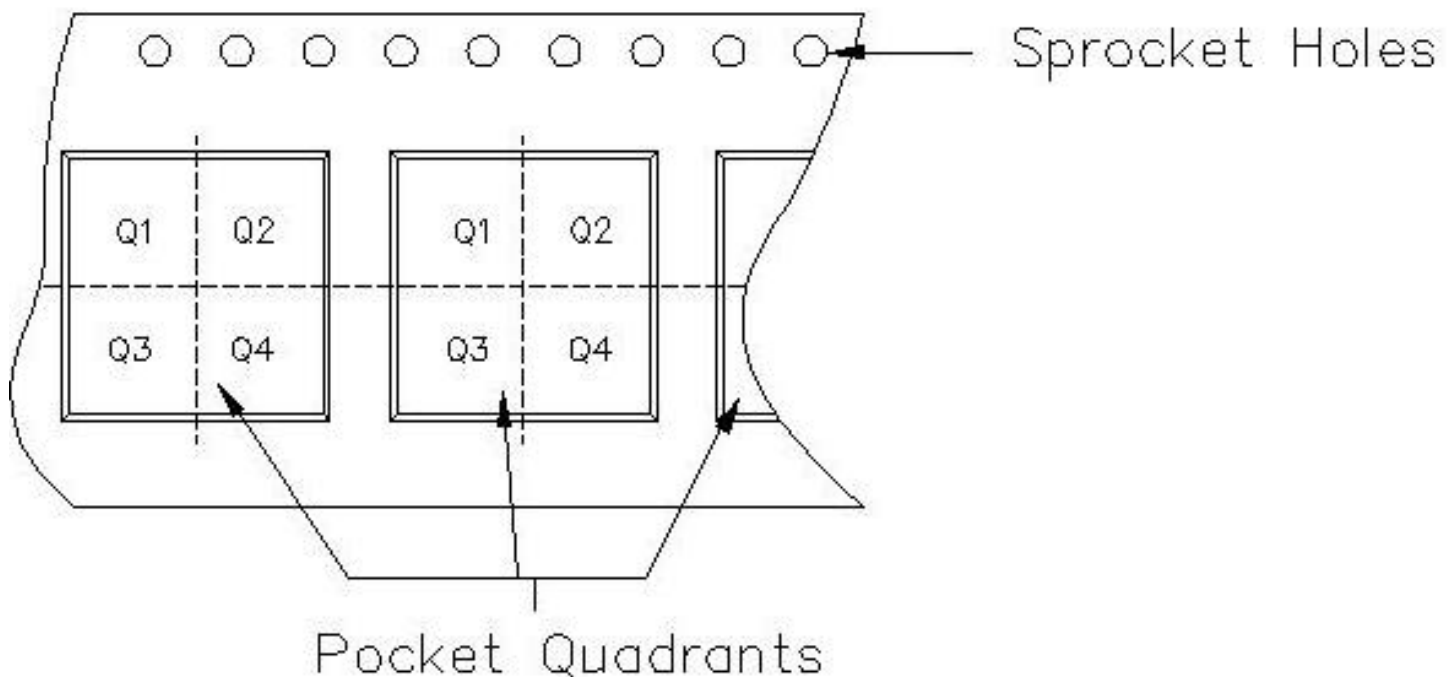
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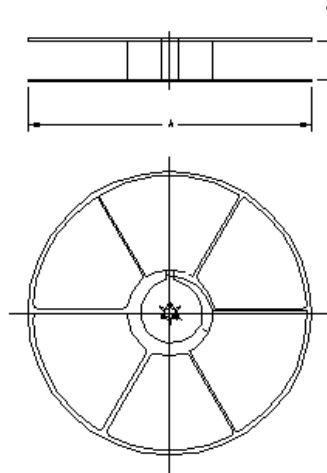
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



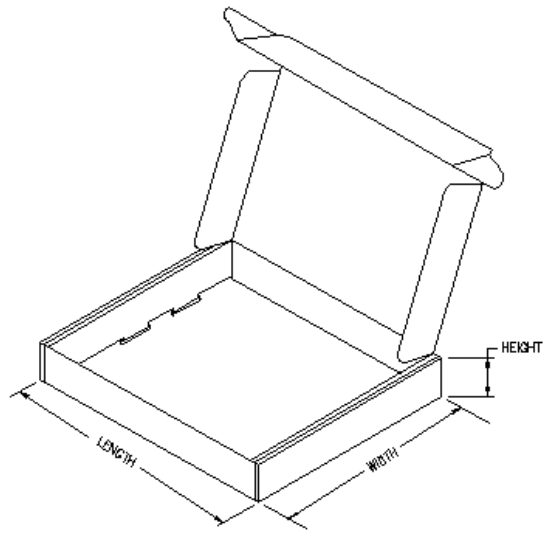
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC240ADBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74LVC240ADGVR	DGV	20	MLA	330	12	7.0	5.6	1.6	8	12	Q1
SN74LVC240ADWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74LVC240ANSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74LVC240APWR	PW	20	MLA	330	16	6.95	7.1	1.6	8	16	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LVC240ADBR	DB	20	MLA	346.0	346.0	33.0
SN74LVC240ADGVR	DGV	20	MLA	346.0	346.0	29.0
SN74LVC240ADWR	DW	20	MLA	333.2	333.2	31.75
SN74LVC240ANSR	NS	20	MLA	333.2	333.2	31.75
SN74LVC240APWR	PW	20	MLA	346.0	346.0	33.0



DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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