

Distributed by:

JAMECO[®]
ELECTRONICS

www.Jameco.com ♦ 1-800-831-4242

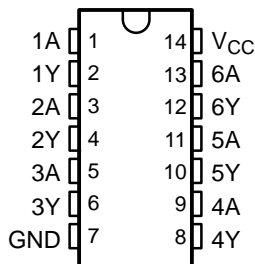
The content and copyrights of the attached
material are the property of its owner.

Jameco Part Number 818110

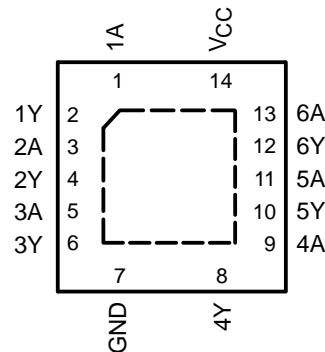
FEATURES

- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

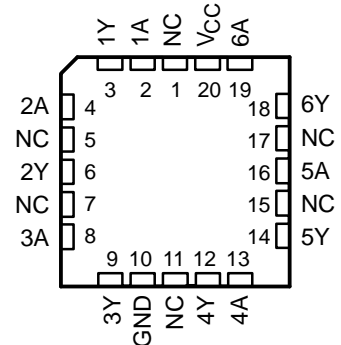
SN54LVC14A ... J OR W PACKAGE
SN74LVC14A ... D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC14A ... RGY PACKAGE
(TOP VIEW)



SN54LVC14A ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC14ARGYR	LC14A
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC14AD	LVC14A
		Reel of 2500	SN74LVC14ADR	
		Reel of 250	SN74LVC14ADT	
	SOP – NS	Reel of 2000	SN74LVC14ANSR	LVC14A
	SSOP – DB	Reel of 2000	SN74LVC14ADBR	LC14A
	TSSOP – PW	Tube of 90	SN74LVC14APW	LC14A
		Reel of 2000	SN74LVC14APWR	
Reel of 250		SN74LVC14APWT		
TVSOP – DGV	Reel of 2000	SN74LVC14ADGVR	LC14A	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC14AJ	SNJ54LVC14AJ
	CFP – W	Tube of 150	SNJ54LVC14AW	SNJ54LVC14AW
	LCCC – FK	Tube of 55	SNJ54LVC14AFK	SNJ54LVC14AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

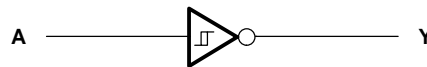
The devices contain six independent inverters and perform the Boolean function $Y = \bar{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

**FUNCTION TABLE
 (EACH INVERTER)**

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



Absolute Maximum Ratings ⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50 mA
I_{OK}	Output clamp current	$V_O < 0$		-50 mA
I_O	Continuous output current			±50 mA
	Continuous current through V_{CC} or GND			±100 mA
θ_{JA}	Package thermal impedance	D package ⁽⁴⁾		86
		DB package ⁽⁴⁾		96
		DGV package ⁽⁴⁾		127
		NS package ⁽⁴⁾		76
		PW package ⁽⁴⁾		113
		RGY package ⁽⁵⁾		47
T_{stg}	Storage temperature range	-65	150	°C
P_{tot}	Power dissipation	$T_A = -40^\circ\text{C}$ to 125°C ⁽⁶⁾⁽⁷⁾		500 mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Oonditions⁽¹⁾

		SN54LVC14A		UNIT	
		–55 TO 125°C			
		MIN	MAX		
V _{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 2.7 V		–12	mA
		V _{CC} = 3 V		–24	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾

		SN74LVC14A						UNIT	
		T _A = 25°C		–40 TO 85°C		–40 TO 125°C			
		MIN	MAX	MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4		–4		–4	mA
		V _{CC} = 2.3 V		–8		–8		–8	
		V _{CC} = 2.7 V		–12		–12		–12	
		V _{CC} = 3 V		–24		–24		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4		4		4	mA
		V _{CC} = 2.3 V		8		8		8	
		V _{CC} = 2.7 V		12		12		12	
		V _{CC} = 3 V		24		24		24	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

SCAS285X–MARCH 1993–REVISED JULY 2005

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC14A			UNIT
			–55 TO 125°C			
			MIN	TYP	MAX	
V _{T+} Positive-going threshold		2.7 V	0.8	2	V	
		3 V	0.9	2		
		3.6 V	1.1	2		
V _{T–} Negative-going threshold		2.7 V	0.4	1.4	V	
		3 V	0.6	1.5		
		3.6 V	0.8	1.7		
ΔV _T Hysteresis (V _{T+} – V _{T–})		2.7 V	0.3	1.1	V	
		3 V	0.3	1.2		
		3.6 V	0.3	1.2		
V _{OH}	I _{OH} = –100 μA	2.7 V to 3.6 V	V _{CC} – 0.2		V	
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
I _{OH} = –24 mA	3 V	2.2				
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V	0.2		V	
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		μA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		μA	
C _i	V _I = V _{CC} or GND	3.3 V	5 ⁽¹⁾		pF	

(1) T_A = 25°C

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC14A						UNIT	
			T _A = 25°C			–40 TO 85°C		–40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{T+} Positive-going threshold		1.65 V	0.4	1.3	0.4	1.3	0.4	1.3	V	
		1.95 V	0.6	1.5	0.6	1.5	0.6	1.5		
		2.3 V	0.8	1.7	0.8	1.7	0.8	1.7		
		2.5 V	0.8	1.7	0.8	1.7	0.8	1.7		
		2.7 V	0.8	2	0.8	2	0.8	2		
		3 V	0.9	2	0.9	2	0.9	2		
		3.6 V	1.1	2	1.1	2	1.1	2		
V _{T–} Negative-going threshold		1.65 V	0.15	0.85	0.15	0.85	0.15	0.85	V	
		1.95 V	0.25	0.95	0.25	0.95	0.25	0.95		
		2.3 V	0.4	1.2	0.4	1.2	0.4	1.2		
		2.5 V	0.4	1.2	0.4	1.2	0.4	1.2		
		2.7 V	0.4	1.4	0.4	1.4	0.4	1.4		
		3 V	0.6	1.5	0.6	1.5	0.6	1.5		
		3.6 V	0.8	1.7	0.8	1.7	0.8	1.7		
ΔV _T Hysteresis (V _{T+} – V _{T–})		1.65 V	0.1	1.15	0.1	1.15	0.1	1.15	V	
		1.95 V	0.15	1.25	0.15	1.25	0.15	1.25		
		2.3 V	0.25	1.3	0.25	1.3	0.25	1.3		
		2.5 V	0.25	1.3	0.25	1.3	0.25	1.3		
		2.7 V	0.3	1.1	0.3	1.1	0.3	1.1		
		3 V	0.3	1.2	0.3	1.2	0.3	1.2		
		3.6 V	0.3	1.2	0.3	1.2	0.3	1.2		
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} – 0.2		V _{CC} – 0.2		V _{CC} – 0.3		V	
	I _{OH} = –4 mA	1.65 V	1.29		1.2		1.05			
	I _{OH} = –8 mA	2.3 V	1.9		1.7		1.65			
	I _{OH} = –12 mA	2.7 V	2.2		2.2		2.05			
		3 V	2.4		2.4		2.25			
	I _{OH} = –24 mA	3 V	2.3		2.2		2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.1		0.2		0.3		V	
	I _{OL} = 4 mA	1.65 V	0.24		0.45		0.6			
	I _{OL} = 8 mA	2.3 V	0.3		0.7		0.75			
	I _{OL} = 12 mA	2.7 V	0.4		0.4		0.6			
	I _{OL} = 24 mA	3 V	0.55		0.55		0.8			
I _I	V _I = 5.5 V or GND	3.6 V	±1		±5		±20		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	1		10		40		μA	
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		500		5000		μA	
C _i	V _I = V _{CC} or GND	3.3 V	5						pF	

SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

SCAS285X—MARCH 1993—REVISED JULY 2005



Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54LVC14A		UNIT
				-55 TO 125°C		
				MIN	MAX	
t_{pd}	A	Y	2.7 V	7.5		ns
			$3.3 V \pm 0.3 V$	1	6.4	

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

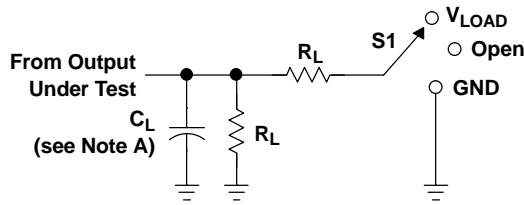
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74LVC14A						UNIT	
				$T_A = 25^\circ C$			-40 TO 85°C		-40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t_{pd}	A	Y	$1.8 V \pm 0.15 V$	1	5	10.5	1	11	1	13	ns
			$2.5 V \pm 0.2 V$	1	3.4	7.3	1	7.8	1	10	
			2.7 V	1	3.6	7.3	1	7.5	1	9.5	
			$3.3 V \pm 0.3 V$	1	3.2	6.2	1	6.4	1	8	
$t_{sk(o)}$			$3.3 V \pm 0.3 V$			1		1		1.5	ns

Operating Characteristics

$T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	f = 10 MHz	1.8 V	11	pF
			2.5 V	12	
			3.3 V	15	

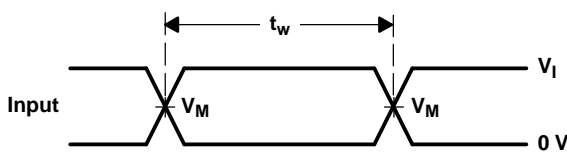
Parameter Measurement Information



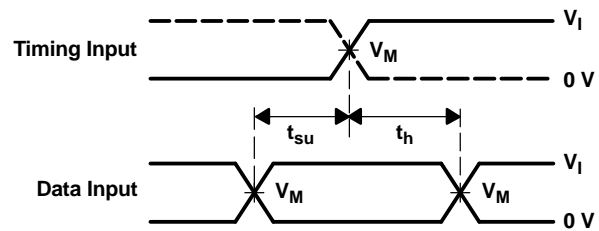
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

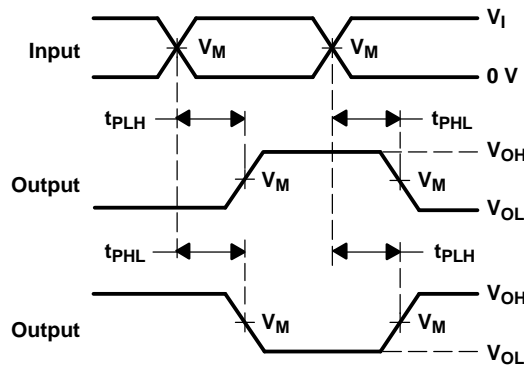
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



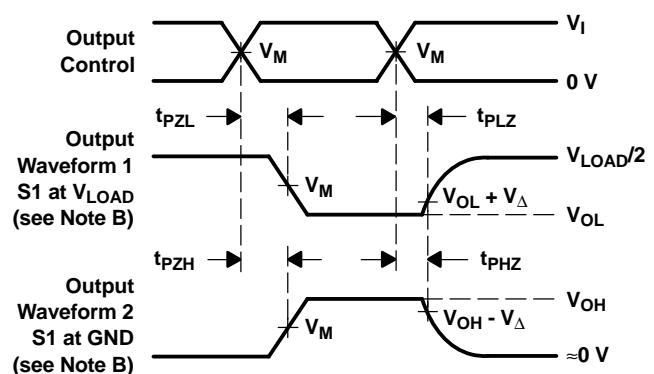
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9761501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9761501QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9761501QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9761501V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9761501VCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9761501VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN74LVC14AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LVC14ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC14APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC14APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC14ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LVC14ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SNJ54LVC14AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LVC14AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LVC14AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

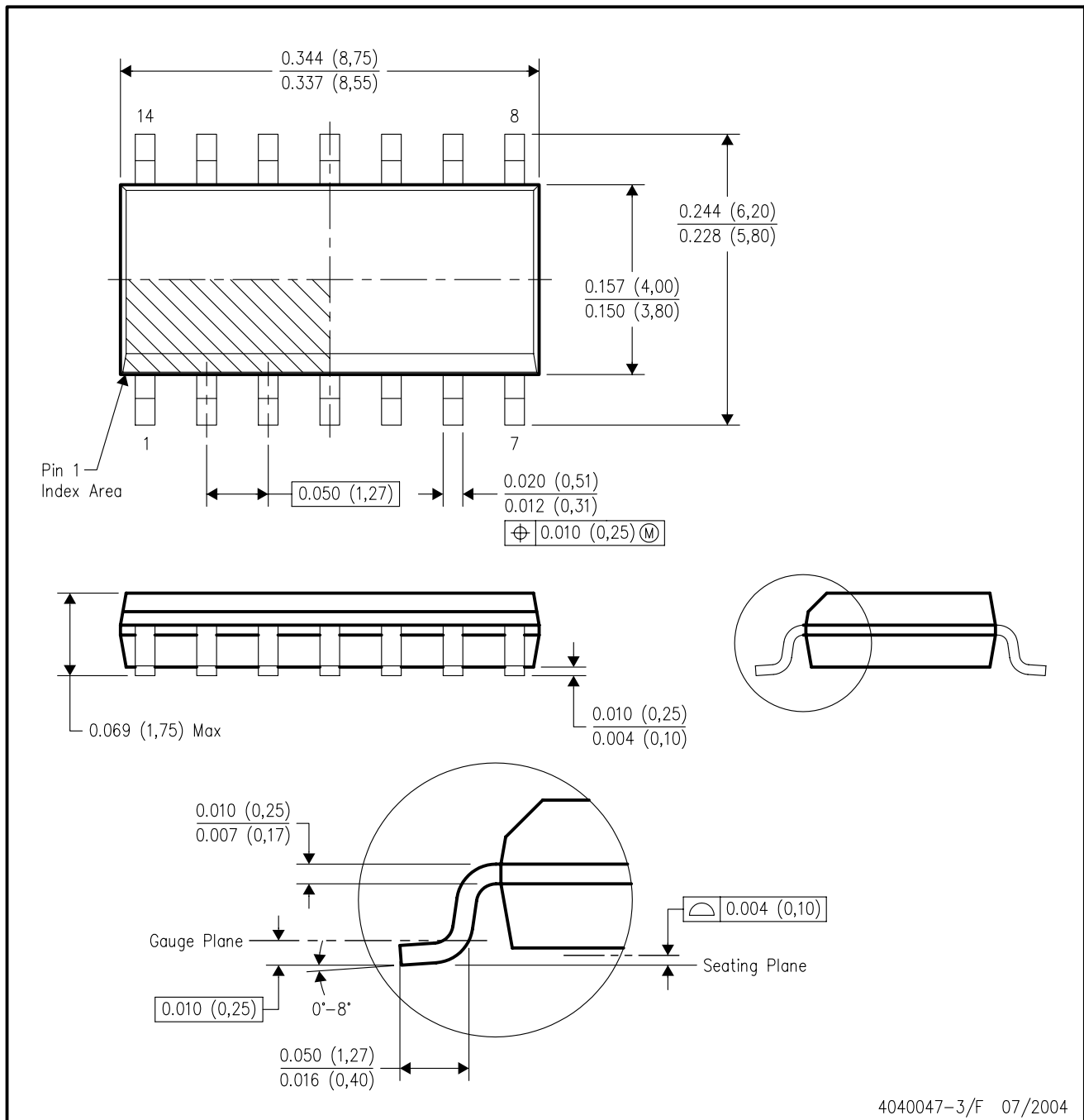


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

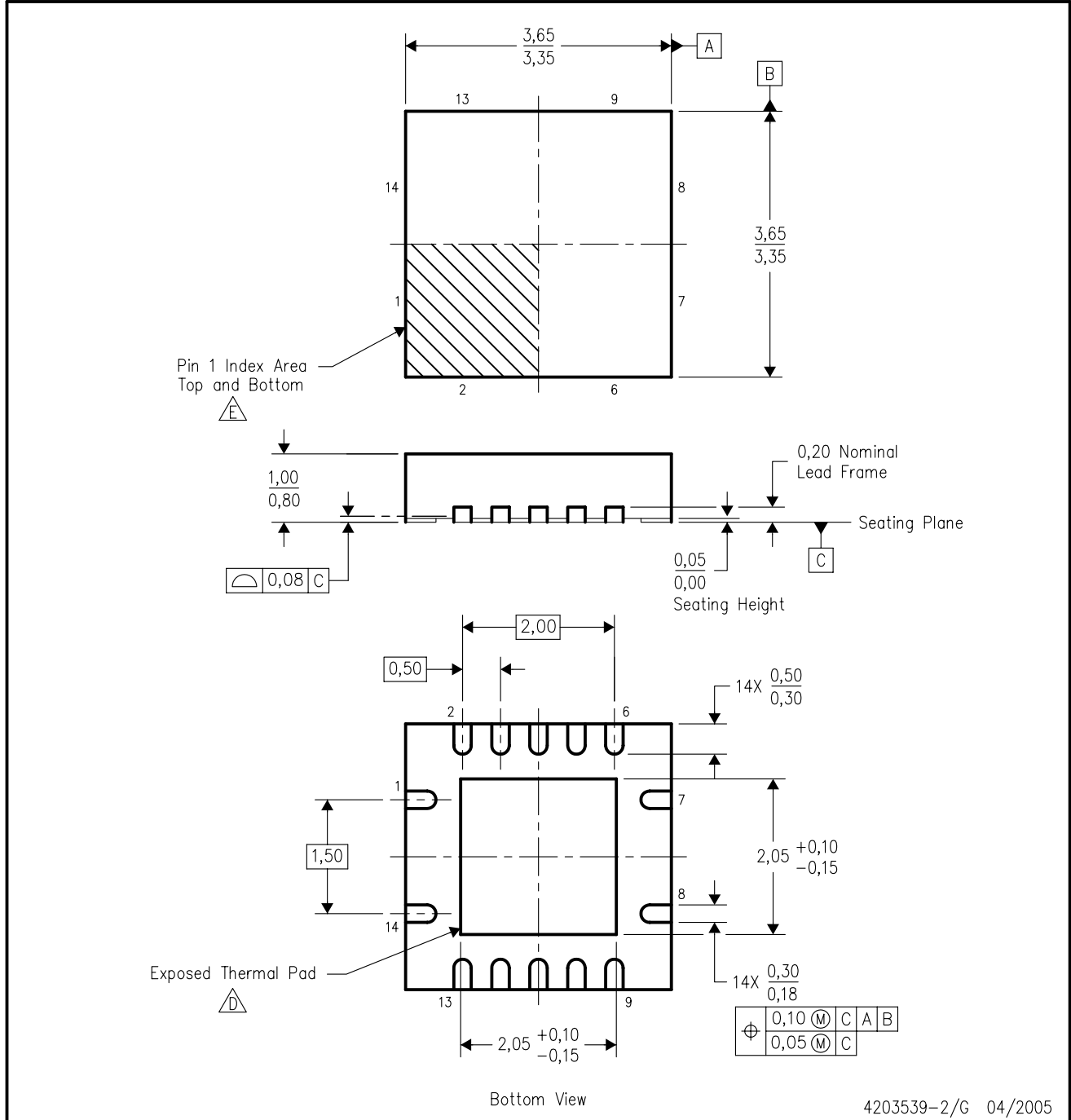
PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

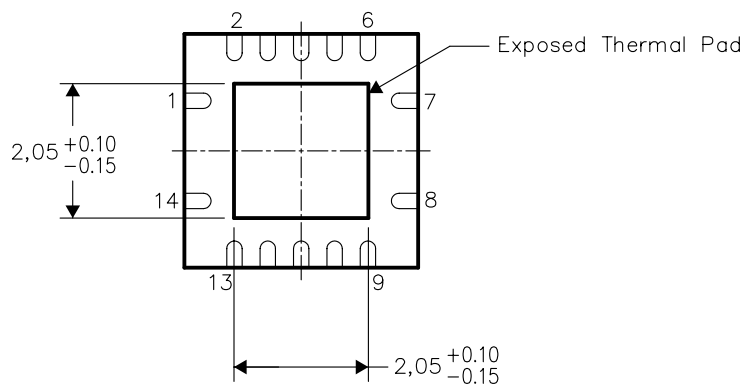
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

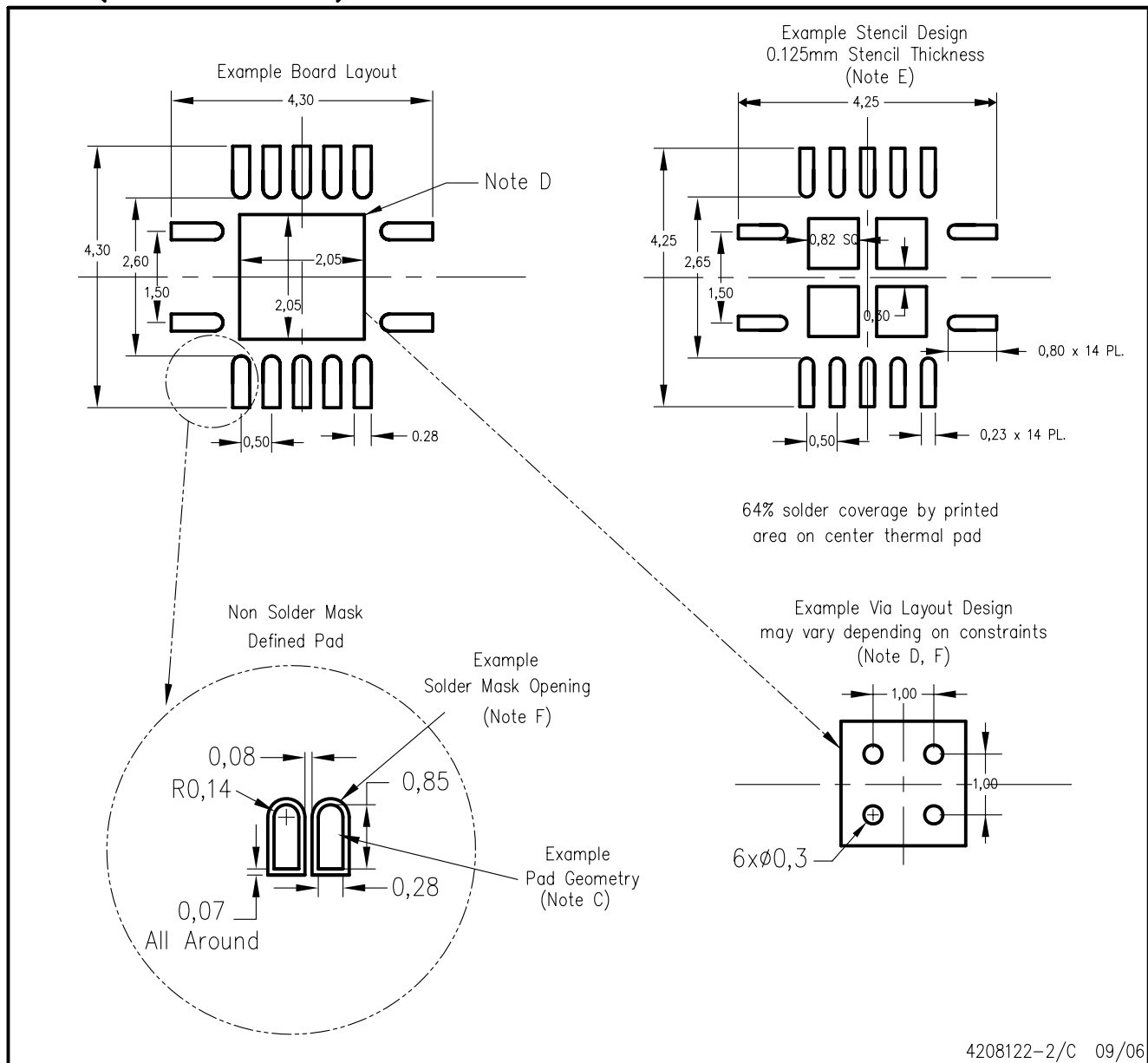


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N14)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265