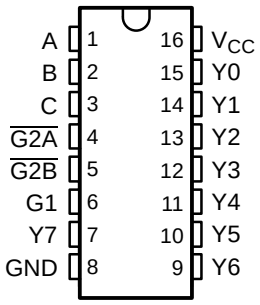
SN54LVC138A, SN74LVC138A
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCAS291S–MARCH 1993–REVISED APRIL 2005

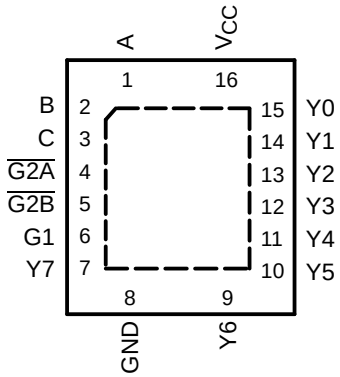
FEATURES

- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.8 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

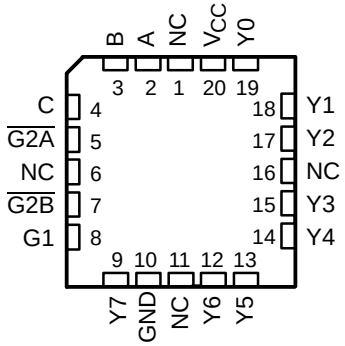
SN54LVC138A . . . J OR W PACKAGE
SN74LVC138A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC138A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC138A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC138A 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC138A 3-line to 8-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC138ARGYR	LC138A
	SOIC – D	Tube of 40	SN74LVC138AD	LVC138A
		Reel of 2500	SN74LVC138ADR	
		Reel of 250	SN74LVC138ADT	
	SOP – NS	Reel of 2000	SN74LVC138ANSR	LVC138A
	SSOP – DB	Reel of 2000	SN74LVC138ADBR	LC138A
	TSSOP – PW	Tube of 90	SN74LVC138APW	LC138A
		Reel of 2000	SN74LVC138APWR	
		Reel of 250	SN74LVC138APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC138ADGVR	LC138A
	VFBGA – GQN	Reel of 1000	SN74LVC138AGQNR	LC138A
	VFBGA – ZQN (Pb-free)		SN74LVC138AZQNR	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC138AJ	SNJ54LVC138AJ
	CFP – W	Tube of 150	SNJ54LVC138AW	SNJ54LVC138AW
	LCCC – FK	Tube of 55	SNJ54LVC138AFK	SNJ54LVC138AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

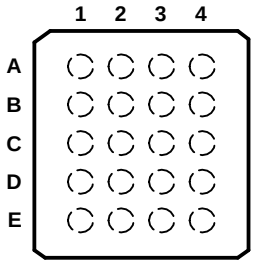
DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 'LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

GQN OR ZQN PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

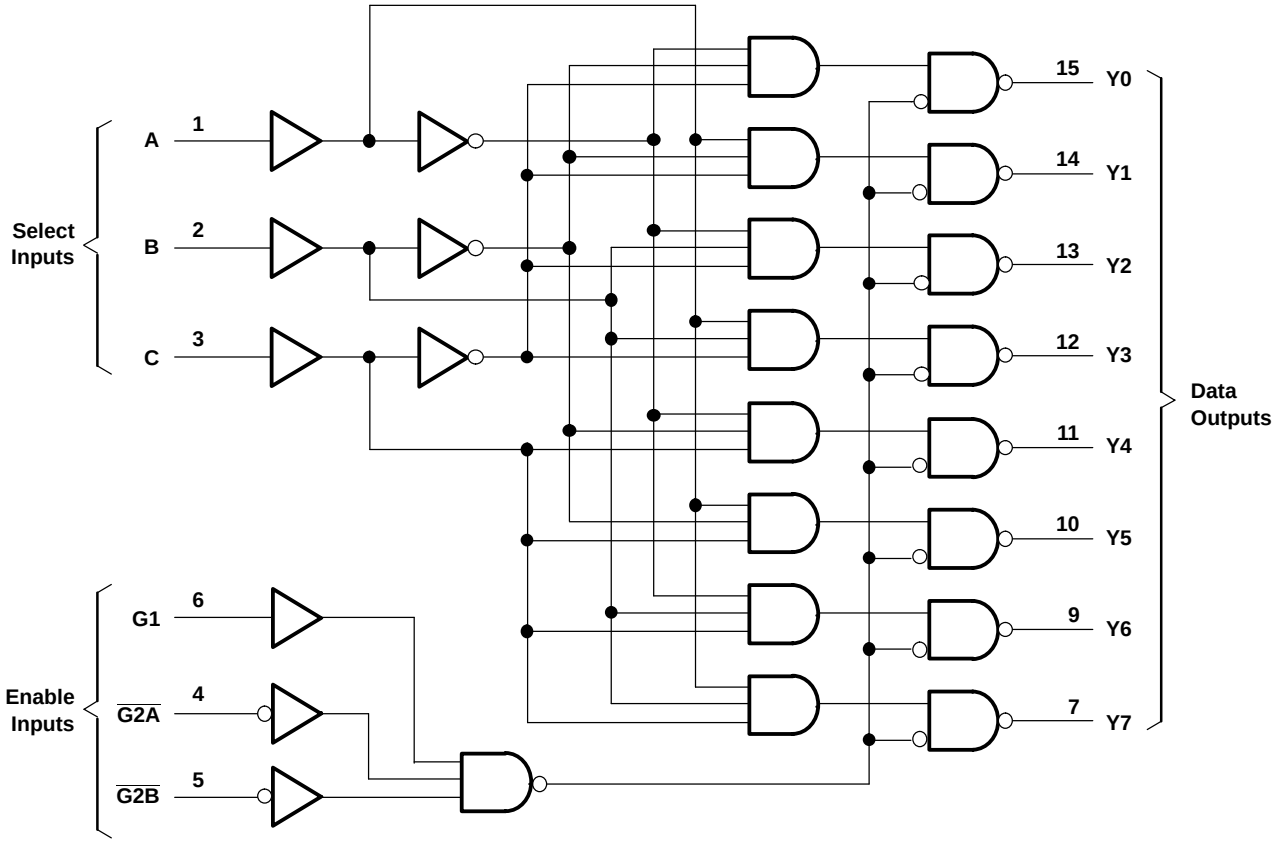
	1	2	3	4
A	B	A	V_{CC}	Y0
B	C	NC(1)	NC(1)	Y1
C	$\overline{G2B}$	$\overline{G2A}$	Y3	Y2
D	G1	NC(1)	NC(1)	Y4
E	GND	Y7	Y6	Y5

(1) NC - No internal connection

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	**$\overline{G2A}$**	**$\overline{G2B}$**	**C**	**B**	**A**	**Y0**	**Y1**	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Output voltage range[2][3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	D package[4]		73	°C/W
		DB package[4]		82	
		DGV package[4]		120	
		GQN/ZQN package[4]		78	
		NS package[4]		64	
		PW package[4]		108	
		RGY package[5]		39	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions(1)

			SN54LVC138A		SN74LVC138A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V				–4	mA
		V_{CC} = 2.3 V				–8	
		V_{CC} = 2.7 V		–12		–12	
		V_{CC} = 3 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10	ns/V
T_A	Operating free-air temperature		–55	125	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVC138A			SN74LVC138A			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{OH}	I_{OH} = –100 μA	1.65 V to 3.6 V				V_{CC} – 0.2			V
		2.7 V to 3.6 V	V_{CC} – 0.2						
	I_{OH} = –4 mA	1.65 V				1.2			
	I_{OH} = –8 mA	2.3 V				1.7			
	I_{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I_{OH} = –24 mA	3 V	2.2			2.2			
V_{OL}	I_{OL} = 100 μA	1.65 V to 3.6 V						0.2	V
		2.7 V to 3.6 V			0.2				
	I_{OL} = 4 mA	1.65 V						0.45	
	I_{OL} = 8 mA	2.3 V						0.7	
	I_{OL} = 12 mA	2.7 V			0.4			0.4	
	I_{OL} = 24 mA	3 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	3.6 V			±5			±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			10			10	μA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		5			5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC138A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A or B or C	Y		7.9	1	6.7	ns
	$\overline{G2A}$ or $\overline{G2B}$			7.4	1	6.5	
	G1			6.4	1	5.8	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

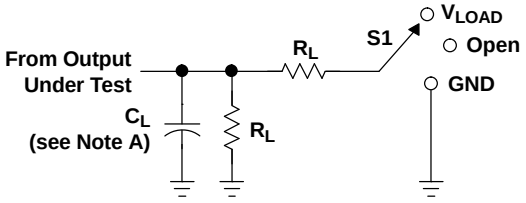
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC138A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B or C	Y	1	22	1	9.9	1	7.9	1	6.7	ns
	$\overline{G2A}$ or $\overline{G2B}$		1	21	1	9.4	1	7.4	1	6.5	
	G1		1	20.3	1	8.4	1	6.4	1	5.8	
$t_{sk(o)}$										1	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	25	26	27	pF

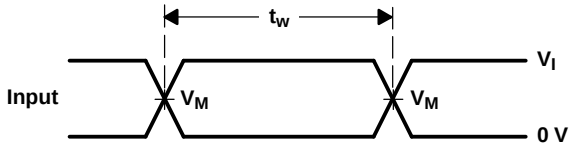
PARAMETER MEASUREMENT INFORMATION



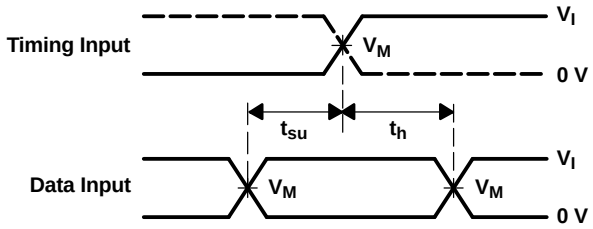
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

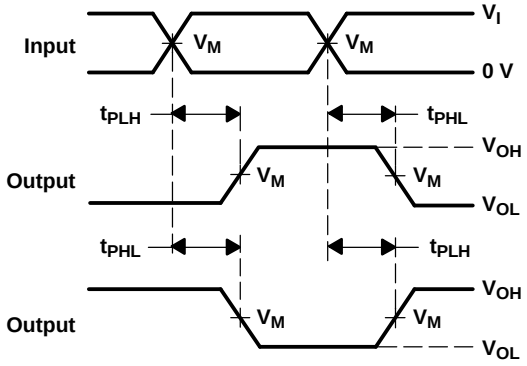
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



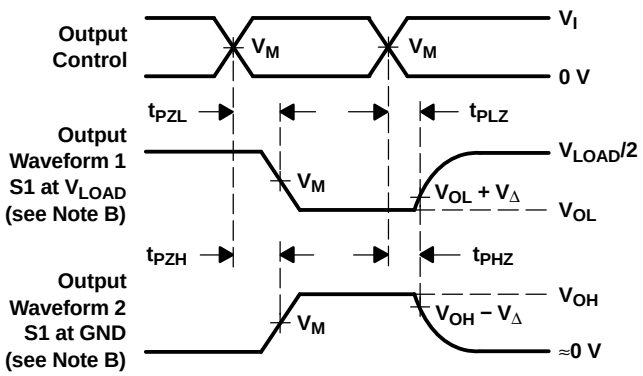
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9752601Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9752601QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9752601QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN74LVC138AD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138ADBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
SN74LVC138ADBR	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138ADBRE4	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC138ADGVR	ACTIVE	TVSOP	DGV	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC138ADR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC138ADT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138ADTE4	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138AGQNR	ACTIVE	VFBGA	GQN	20	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVC138ANSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138ANSRE4	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVC138APW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138APWE4	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC138APWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
SN74LVC138APWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138APWRE4	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC138APWT	ACTIVE	TSSOP	PW	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVC138APWTE4	ACTIVE	TSSOP	PW	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LVC138APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC138ARGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LVC138AZQNR	ACTIVE	VFBGA	ZQN	20	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SNJ54LVC138AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LVC138AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LVC138AW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

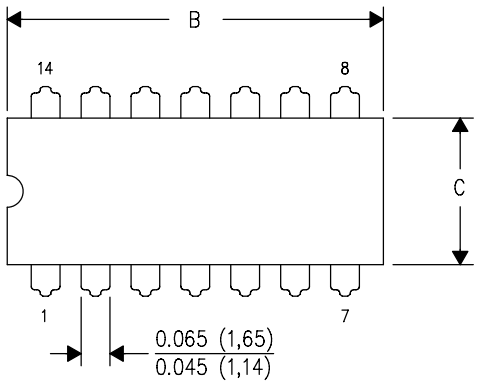
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

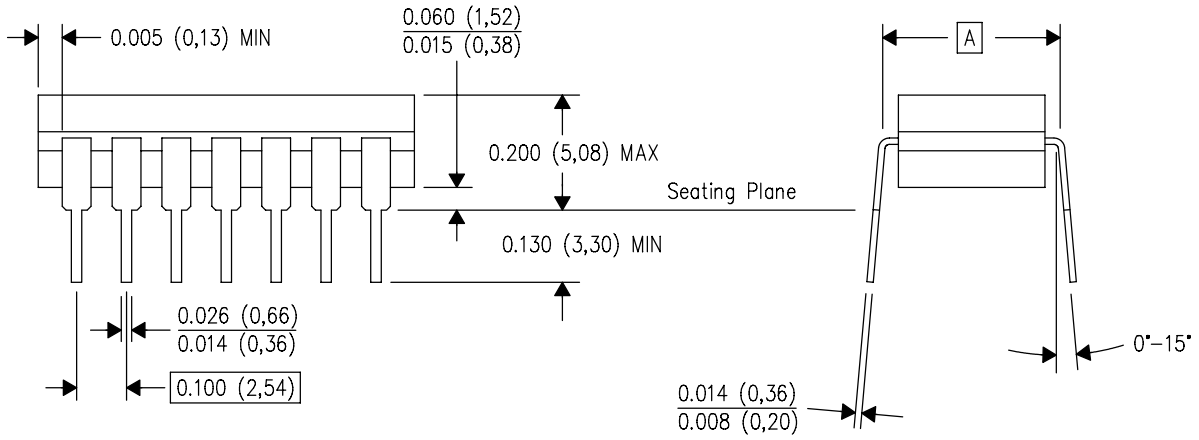
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



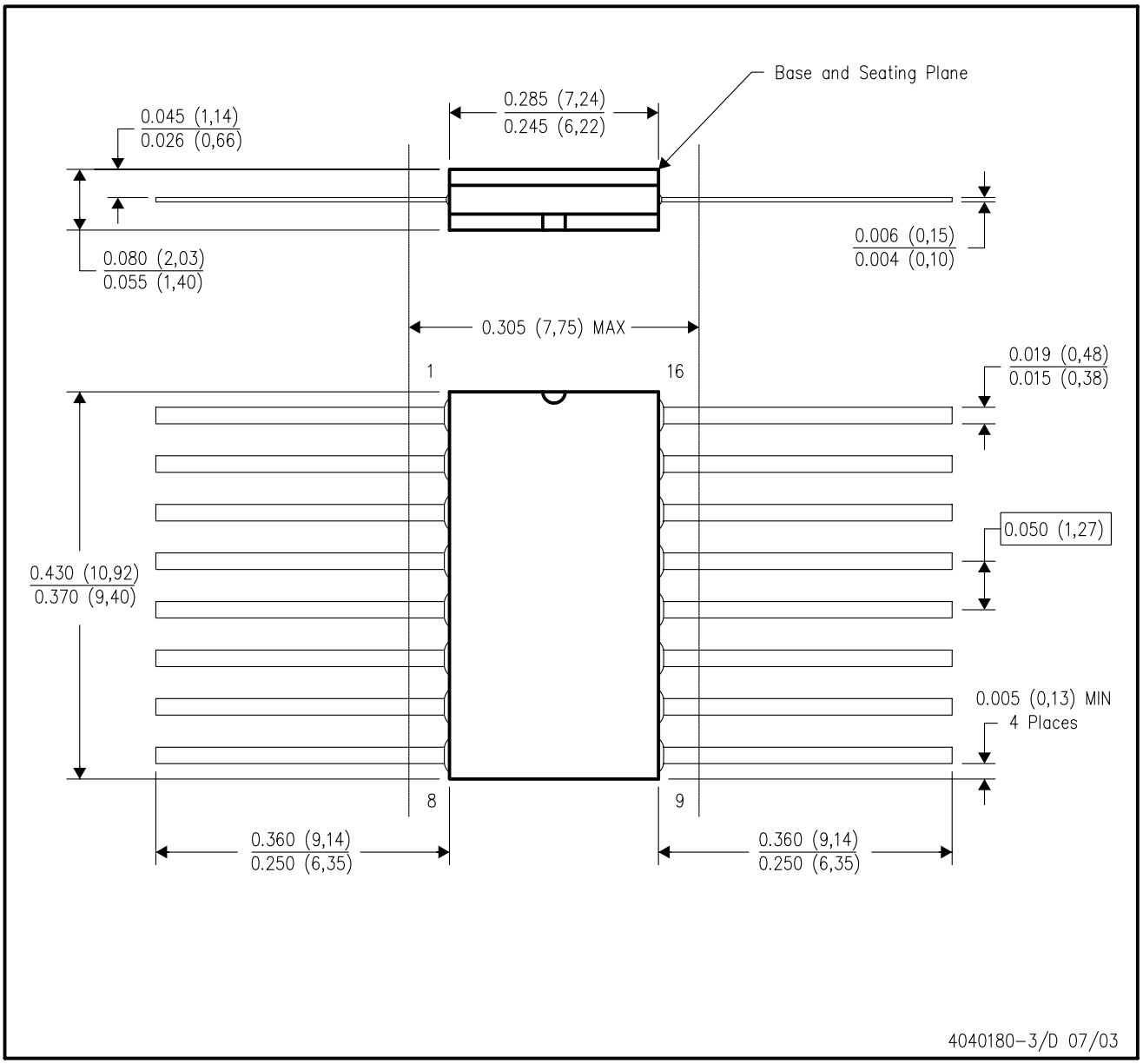
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

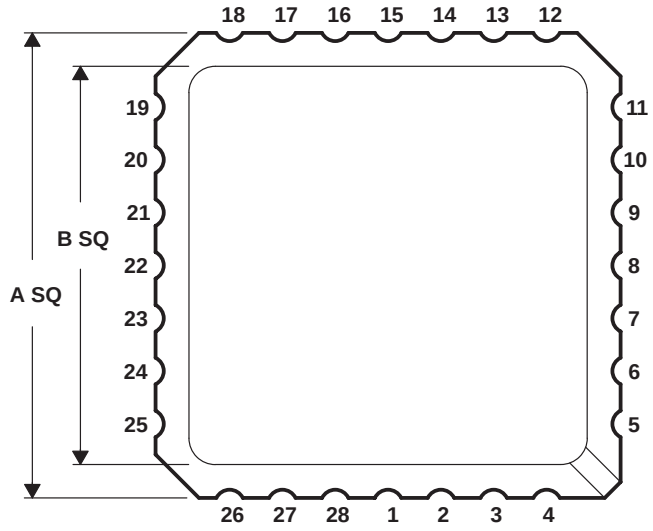
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



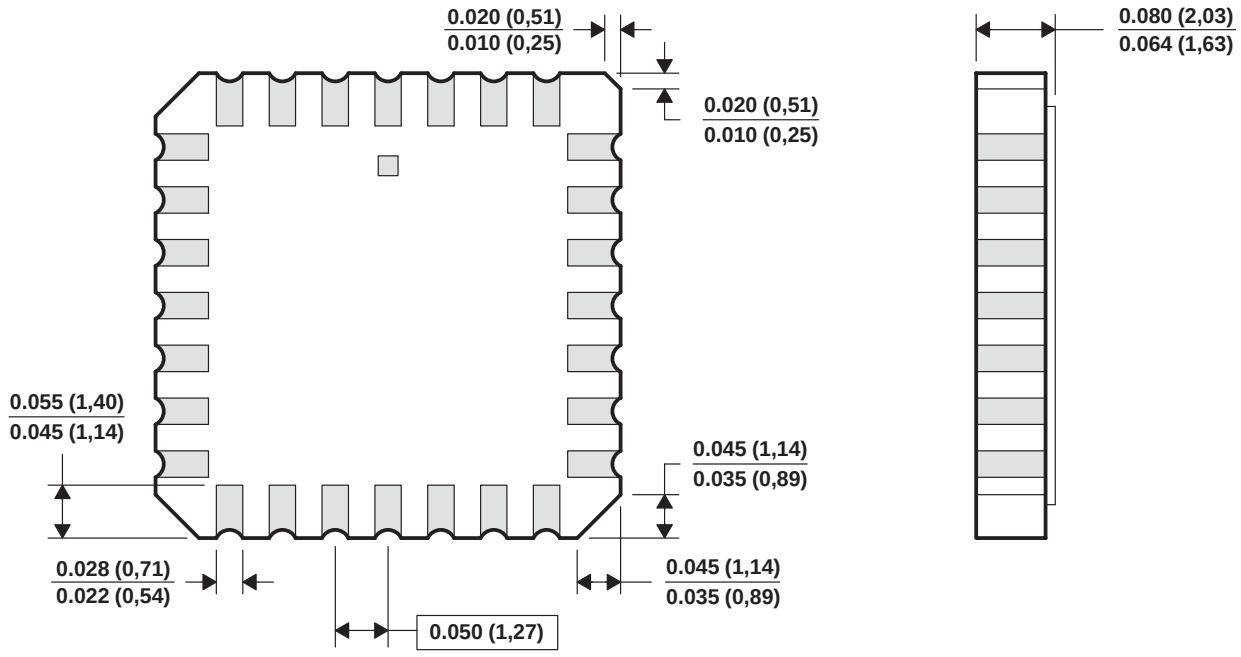
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



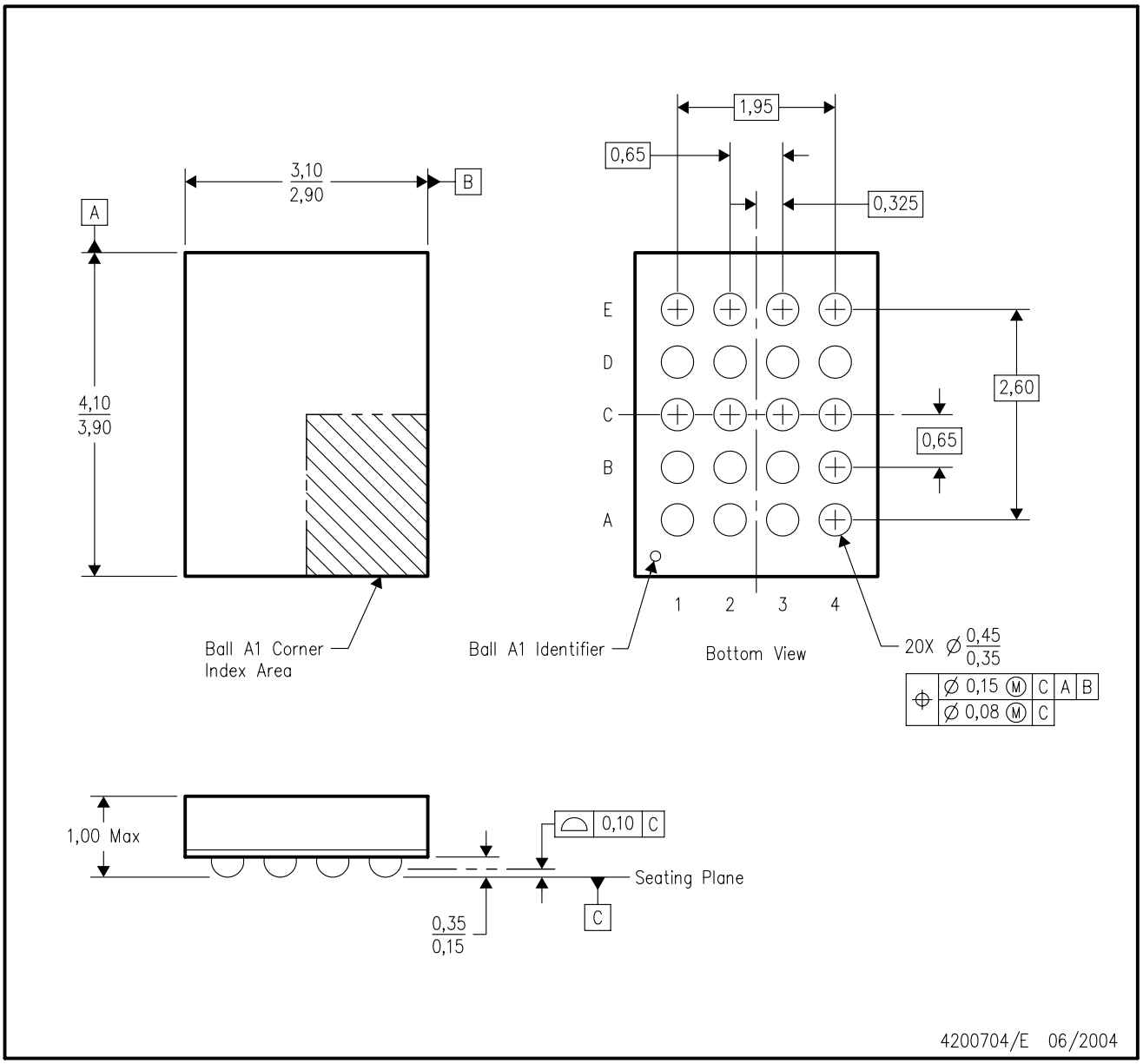
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

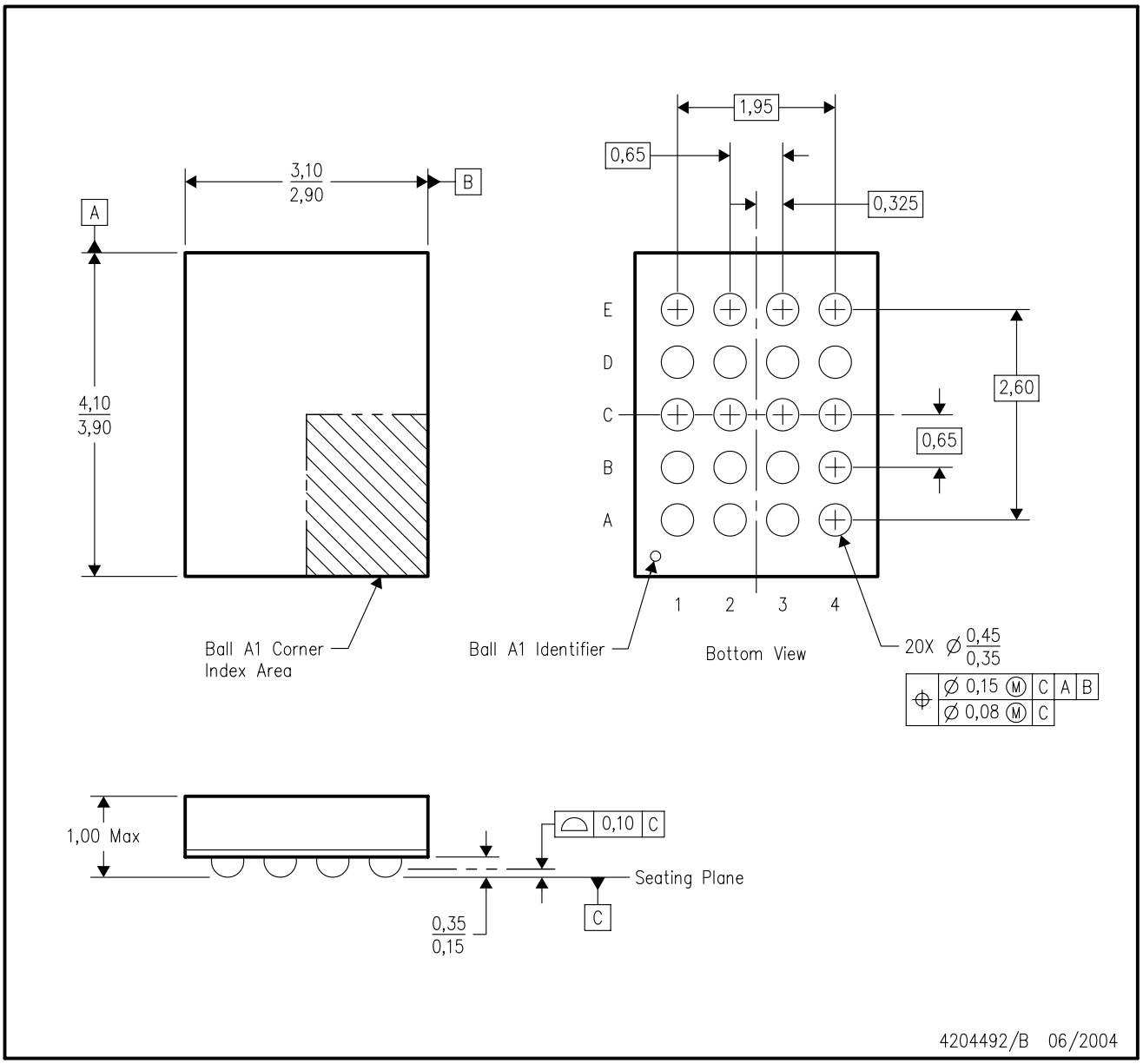
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

GQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is tin–lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead–free.

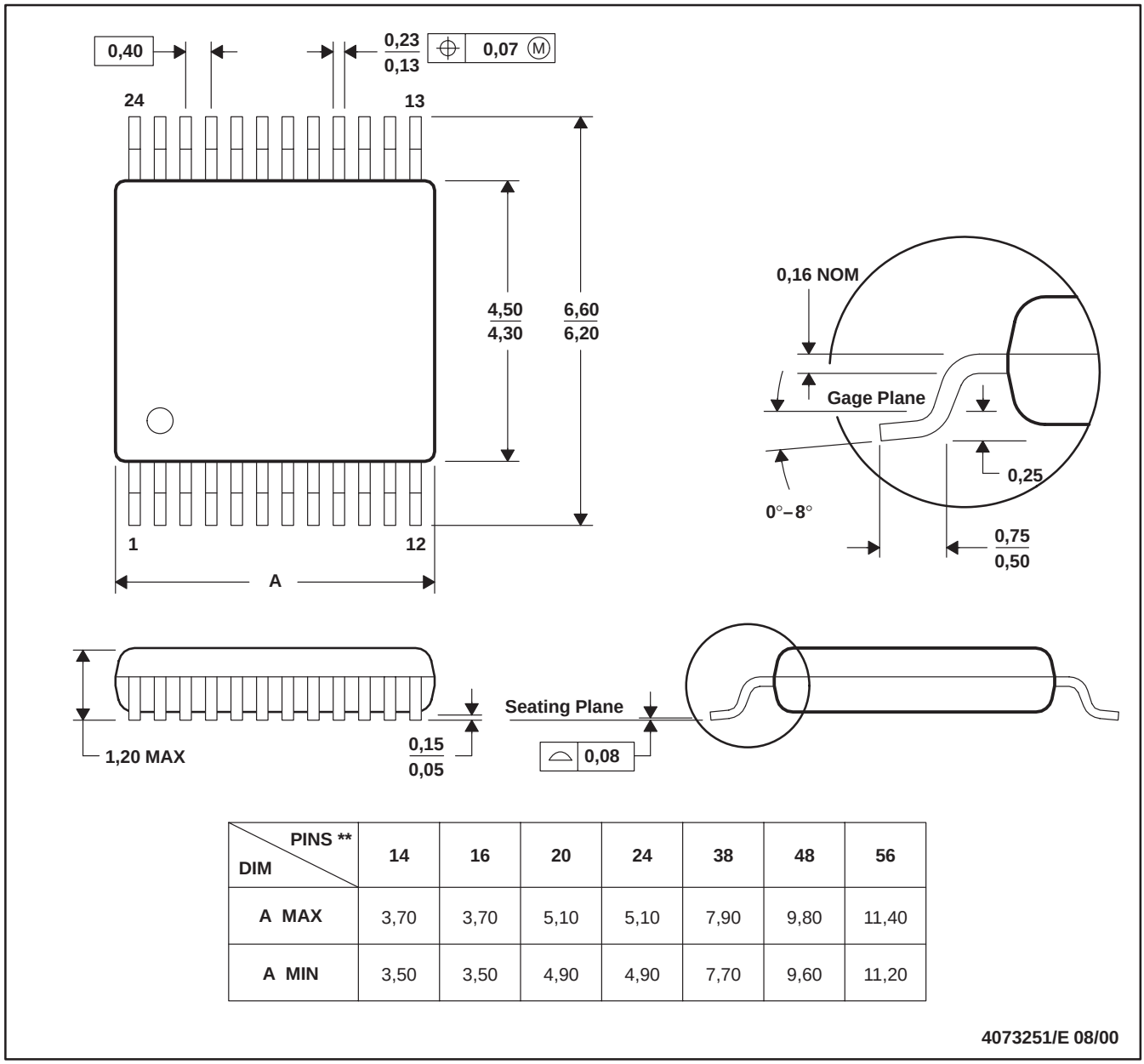
ZQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

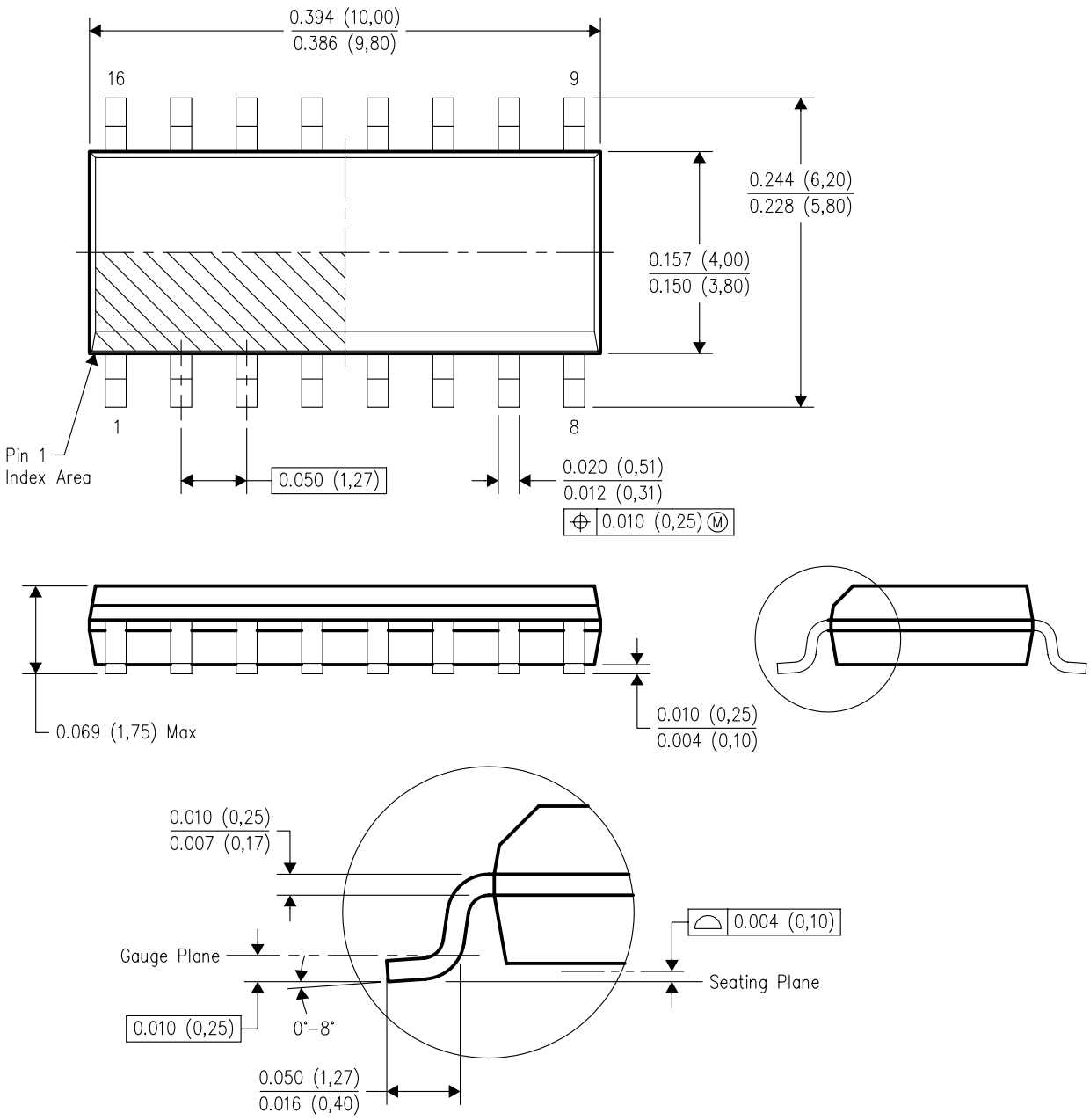


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

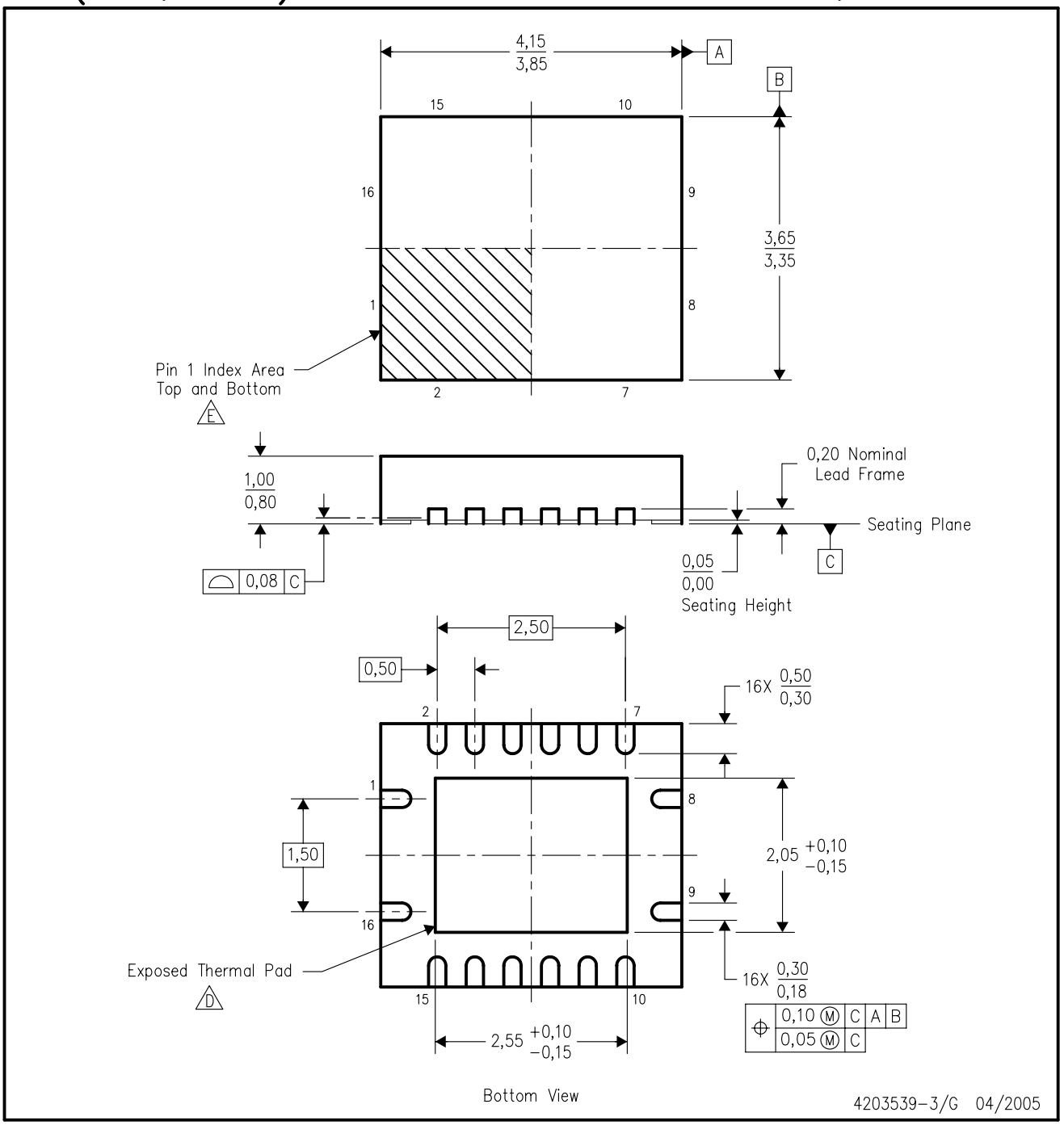
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK

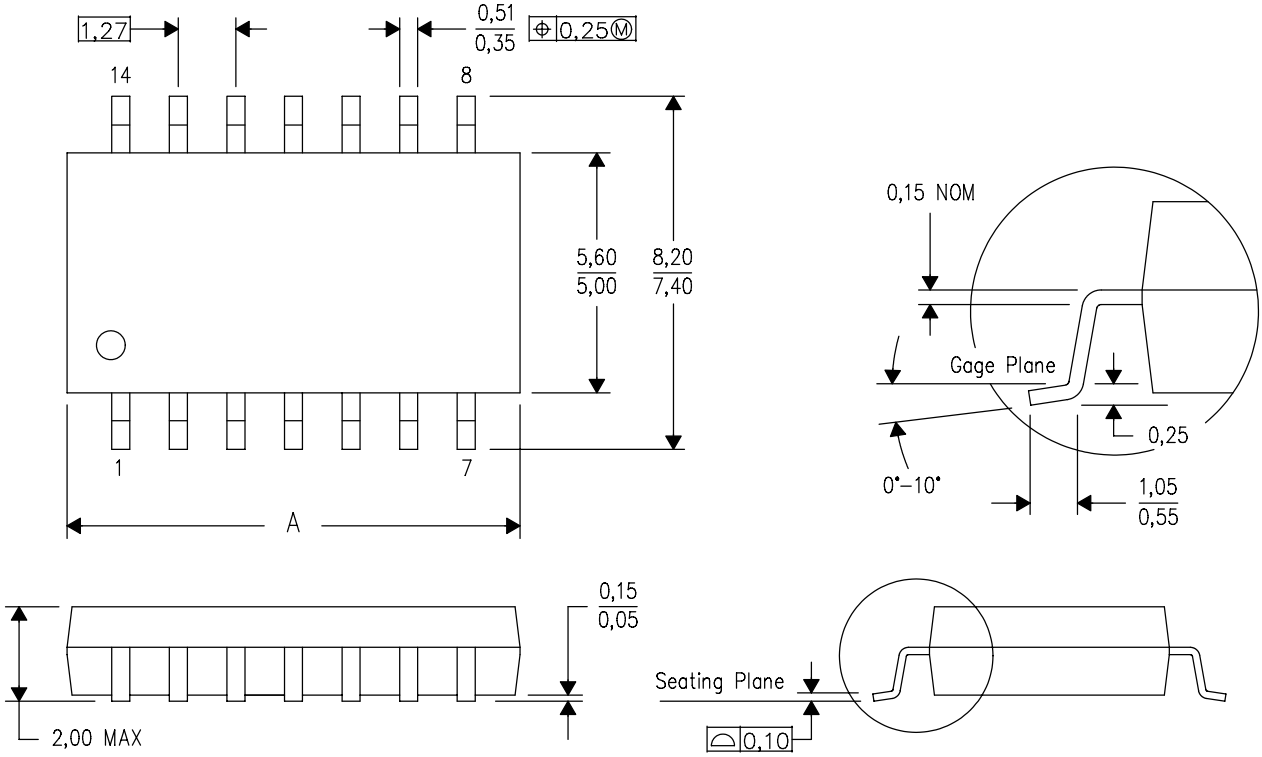


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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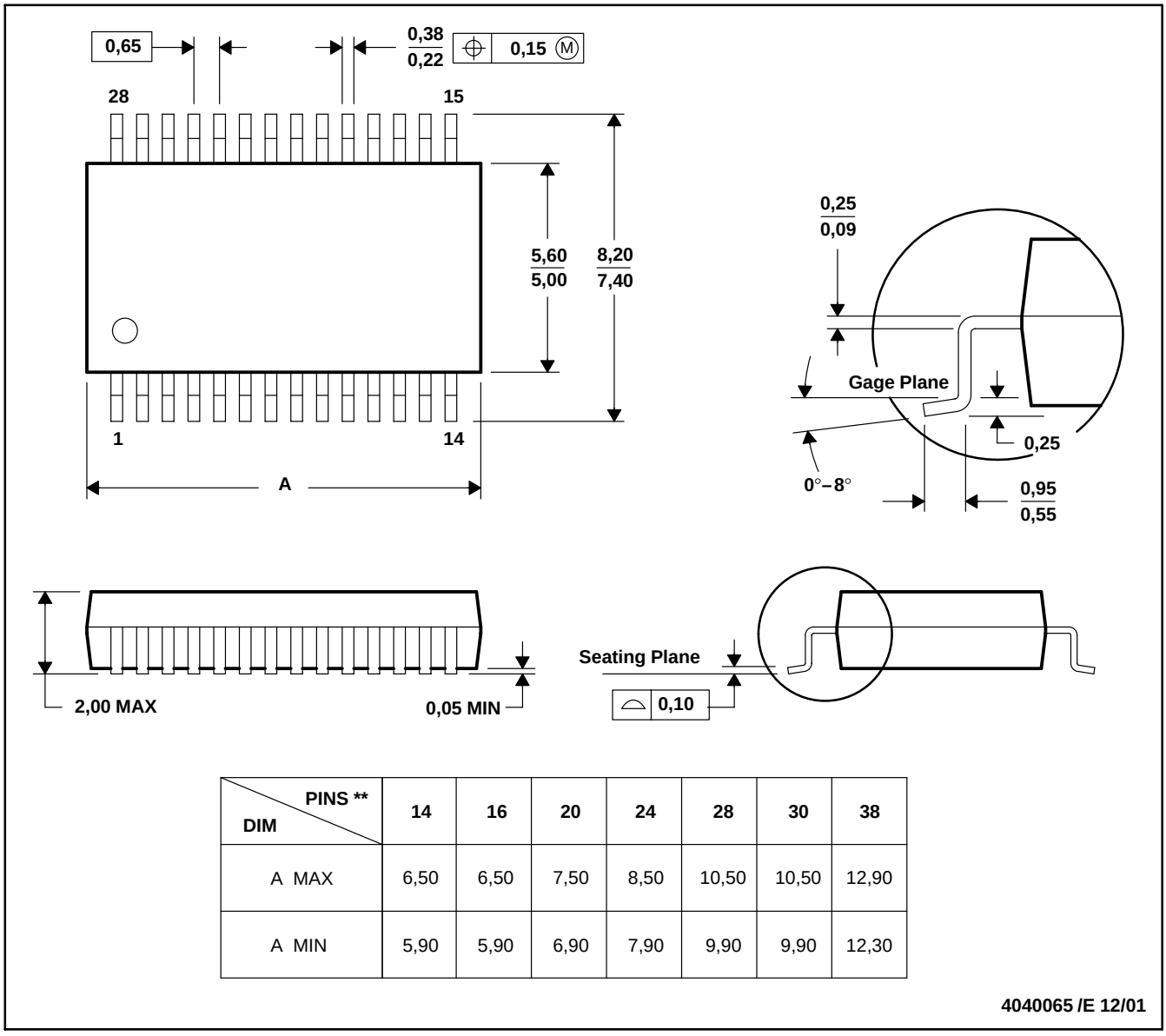
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



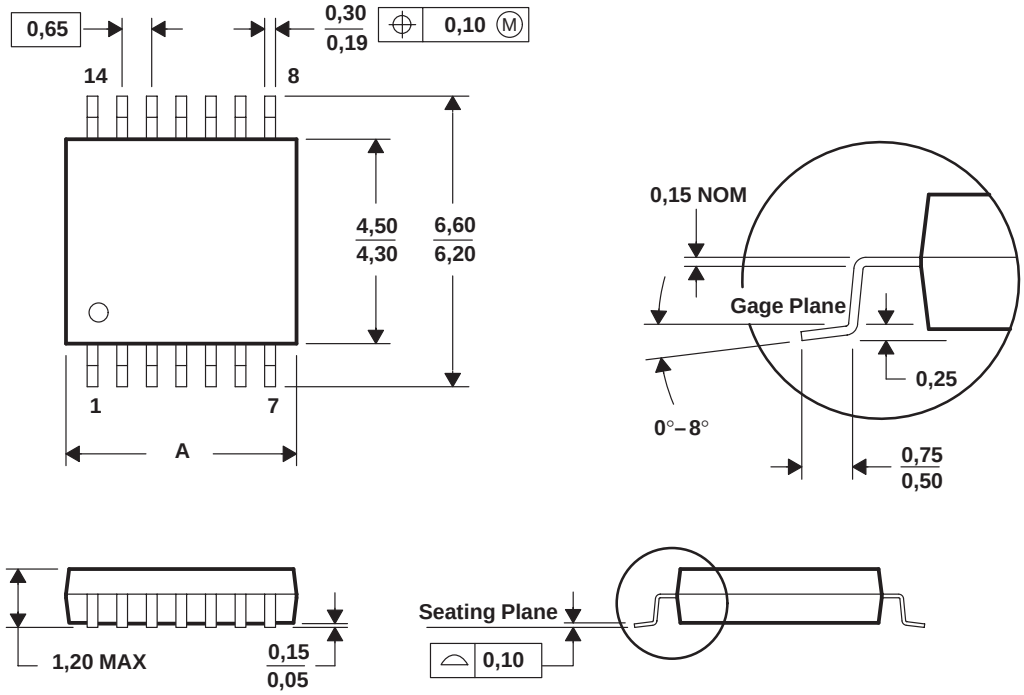
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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