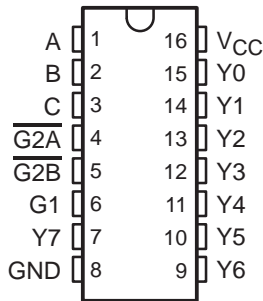


# SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

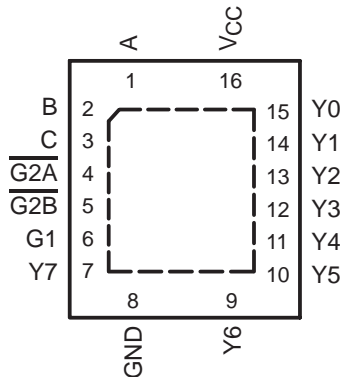
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.8 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

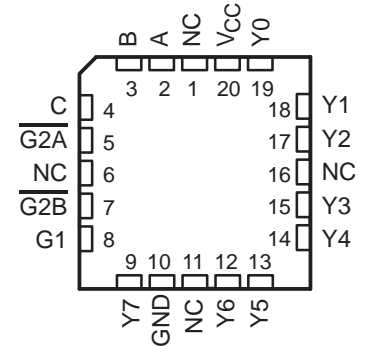
SN54LVC138A ... J OR W PACKAGE  
SN74LVC138A ... D, DB, DGV, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVC138A ... RGY PACKAGE  
(TOP VIEW)



SN54LVC138A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN54LVC138A 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC138A 3-line to 8-line decoder/demultiplexer is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC138ARGYR	LC138A
	SOIC – D	Tube of 40	SN74LVC138AD	LVC138A
		Reel of 2500	SN74LVC138ADR	
		Reel of 250	SN74LVC138ADT	
	SOP – NS	Reel of 2000	SN74LVC138ANSR	LVC138A
	SSOP – DB	Reel of 2000	SN74LVC138ADBR	LC138A
	TSSOP – PW	Tube of 90	SN74LVC138APW	LC138A
		Reel of 2000	SN74LVC138APWR	
		Reel of 250	SN74LVC138APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC138ADGVR	LC138A
VFBGA – GQN	Reel of 1000	SN74LVC138AGQNR	LC138A	
		SN74LVC138AZQNR		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC138AJ	SNJ54LVC138AJ
	CFP – W	Tube of 150	SNJ54LVC138AW	SNJ54LVC138AW
	LCCC – FK	Tube of 55	SNJ54LVC138AFK	SNJ54LVC138AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

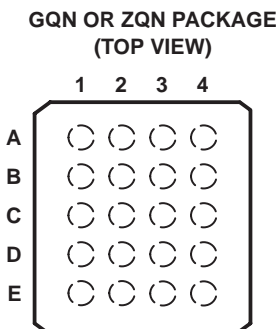
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## description/ordering information (continued)

The 'LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.



## terminal assignments

	1	2	3	4
A	B	A	V <sub>CC</sub>	Y0
B	C	NC	NC	Y1
C	$\overline{G2B}$	$\overline{G2A}$	Y3	Y2
D	G1	NC	NC	Y4
E	GND	Y7	Y6	Y5

NC – No internal connection

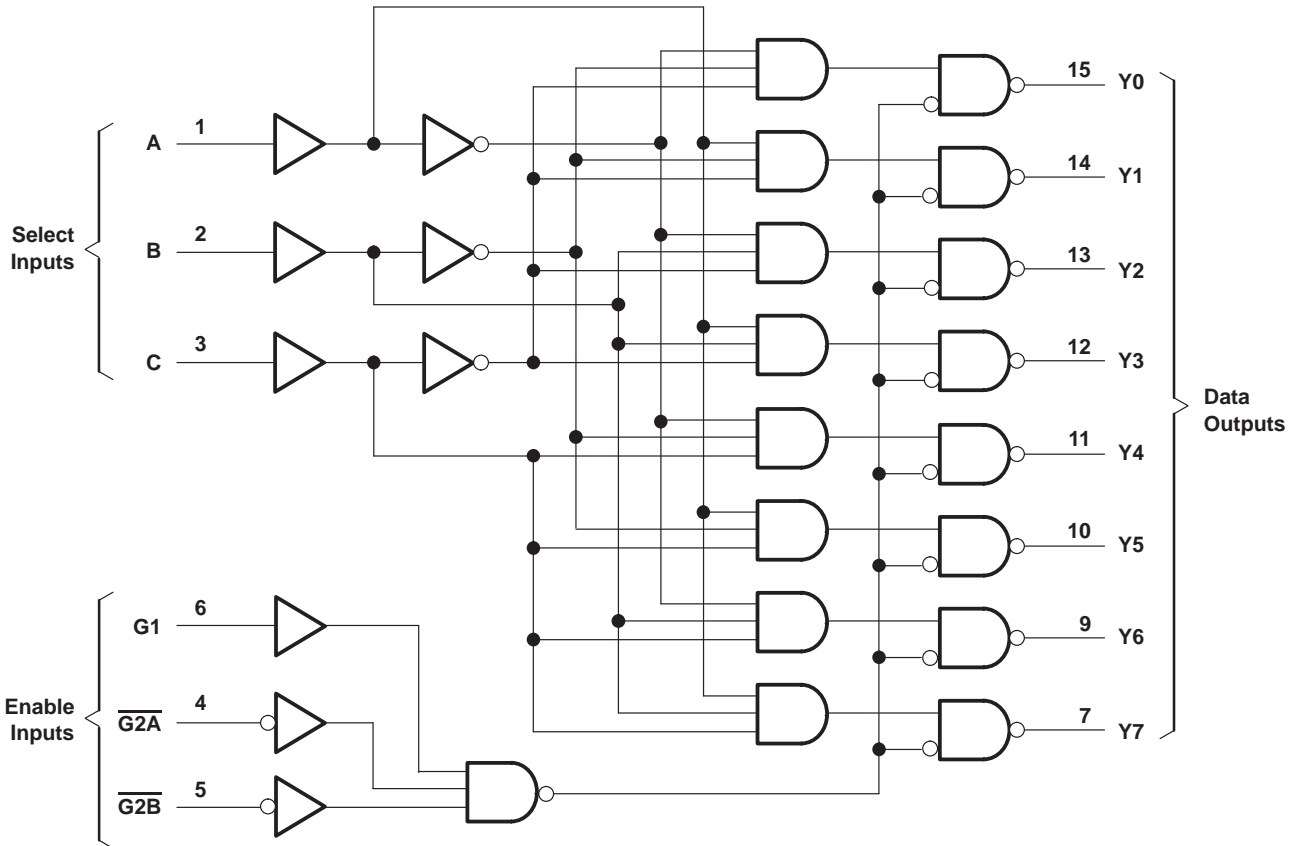
## FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

# SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

# SN54LVC138A, SN74LVC138A

## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): GQN/ZQN package	78°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 5)

		SN54LVC138A		SN74LVC138A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
$V_{IH}$ High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		2		
$V_{IL}$ Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			0.7		
	$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
$V_I$ Input voltage		0	5.5	0	5.5	V
$V_O$ Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current	$V_{CC} = 1.65$ V			–4		mA
	$V_{CC} = 2.3$ V			–8		
	$V_{CC} = 2.7$ V		–12	–12		
	$V_{CC} = 3$ V		–24	–24		
$I_{OL}$ Low-level output current	$V_{CC} = 1.65$ V			4		mA
	$V_{CC} = 2.3$ V			8		
	$V_{CC} = 2.7$ V		12	12		
	$V_{CC} = 3$ V		24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			10		10	ns/V
$T_A$ Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC138A			SN74LVC138A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V				V <sub>CC</sub> -0.2			V
		2.7 V to 3.6 V	V <sub>CC</sub> -0.2						
	I <sub>OH</sub> = -4 mA	1.65 V			1.2				
	I <sub>OH</sub> = -8 mA	2.3 V			1.7				
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		2.2				
		3 V	2.4		2.4				
I <sub>OH</sub> = -24 mA	3 V	2.2		2.2					
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V			0.2				
	I <sub>OL</sub> = 4 mA	1.65 V			0.45				
	I <sub>OL</sub> = 8 mA	2.3 V			0.7				
	I <sub>OL</sub> = 12 mA	2.7 V			0.4	0.4			
3 V				0.55	0.55				
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5			±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5			5		pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC138A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B or C	Y	7.9		1	6.7	ns
	G2A or G2B		7.4		1	6.5	
	G1		6.4		1	5.8	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC138A								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B or C	Y	1	22	1	9.9	1	7.9	1	6.7	ns
	G2A or G2B		1	21	1	9.4	1	7.4	1	6.5	
	G1		1	20.3	1	8.4	1	6.4	1	5.8	
t <sub>sk(o)</sub>									1	ns	



# SN54LVC138A, SN74LVC138A

## 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

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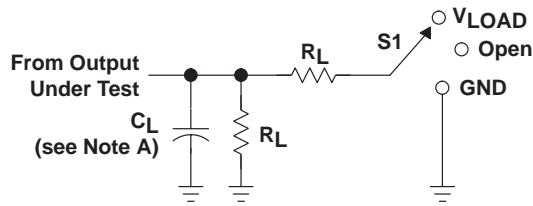
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operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	VCC = 1.8 V	VCC = 2.5 V	VCC = 3.3 V	UNIT
		TYP	TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance	f = 10 MHz	25	26	27	pF



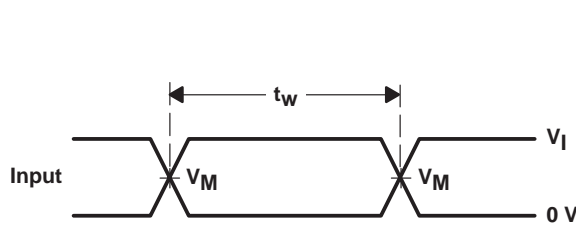
## PARAMETER MEASUREMENT INFORMATION



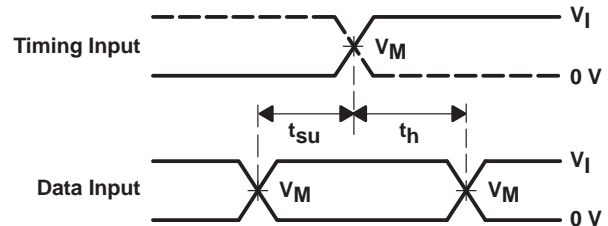
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

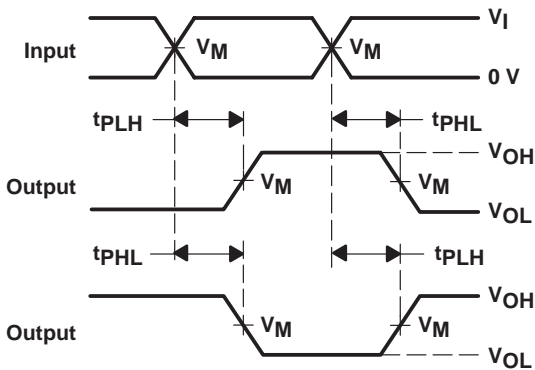
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



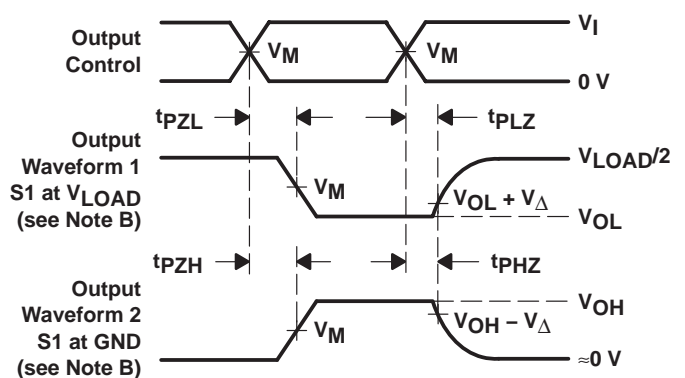
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

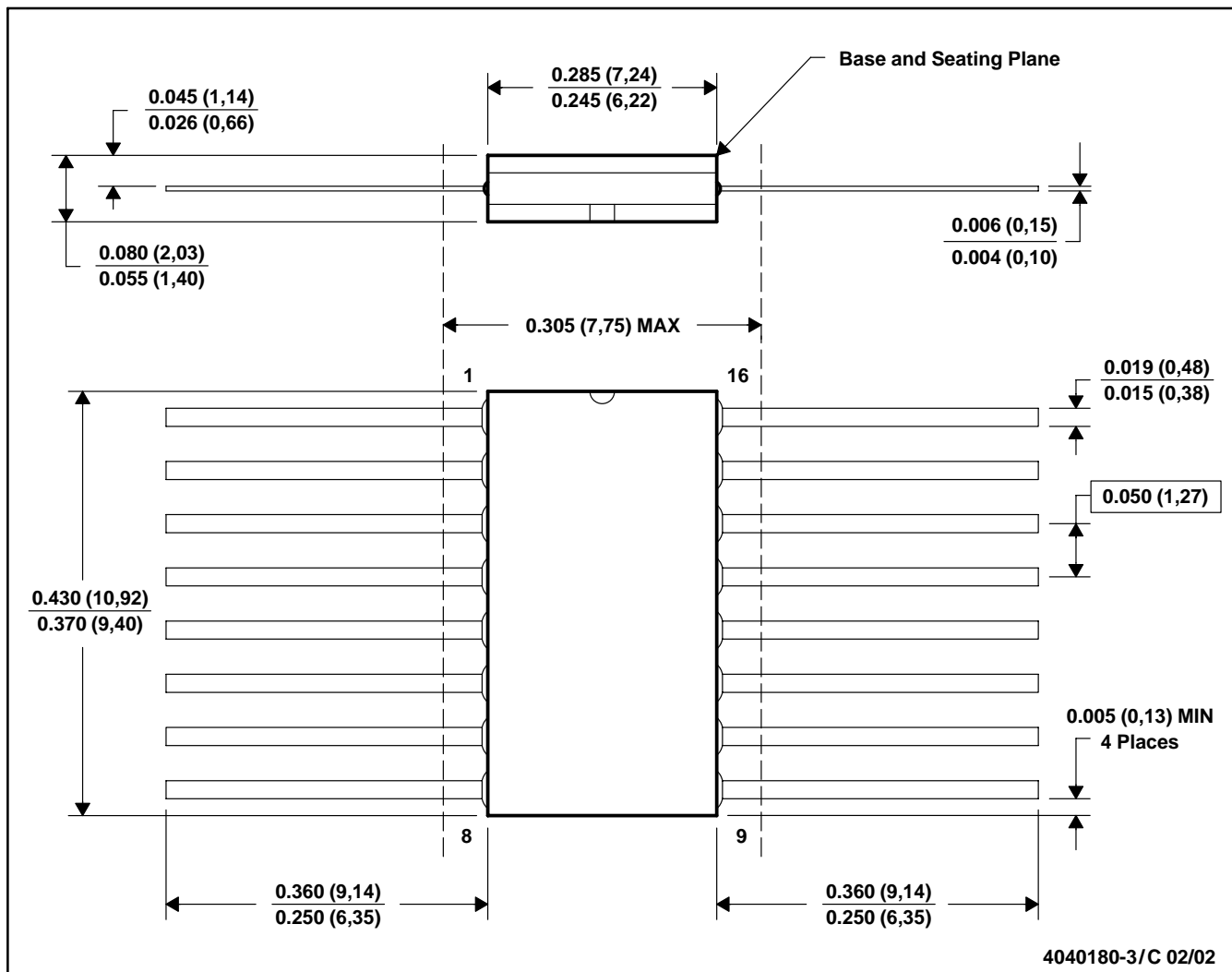


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/C 02/02

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835 GDFP-1F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

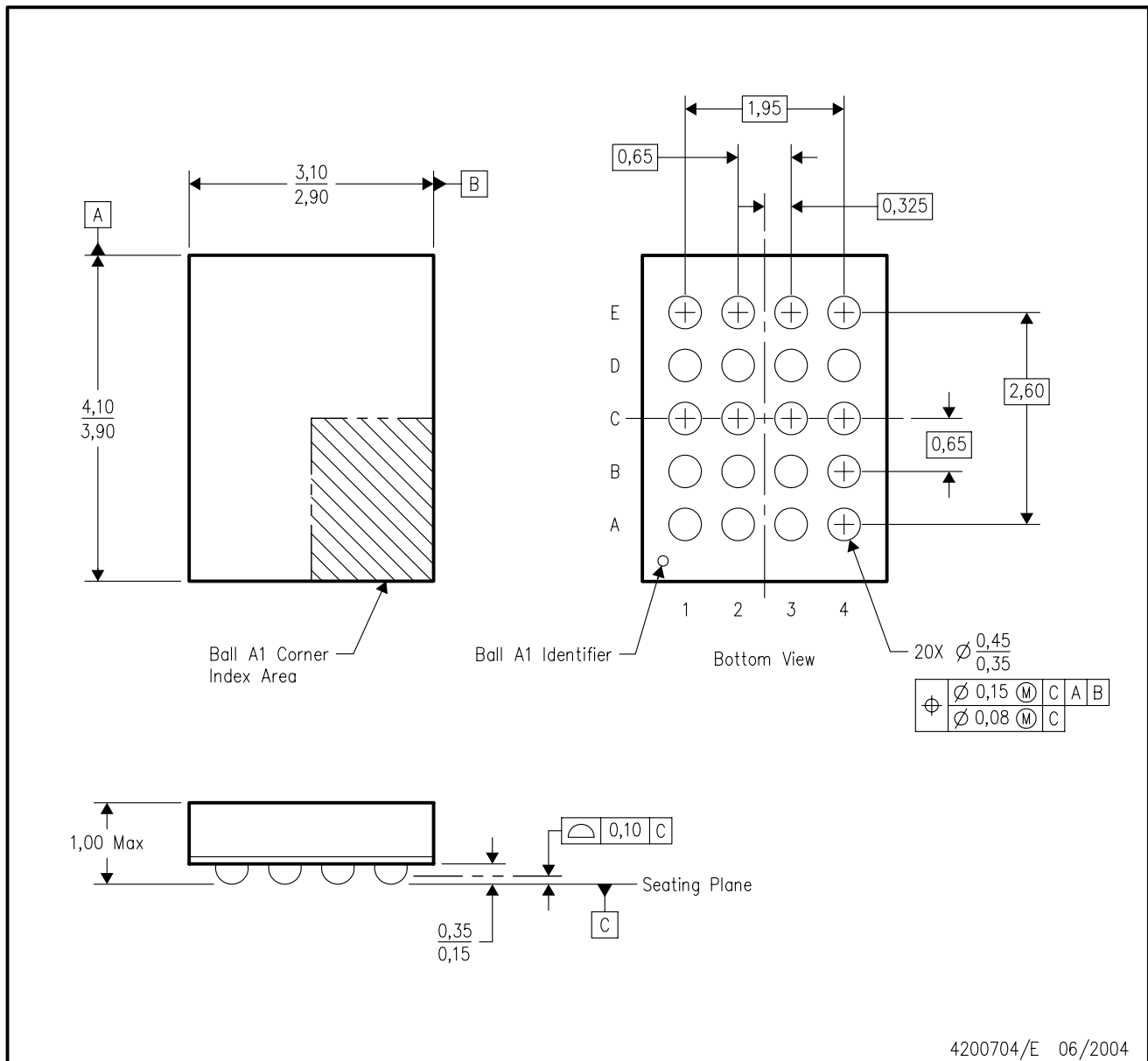
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

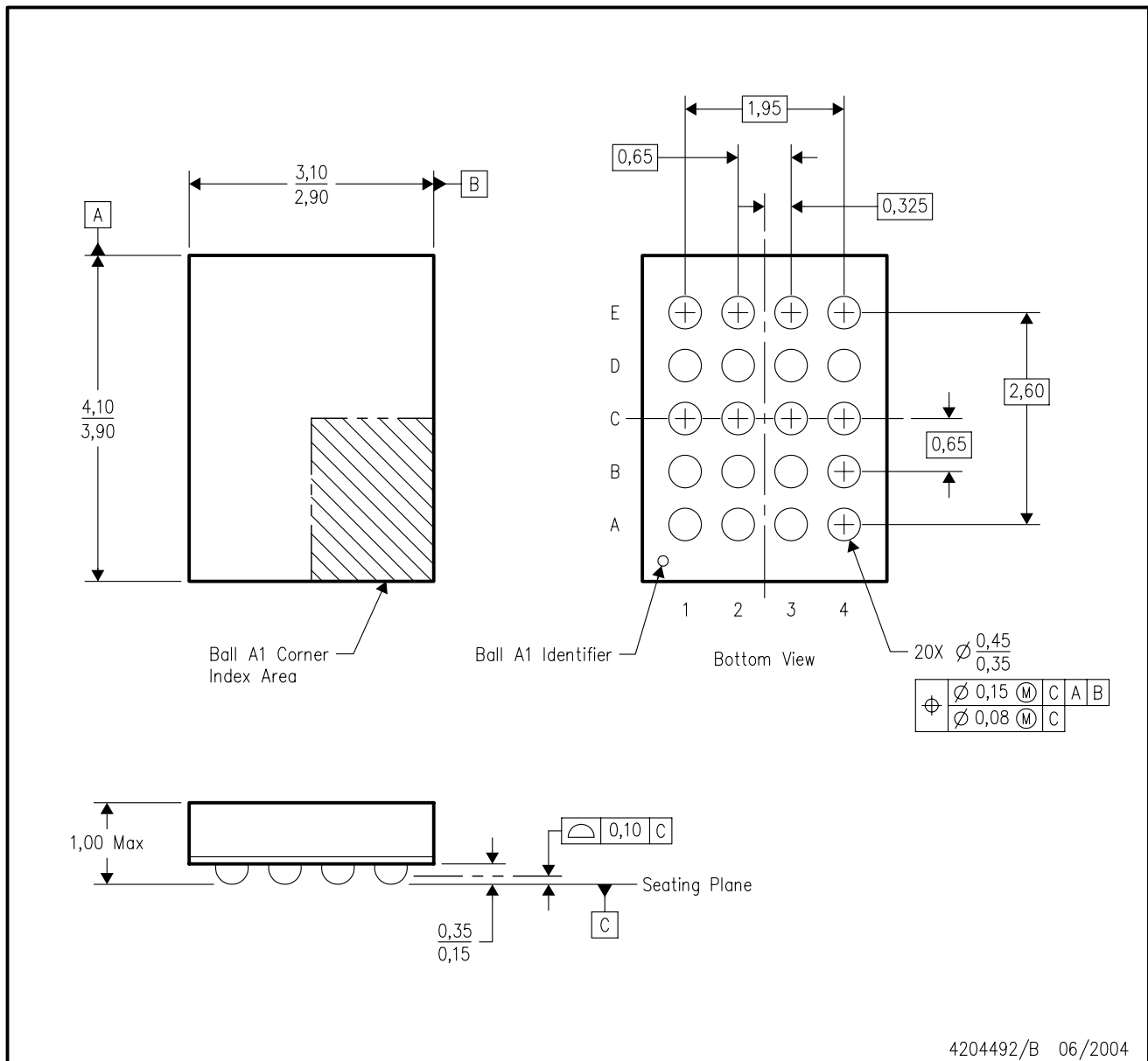


4200704/E 06/2004

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC M0-225 variation BC.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



4204492/B 06/2004

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

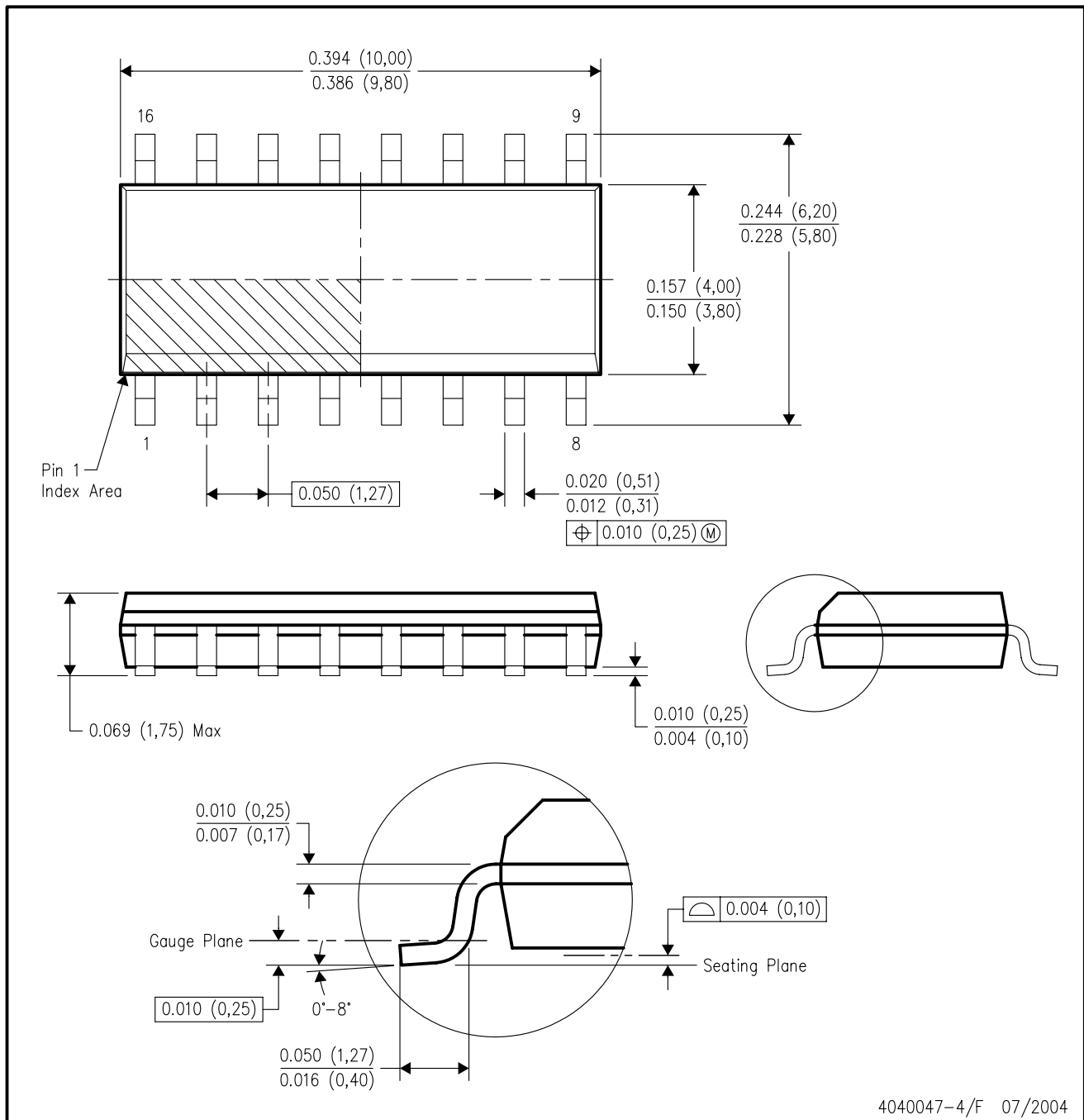


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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