

SN74LVC125A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS290N – JANUARY 1993 – REVISED FEBRUARY 2004

- Operates From 1.65 V to 3.6 V
- Specified From -40°C to 85°C and -40°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

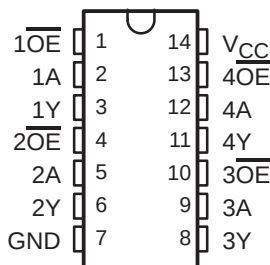
This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

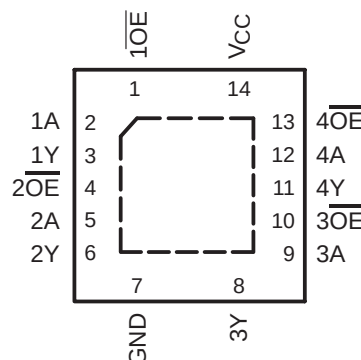
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

D, DB, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC125ARGYR	LC125A
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC125AD	LVC125A
		Reel of 2500	SN74LVC125ADR	
		Reel of 250	SN74LVC125ADT	
	SOP – NS	Reel of 2000	SN74LVC125ANSR	LVC125A
	SSOP – DB	Reel of 2000	SN74LVC125ADBR	LC125A
	TSSOP – PW	Tube of 90	SN74LVC125APW	LC125A
		Reel of 2000	SN74LVC125APWR	
		Reel of 250	SN74LVC125APWT	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74LVC125A

QUADRUPLE BUS BUFFER GATE

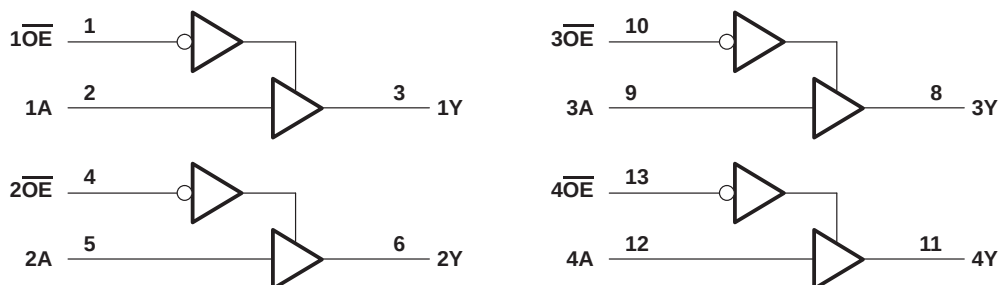
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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C
Power dissipation, P_{tot} ($T_A = -40^\circ\text{C}$ to 125°C) (see Notes 5 and 6)	500 mW

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.
 5. For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
 6. For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

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recommended operating conditions (see Note 7)

		T _A = 25°C		–40 TO 85°C		–40 TO 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC} Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		1.5		
V _{IH} High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65×V _{CC}		0.65×V _{CC}		0.65×V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
	V _{CC} = 2.7 V to 3.6 V	2		2		2		
V _{IL} Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35×V _{CC}		0.35×V _{CC}		0.35×V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V	0.7		0.7		0.7		
	V _{CC} = 2.7 V to 3.6 V	0.8		0.8		0.8		
V _I Input voltage		0	5.5	0	5.5	0	5.5	V
V _O Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH} High-level output current	V _{CC} = 1.65 V	–4		–4		–4		mA
	V _{CC} = 2.3 V	–8		–8		–8		
	V _{CC} = 2.7 V	–12		–12		–12		
	V _{CC} = 3 V	–24		–24		–24		
I _{OL} Low-level output current	V _{CC} = 1.65 V	4		4		4		mA
	V _{CC} = 2.3 V	8		8		8		
	V _{CC} = 2.7 V	12		12		12		
	V _{CC} = 3 V	24		24		24		mA
Δt/Δv Input transition rise or fall rate		8		8		8		ns/V

NOTE 7: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} –0.2			V _{CC} –0.2		V _{CC} –0.3		V
	I _{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3 V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
	I _{OH} = –24 mA	3 V	2.3			2.2		2		
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65 V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3 V	0.3			0.7		0.75		
	I _{OL} = 12 mA	2.7 V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3 V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±1			±10		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3 V	5							pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	1	4.5	11.8	1	12.3	1	13.8	ns
			2.5 V ± 0.2 V	1	2.7	5.8	1	6.3	1	8.4	
			2.7 V	1	3	5.3	1	5.5	1	7	
			3.3 V ± 0.3 V	1	2.5	4.6	1	4.8	1	6	
t _{en}	$\overline{\text{OE}}$	Y	1.8 V ± 0.15 V	1	4.3	13.8	1	14.3	1	15.8	ns
			2.5 V ± 0.2 V	1	2.7	6.9	1	7.4	1	9.5	
			2.7 V	1	3.3	6.4	1	6.6	1	8.5	
			3.3 V ± 0.3 V	1	2.4	5.2	1	5.4	1	7	
t _{dis}	$\overline{\text{OE}}$	Y	1.8 V ± 0.15 V	1	4.3	10.6	1	11.1	1	12.6	ns
			2.5 V ± 0.2 V	1	2.2	5.1	1	5.6	1	7.7	
			2.7 V	1	2.5	4.8	1	5	1	6.5	
			3.3 V ± 0.3 V	1	2.4	4.4	1	4.6	1	6	
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns

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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	7.4	pF
			2.5 V	11.3	
			3.3 V	15	



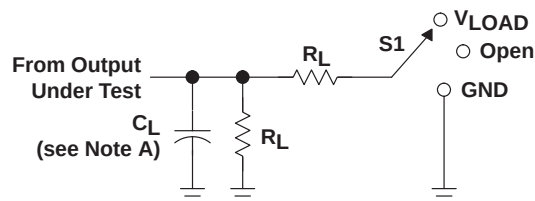
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QUADRUPLE BUS BUFFER GATE

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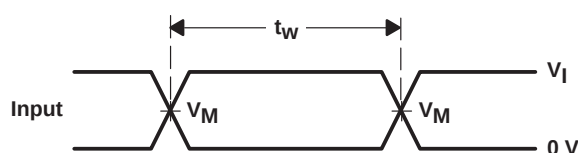
PARAMETER MEASUREMENT INFORMATION



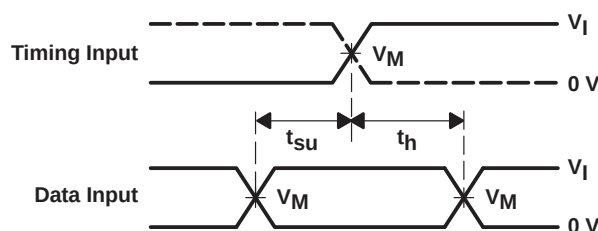
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

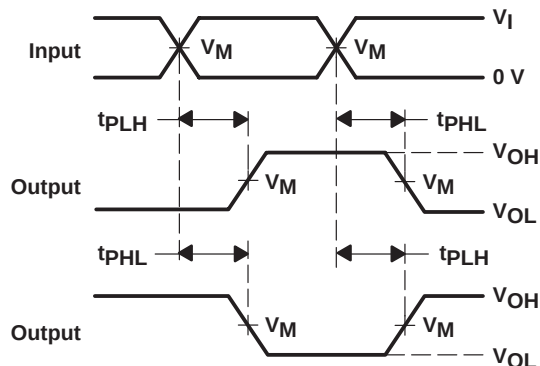
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



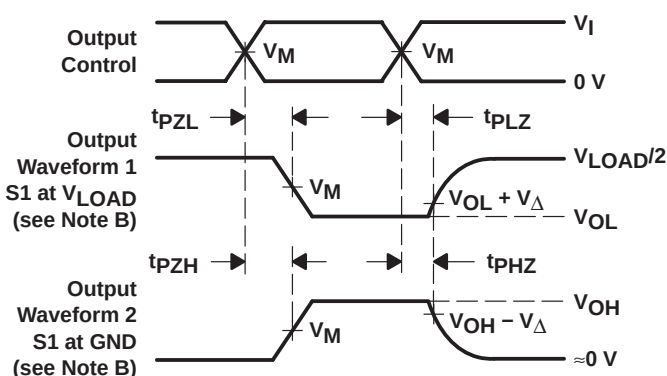
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

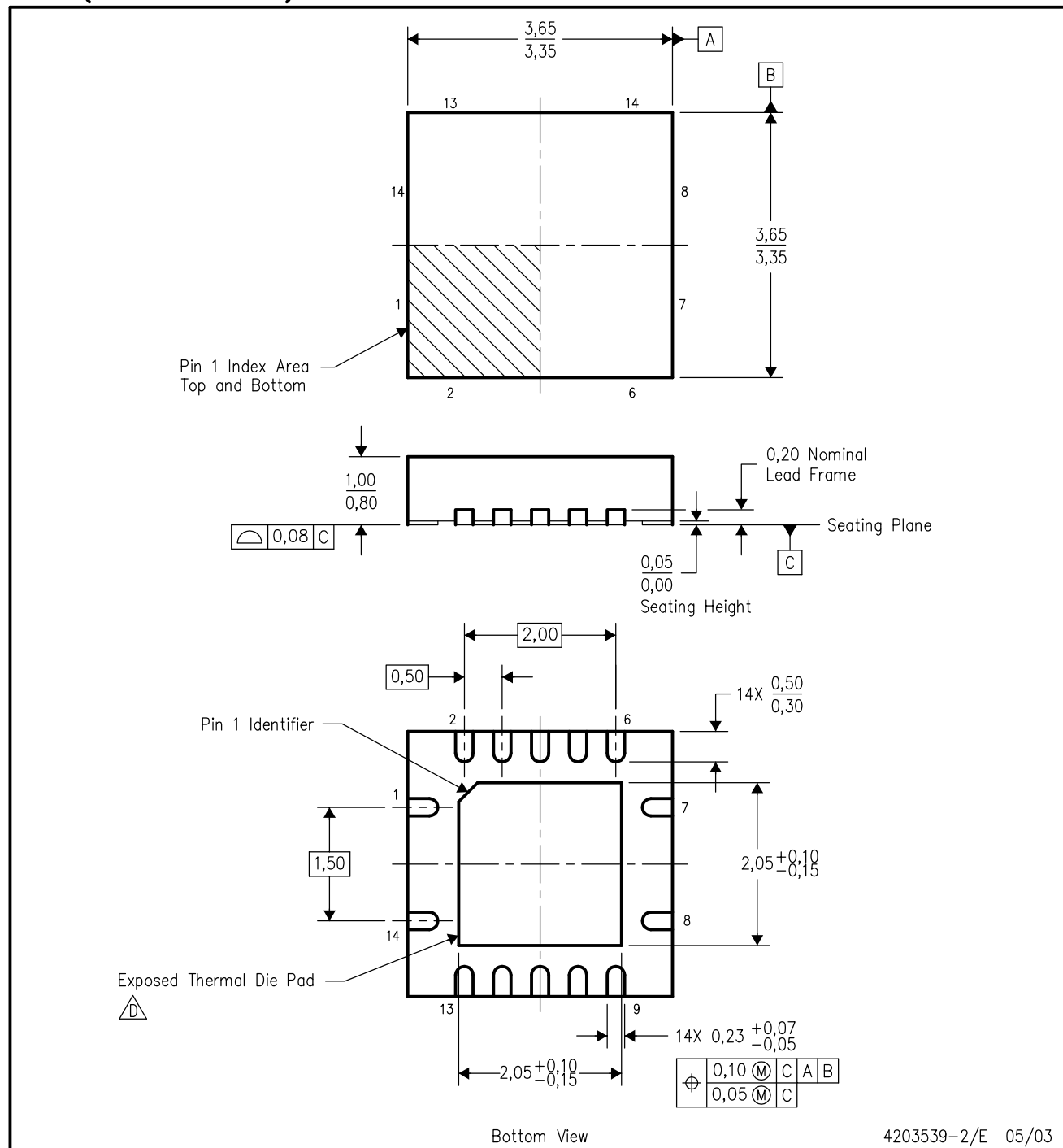
Figure 1. Load Circuit and Voltage Waveforms



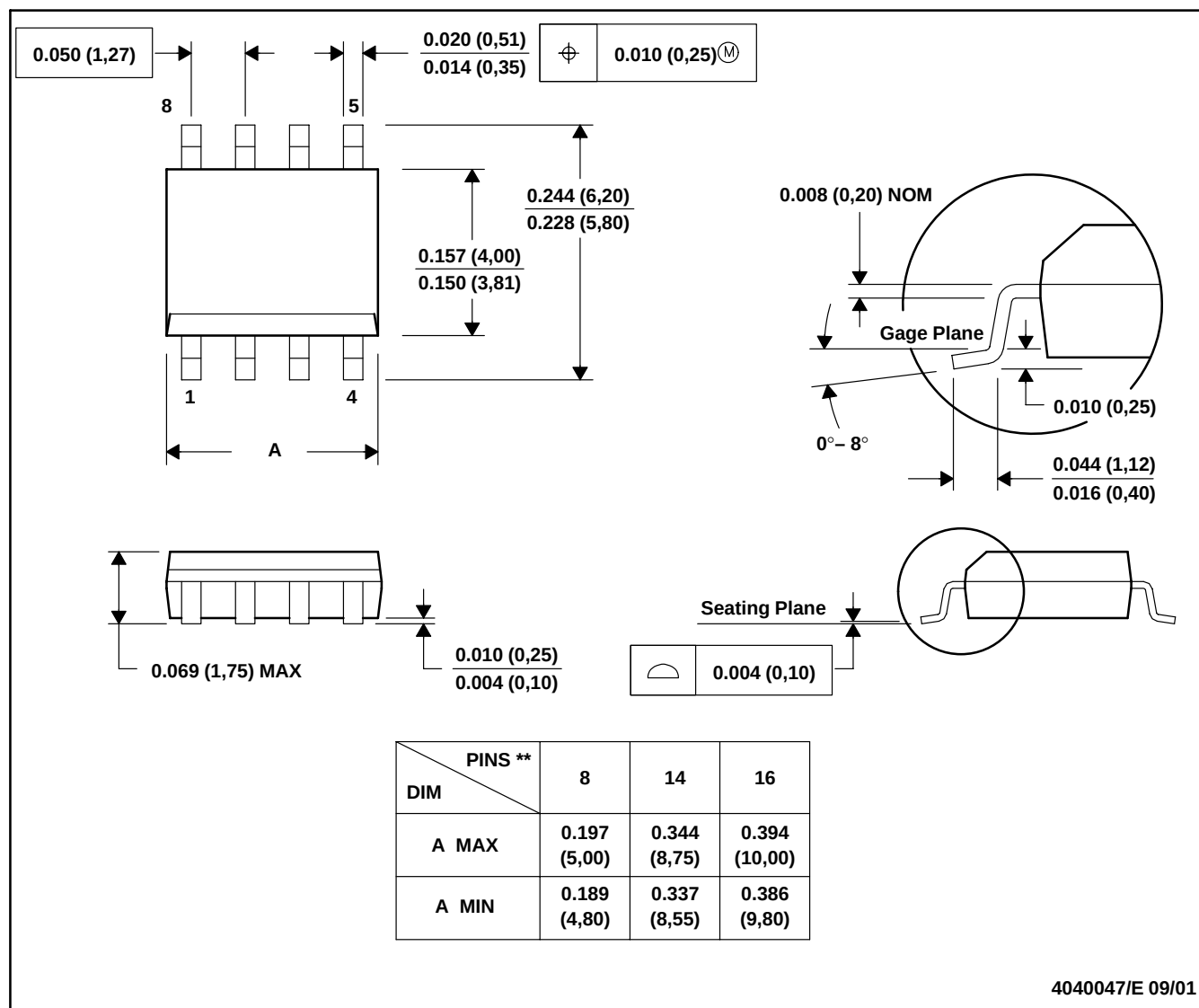
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RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

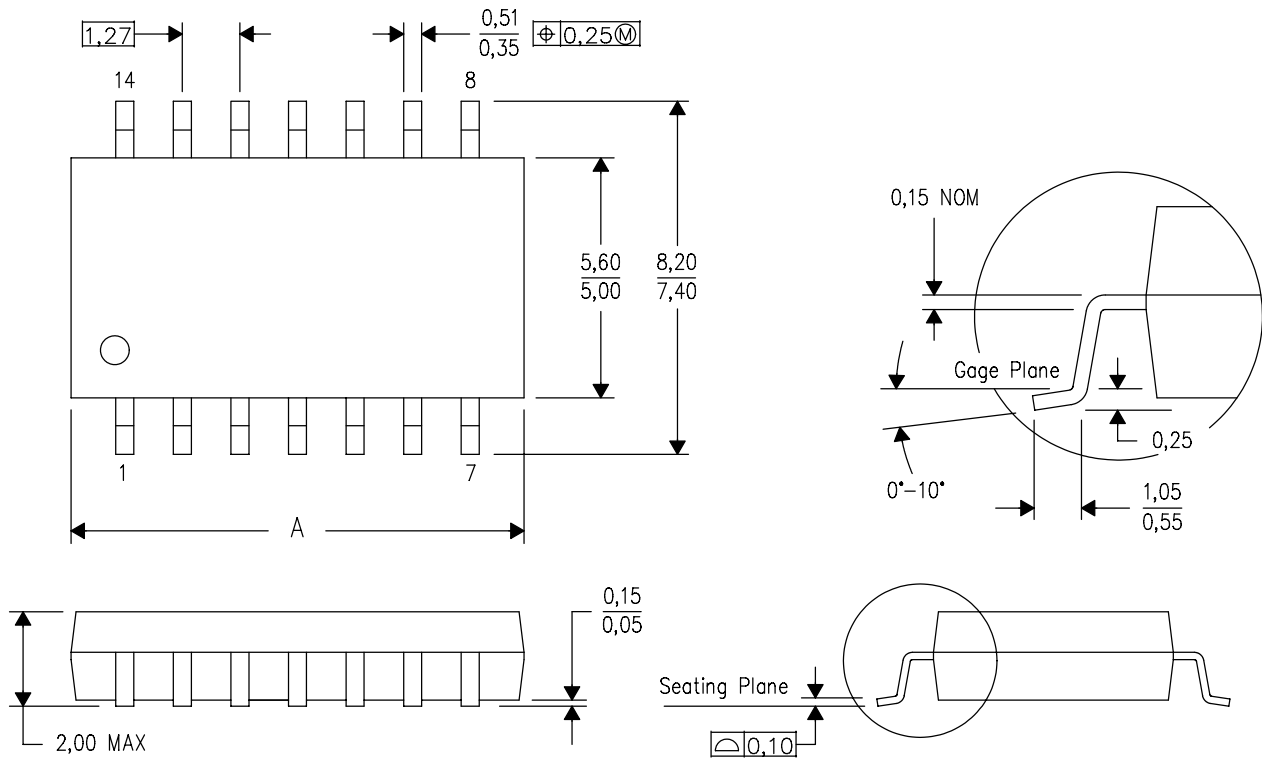
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

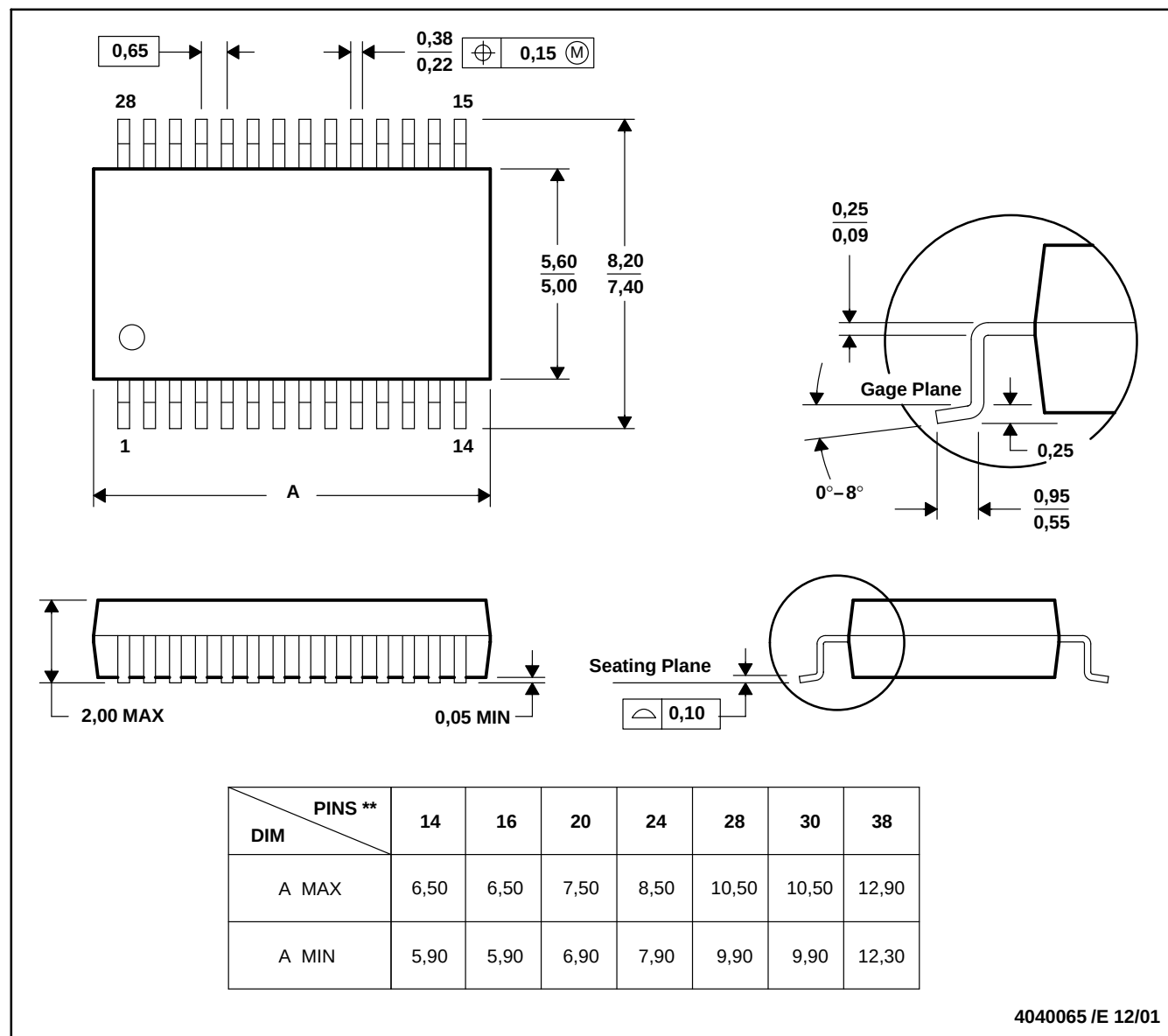
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

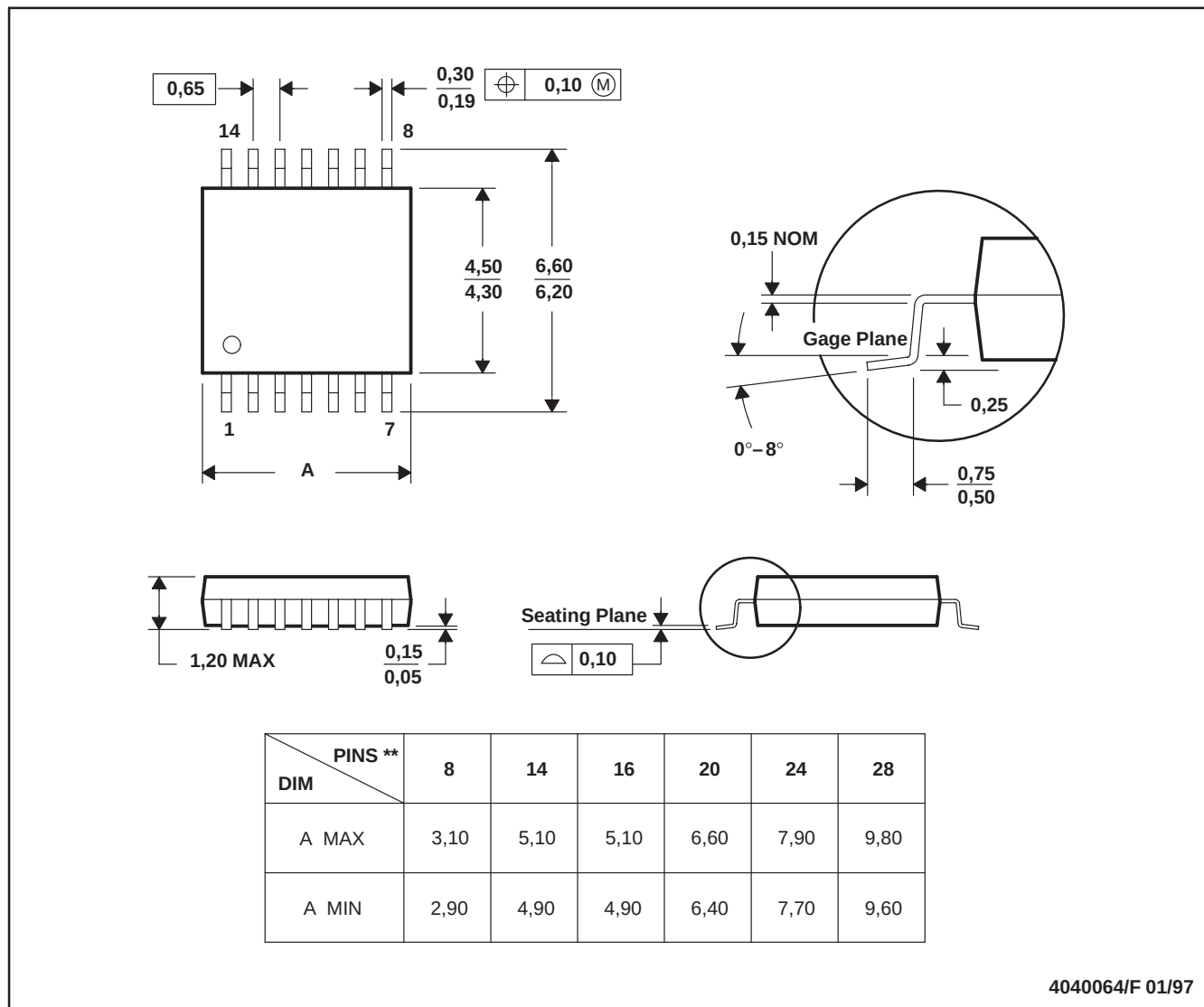


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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