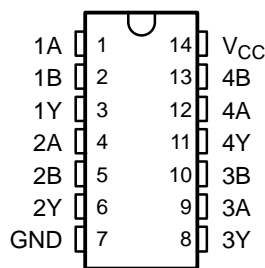


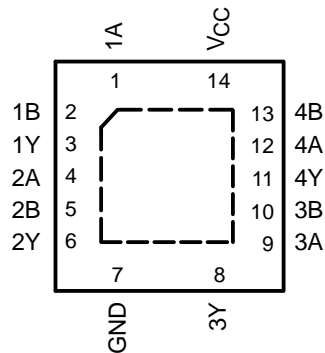
FEATURES

- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.1 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

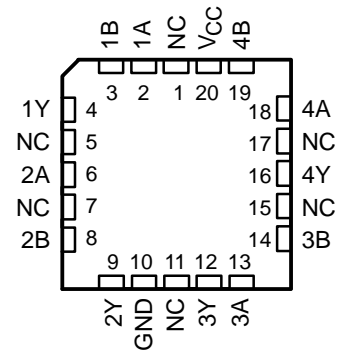
SN54LVC08A ... J OR W PACKAGE
SN74LVC08A ... D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC08A ... RGY PACKAGE
(TOP VIEW)



SN54LVC08A ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC08A quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC08A quadruple 2-input positive-AND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC08A devices perform the Boolean function $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVC08A, SN74LVC08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCAS283P–JANUARY 1993–REVISED AUGUST 2005

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC08ARGYR	LC08A
–40°C to 125°C	SOIC – D	Tube of 50	SN74LVC08AD	LVC08A
		Reel of 2500	SN74LVC08ADR	
		Reel of 250	SN74LVC08ADT	
	SOP – NS	Reel of 2000	SN74LVC08ANSR	LVC08A
	SSOP – DB	Reel of 2000	SN74LVC08ADBR	LC08A
	TSSOP – PW	Tube of 90	SN74LVC08APW	LC08A
		Reel of 2000	SN74LVC08APWR	
Reel of 250		SN74LVC08APWT		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC08AJ	SNJ54LVC08AJ
	CFP – W	Tube of 150	SNJ54LVC08AW	SNJ54LVC08AW
	LCCC – FK	Tube of 55	SNJ54LVC08AFK	SNJ54LVC08AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH GATE)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50 mA
I_{OK}	Output clamp current	$V_O < 0$		-50 mA
I_O	Continuous output current			±50 mA
	Continuous current through V_{CC} or GND			±100 mA
θ_{JA}	Package thermal impedance	D package ⁽⁴⁾		86
		DB package ⁽⁴⁾		96
		NS package ⁽⁴⁾		76
		PW package ⁽⁴⁾		113
		RGY package ⁽⁵⁾		47
T_{stg}	Storage temperature range	-65	150	°C
P_{tot}	Power dissipation ⁽⁶⁾⁽⁷⁾	$T_A = -40^\circ\text{C}$ to 125°C		500 mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above 70°C , the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, NS, and PW packages: above 60°C , the value of P_{tot} derates linearly with 5.5 mW/K.

SN54LVC08A, SN74LVC08A QUADRUPLE 2-INPUT POSITIVE-AND GATES

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Recommended Operating Conditions⁽¹⁾

		SN54LVC08A		UNIT		
		–55°C to 125°C				
		MIN	MAX			
V _{CC}	Supply voltage	Operating	2	3.6	V	
		Data retention only	1.5			
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		2	V	
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V	
V _I	Input voltage			0	5.5	V
V _O	Output voltage			0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		–12		mA
		V _{CC} = 3 V		–24		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12		mA
		V _{CC} = 3 V		24		
Δt/Δv	Input transition rise or fall rate			8	ns/V	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾

		SN74LVC08A						UNIT	
		T _A = 25°C		–40°C to 85°C		–40°C to 125°C			
		MIN	MAX	MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		–4		–4		mA
		V _{CC} = 2.3 V	–8		–8		–8		
		V _{CC} = 2.7 V	–12		–12		–12		
		V _{CC} = 3 V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		4		mA
		V _{CC} = 2.3 V	8		8		8		
		V _{CC} = 2.7 V	12		12		12		
		V _{CC} = 3 V	24		24		24		
Δt/Δv	Input transition rise or fall rate	8		8		8		ns/V	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC08A			UNIT
			–55°C to 125°C			
			MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = –100 μA	2.7 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2.2			
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			pF

(1) T_A = 25°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC08A						UNIT	
			T _A = 25°C			–40°C to 85°C		–40°C to 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3 V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
	I _{OH} = –24 mA	3 V	2.3			2.2		2		
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65 V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3 V	0.3			0.7		0.75		
	I _{OL} = 12 mA	2.7 V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3 V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3 V	5							pF