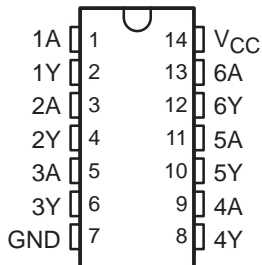


# SN54LVC04A, SN74LVC04A HEX INVERTERS

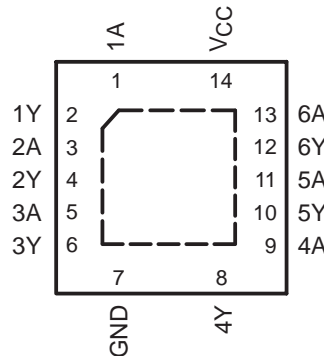
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- Operate From 1.65 V to 3.6 V
- Specified From  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.5 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

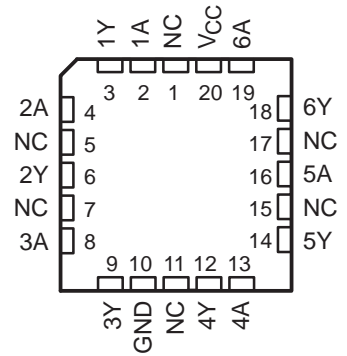
SN54LVC04A . . . J OR W PACKAGE  
SN74LVC04A . . . D, DB, DGV, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVC04A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVC04A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN54LVC04A hex inverter contains six independent inverters designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC04A hex inverter contains six independent inverters designed for 1.65-V to 3.6-V  $V_{CC}$  operation. The 'LVC04A devices perform the Boolean function  $Y = \bar{A}$ .

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	QFN – RGY	Reel of 1000	SN74LVC04ARGYR	LC04A
$-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – D	Tube of 50	SN74LVC04AD	LVC04A
		Reel of 2500	SN74LVC04ADR	
		Reel of 250	SN74LVC04ADT	
	SOP – NS	Reel of 2000	SN74LVC04ANSR	LVC04A
	SSOP – DB	Reel of 2000	SN74LVC04ADBR	LC04A
	TSSOP – PW	Tube of 90	SN74LVC04APW	LC04A
		Reel of 2000	SN74LVC04APWR	
Reel of 250		SN74LVC04APWT		
TVSOP – DGV	Reel of 2000	SN74LVC04ADGVR	LC04A	
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	CDIP – J	Tube of 25	SNJ54LVC04AJ	SNJ54LVC04AJ
	CFP – W	Tube of 150	SNJ54LVC04AW	SNJ54LVC04AW
	LCCC – FK	Tube of 55	SNJ54LVC04AFK	SNJ54LVC04AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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# SN54LVC04A, SN74LVC04A HEX INVERTERS

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## description/ordering information (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic diagram, each inverter (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	-50 mA
Continuous output current, $I_O$	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): DGV package	127°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C
Power dissipation, $P_{tot}$ ( $T_A = -40^\circ\text{C}$ to 125°C) (see Notes 5 and 6)	500 mW

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.
  5. For the D package: above 70°C, the value of  $P_{tot}$  derates linearly with 8 mW/K.
  6. For the DB, DGV, NS, and PW packages: above 60°C, the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

# SN54LVC04A, SN74LVC04A HEX INVERTERS

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## recommended operating conditions (see Note 7)

		SN54LVC04A		UNIT	
		-55 TO 125°C			
		MIN	MAX		
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		2	V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	V
V <sub>I</sub>	Input voltage	0	5.5		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V	-12		mA
		V <sub>CC</sub> = 3 V	-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V	12		mA
		V <sub>CC</sub> = 3 V	24		

NOTE 7: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## recommended operating conditions (see Note 7)

		SN74LVC04A						UNIT	
		T <sub>A</sub> = 25°C		-40 TO 85°C		-40 TO 125°C			
		MIN	MAX	MIN	MAX	MIN	MAX		
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65×V <sub>CC</sub>		0.65×V <sub>CC</sub>		0.65×V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35×V <sub>CC</sub>		0.35×V <sub>CC</sub>		0.35×V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		0.7		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		0.8		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V			-4		-4		mA
		V <sub>CC</sub> = 2.3 V			-8		-8		
		V <sub>CC</sub> = 2.7 V			-12		-12		
		V <sub>CC</sub> = 3 V			-24		-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V			4		4		mA
		V <sub>CC</sub> = 2.3 V			8		8		
		V <sub>CC</sub> = 2.7 V			12		12		
		V <sub>CC</sub> = 3 V			24		24		

NOTE 7: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVC04A, SN74LVC04A HEX INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC04A		UNIT
			-55 TO 125°C		
			MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	V <sub>CC</sub> -0.2		V
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		
	I <sub>OH</sub> = -24 mA	3 V	2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V	0.2		V
	I <sub>OL</sub> = 12 mA	2.7 V	0.4		
	I <sub>OL</sub> = 24 mA	3 V	0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V	±5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	10		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500		μA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN74LVC04A						UNIT	
			T <sub>A</sub> = 25°C			-40 TO 85°C		-40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.3		V
	I <sub>OH</sub> = -4 mA	1.65 V	1.29			1.2		1.05		
	I <sub>OH</sub> = -8 mA	2.3 V	1.9			1.7		1.55		
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
I <sub>OH</sub> = -24 mA	3 V	2.3			2.2		2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I <sub>OL</sub> = 4 mA	1.65 V	0.24			0.45		0.6		
	I <sub>OL</sub> = 8 mA	2.3 V	0.3			0.7		0.85		
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			0.4		0.6		
	I <sub>OL</sub> = 24 mA	3 V	0.55			0.55		0.8		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	1			10		40		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			500		5000		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5							pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC04A		UNIT
				-55 TO 125°C		
				MIN	MAX	
t <sub>pd</sub>	A	Y	2.7 V	5.5		ns
			3.3 V ± 0.3 V	0.5	4.5	



# SN54LVC04A, SN74LVC04A HEX INVERTERS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC04A						UNIT	
				T <sub>A</sub> = 25°C			-40 TO 85°C		-40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>pd</sub>	A	Y	1.8 V ± 0.15 V	1	4.1	7.5	1	8	1	9.5	ns
			2.5 V ± 0.2 V	1	3.6	7	1	7.5	1	9	
			2.7 V	1	3	5.3	1	5.5	1	7	
			3.3 V ± 0.3 V	1	2.5	4.3	1	4.5	1	6	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V					1	1.5	ns	

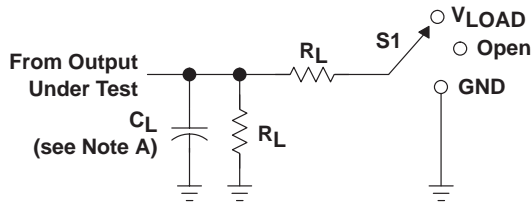
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	6	pF
			2.5 V	7	
			3.3 V	8	

# SN54LVC04A, SN74LVC04A HEX INVERTERS

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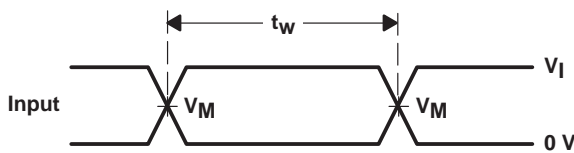
## PARAMETER MEASUREMENT INFORMATION



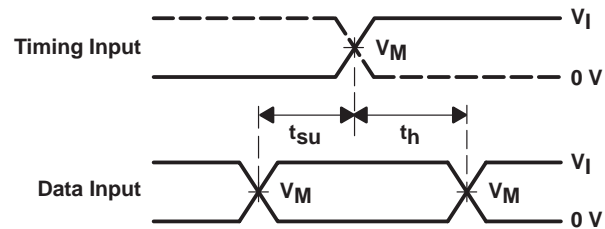
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	$GND$

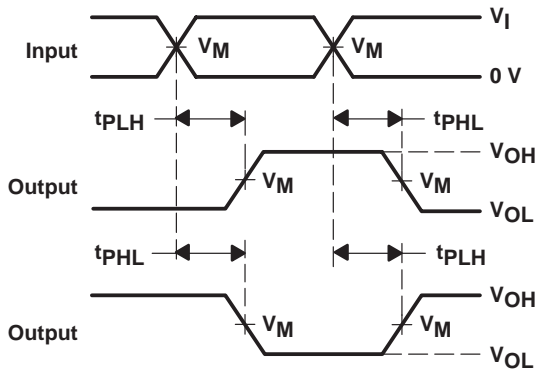
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8 V \pm 0.15 V$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



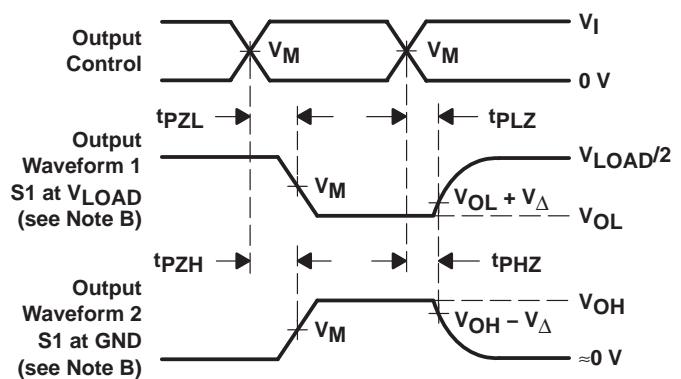
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

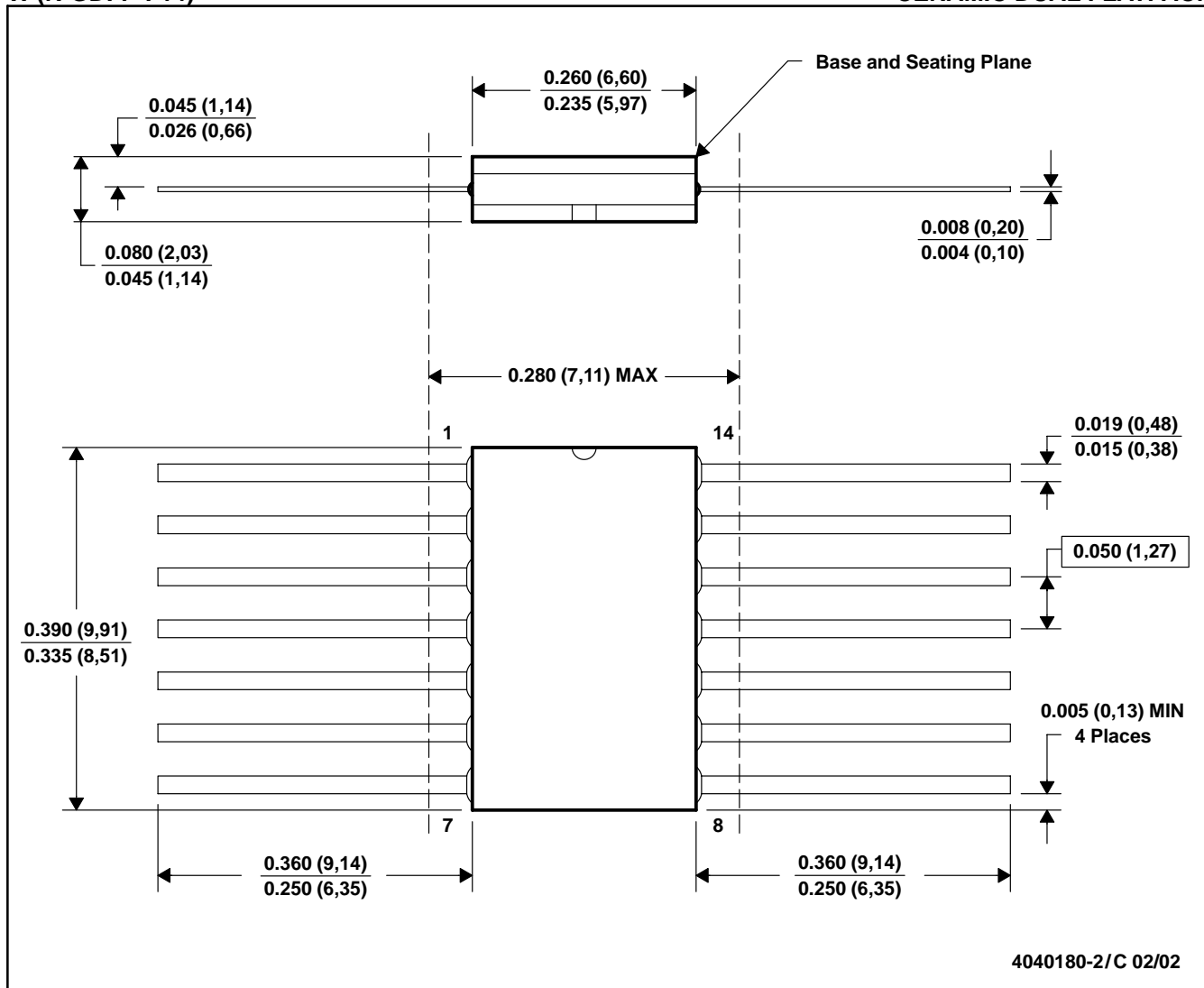
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

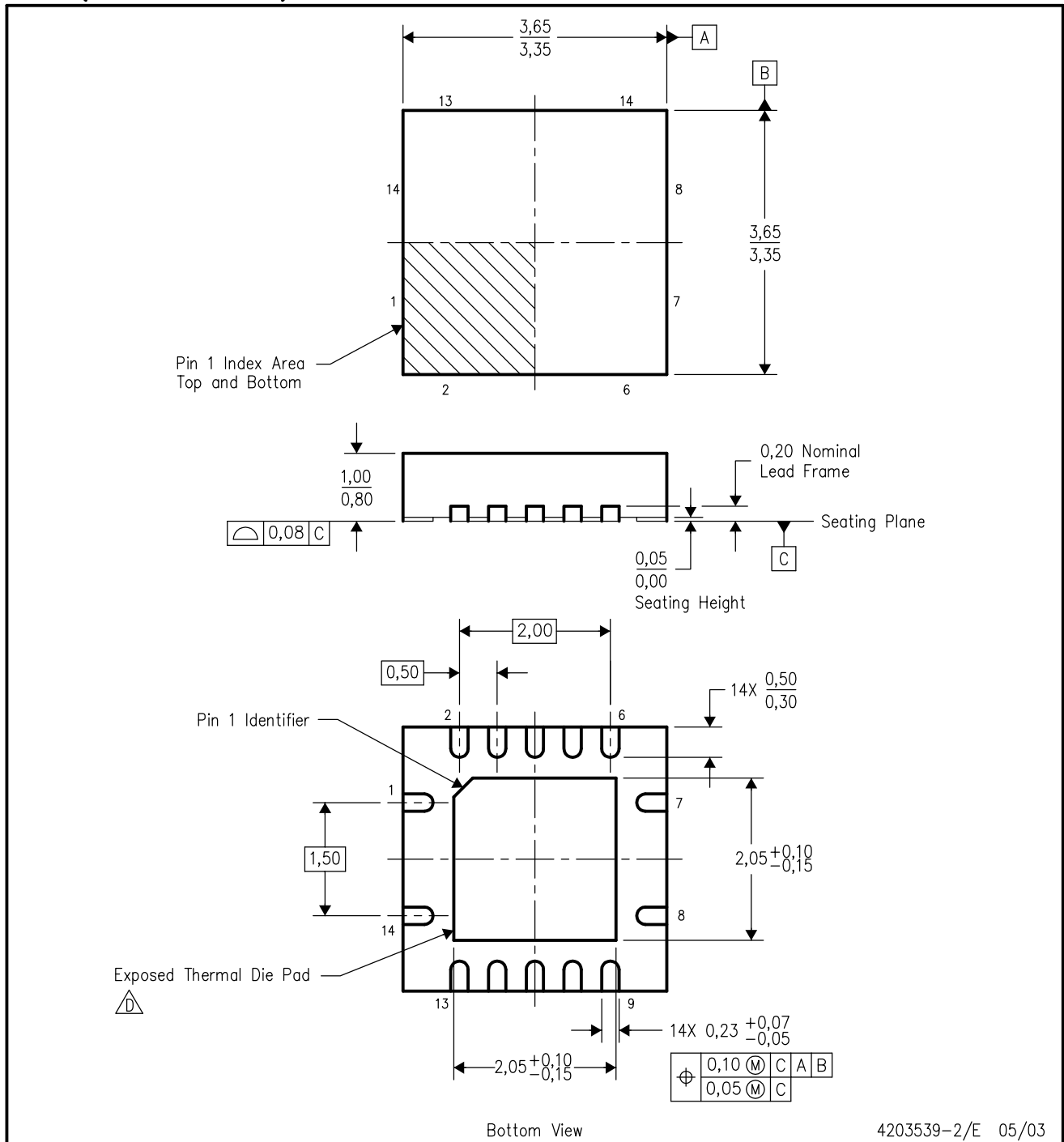
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194


RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

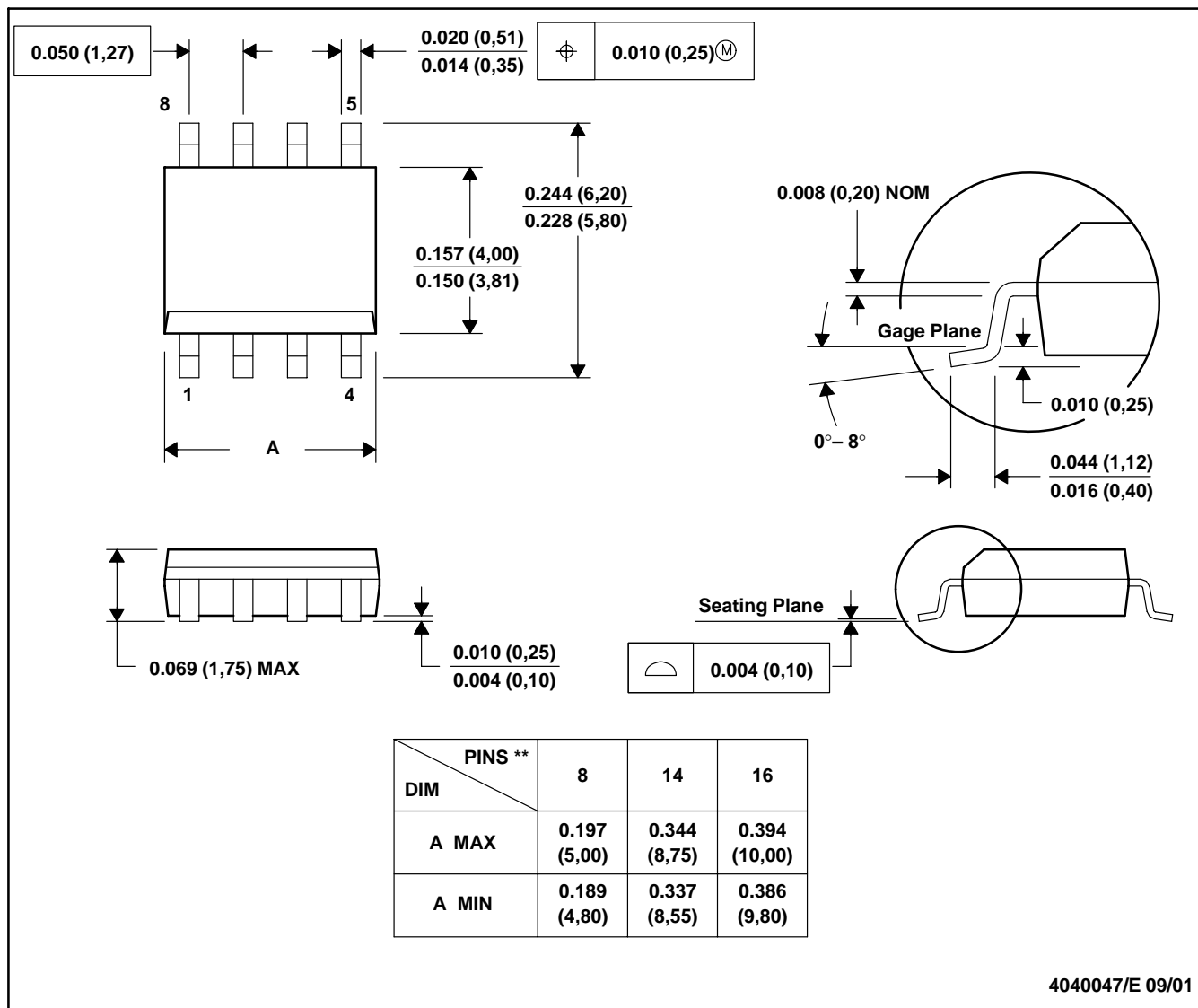
4203539-2/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BA.

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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