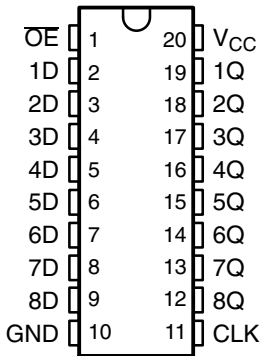


SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

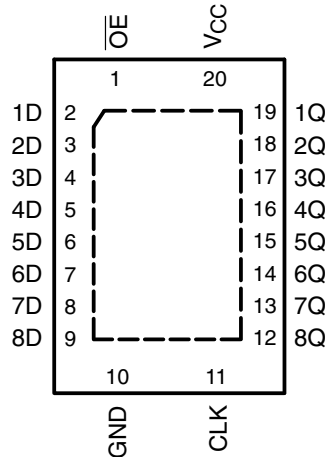
SCLS412I – APRIL 1998 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

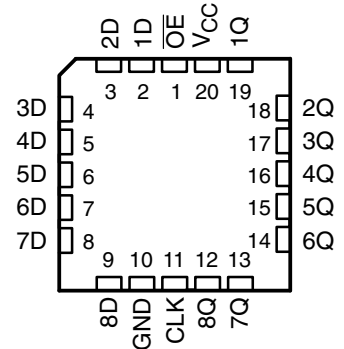
SN54LV574A . . . J OR W PACKAGE
SN74LV574A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV574A . . . RGY PACKAGE
(TOP VIEW)



SN54LV574A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV574ARGYR	LV574A
	SOIC – DW	Tube of 25	SN74LV574ADW	LV574A
		Reel of 2000	SN74LV574ADWR	
	SOP – NS	Reel of 2000	SN74LV574ANSR	74LV574A
	SSOP – DB	Reel of 2000	SN74LV574ADBR	LV574A
	TSSOP – PW	Tube of 70	SN74LV574APW	LV574A
		Reel of 2000	SN74LV574APWR	
		Reel of 250	SN74LV574APWT	
TVSOP – DGV	Reel of 2000	SN74LV574ADGVR	LV574A	
VFBGA – GQN	Reel of 1000	SN74LV574AGQNR	LV574A	
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV574AJ	SNJ54LV574AJ
	CFP – W	Tube of 85	SNJ54LV574AW	SNJ54LV574AW
	LCCC – FK	Tube of 55	SNJ54LV574AFK	SNJ54LV574AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412I – APRIL 1998 – REVISED APRIL 2005

description/ordering information (continued)

The 'LV574A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

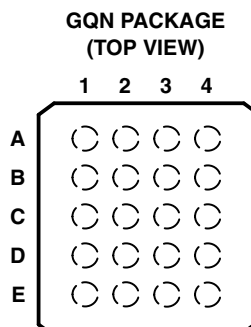
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.



terminal assignments

	1	2	3	4
A	1D	\overline{OE}	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

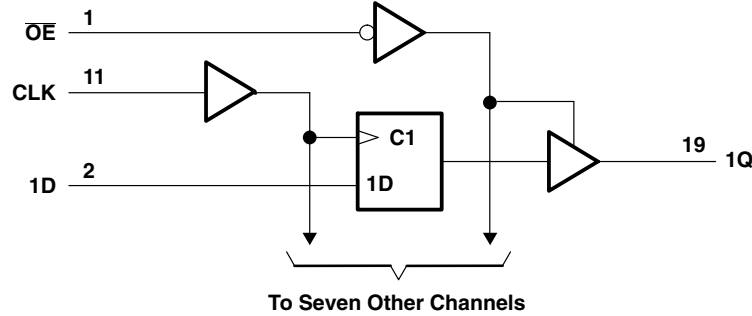
FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412I – APRIL 1998 – REVISED APRIL 2005

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412I – APRIL 1998 – REVISED APRIL 2005

recommended operating conditions (see Note 5)

		SN54LV574A		SN74LV574A		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	2	5.5	2	5.5	V	
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5		0.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$		$V_{CC} \times 0.3$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$		$V_{CC} \times 0.3$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$		$V_{CC} \times 0.3$		
V_I	Input voltage	0	5.5	0	5.5	V	
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$	-50		-50	μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-2		-2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	-8		-8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-16		-16		
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50		50	μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2		2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	8		8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16		16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200		200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	100		100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20		20		
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV574A			SN74LV574A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$		$V_{CC}-0.1$			V	
	$I_{OH} = -2\ \text{mA}$	2.3 V	2		2				
	$I_{OH} = -8\ \text{mA}$	3 V	2.48		2.48				
	$I_{OH} = -16\ \text{mA}$	4.5 V	3.8		3.8				
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V			0.1			V	
	$I_{OL} = 2\ \text{mA}$	2.3 V			0.4				
	$I_{OL} = 8\ \text{mA}$	3 V			0.44				
	$I_{OL} = 16\ \text{mA}$	4.5 V			0.55				
I_I	$V_I = 5.5\ \text{V or GND}$	0 to 5.5 V			± 1			μA	
I_{OZ}	$V_O = V_{CC}\ \text{or GND}$	5.5 V			± 5			μA	
I_{CC}	$V_I = V_{CC}\ \text{or GND, } I_O = 0$	5.5 V			20			μA	
I_{off}	$V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$	0			5			μA	
C_i	$V_I = V_{CC}\ \text{or GND}$	3.3 V	1.8		1.8			pF	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412I – APRIL 1998 – REVISED APRIL 2005

timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7		7		7		ns
t_{su}	Setup time	High or low before CLK \uparrow	5.5		5.5		5.5		ns
t_h	Hold time	Data after CLK \uparrow	2		2		2		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
t_{su}	Setup time	High or low before CLK \uparrow	3.5		3.5		3.5		ns
t_h	Hold time	Data after CLK \uparrow	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV574A		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		5		ns
t_{su}	Setup time	High or low before CLK \uparrow	3.5		3.5		3.5		ns
t_h	Hold time	Data after CLK \uparrow	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV574A		SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	60*	100*		50*		50	MHz	
			$C_L = 50\text{ pF}$	50	85		40		40		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$	9.6*	16.6*		1*	20*	1	20	ns
t_{en}	\overline{OE}	Q		9.2*	16.1*		1*	19*	1	19	
t_{dis}	\overline{OE}	Q		6.5*	12.8*		1*	15*	1	15	
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	11.6	19.6		1	23	1	23	ns
t_{en}	\overline{OE}	Q		10.9	19		1	22	1	22	
t_{dis}	\overline{OE}	Q		8.4	17.5		1	20	1	20	
$t_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS412I – APRIL 1998 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV574A		SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	80*	145*		65*		65		MHz
			$C_L = 50 \text{ pF}$	50	120		45		45		
t_{pd}	CLK	Q	$C_L = 15 \text{ pF}$		6.8*	13.2*	1*	15.5*	1	15.5	ns
t_{en}	\overline{OE}	Q			6.4*	12.8*	1*	15*	1	15	
t_{dis}	\overline{OE}	Q			4.8*	13*	1*	15*	1	15	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$		8.1	16.7			19	19	ns
t_{en}	\overline{OE}	Q			7.7	16.3	1	18.5	1	18.5	
t_{dis}	\overline{OE}	Q			6.1	15	1	17	1	17	
$t_{sk(o)}$							1.5			1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV574A		SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	130*	205*		110*		110		MHz
			$C_L = 50 \text{ pF}$	85	175		75		75		
t_{pd}	CLK	Q	$C_L = 15 \text{ pF}$		4.8*	8.6*	1*	10*	1	10	ns
t_{en}	\overline{OE}	Q			4.6*	9*	1*	10.5*	1	10.5	
t_{dis}	\overline{OE}	Q			3.5*	9*	1*	10.5*	1	10.5	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$		5.7	10.6			12	12	ns
t_{en}	\overline{OE}	Q			5.5	11	1	12.5	1	12.5	
t_{dis}	\overline{OE}	Q			4.1	10.1	1	11.5	1	11.5	
$t_{sk(o)}$							1			1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ C$ (see Note 6)

PARAMETER		SN74LV574A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.6	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	20.4	pF
				5 V	23.8	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

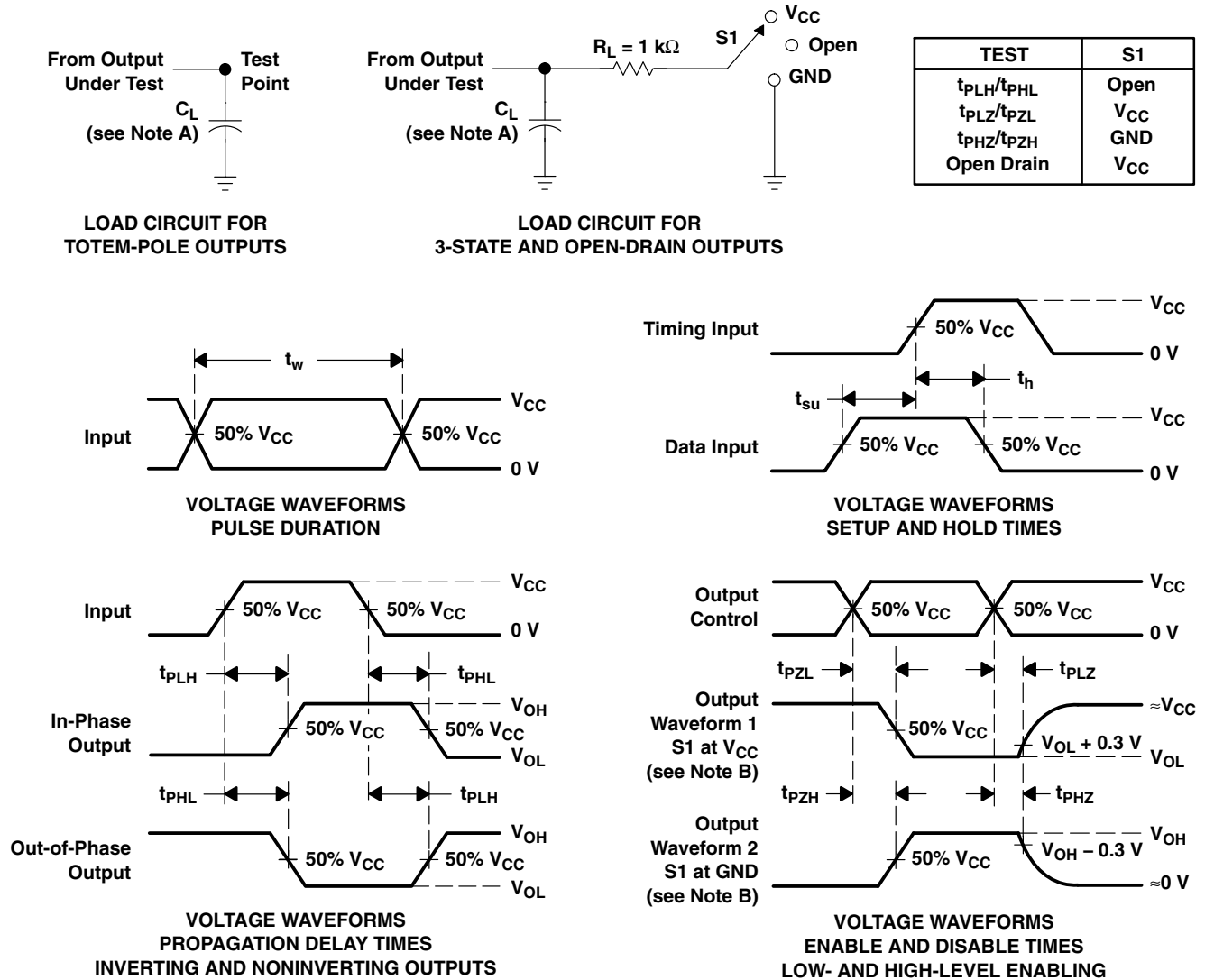


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS4121 – APRIL 1998 – REVISED APRIL 2005

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV574ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV574A	Samples
SN74LV574APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV574A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV574ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV574ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV574APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV574ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV574ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV574ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV574APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV574APWT	TSSOP	PW	20	250	356.0	356.0	35.0
SN74LV574ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV574ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LV574APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LV574APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

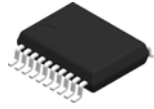
PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

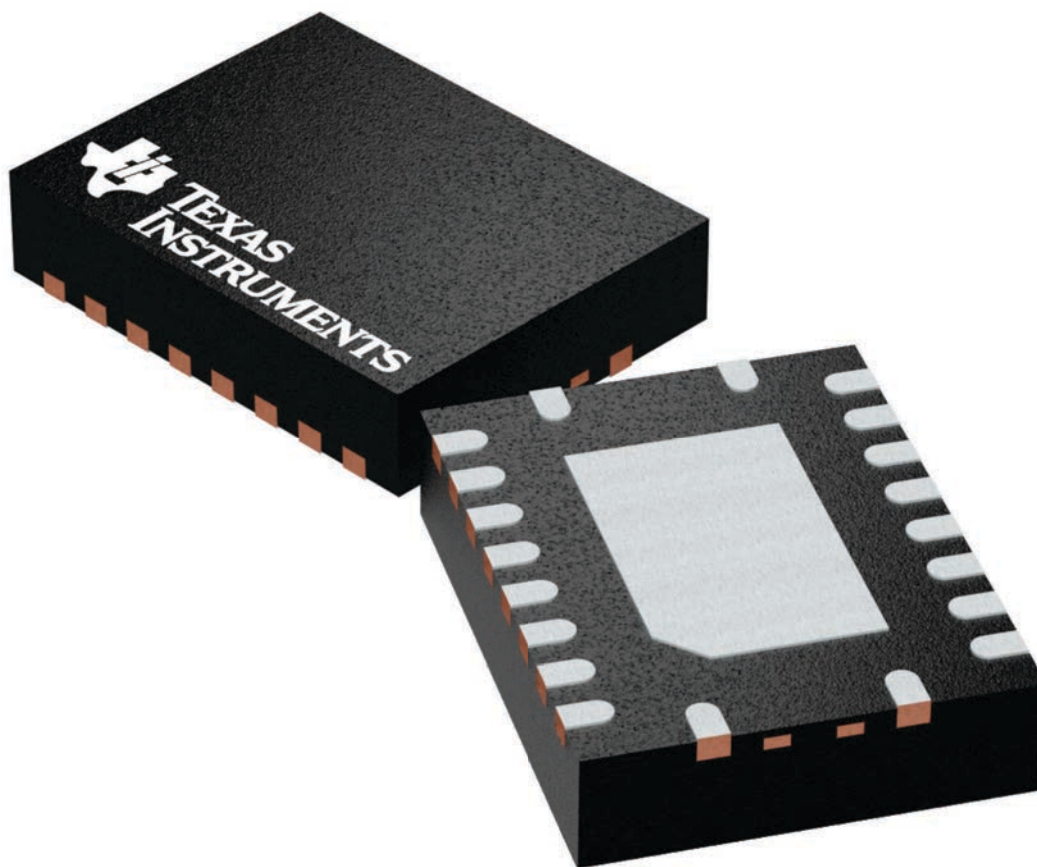
RGY 20

VQFN - 1 mm max height

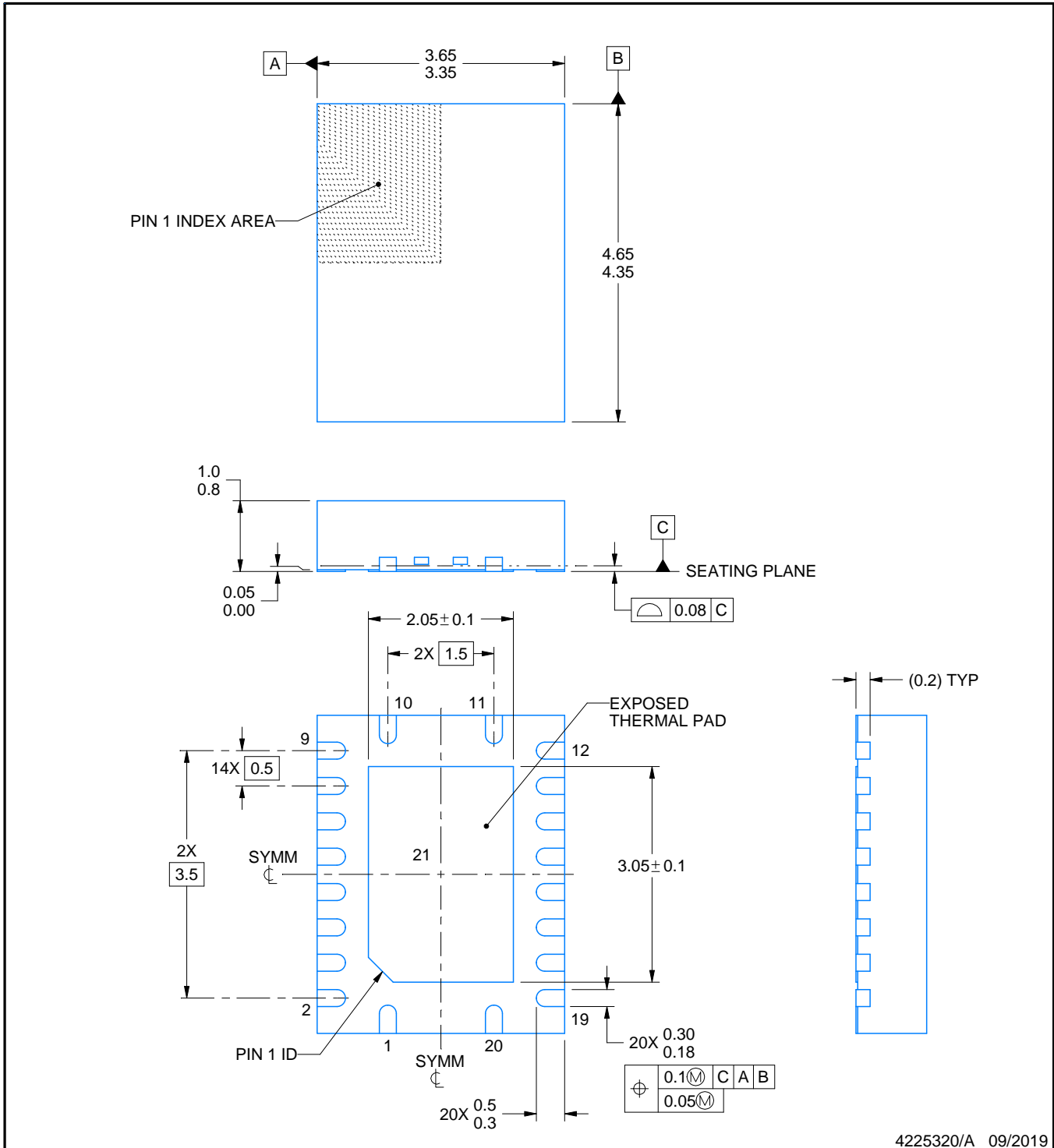
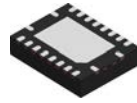
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

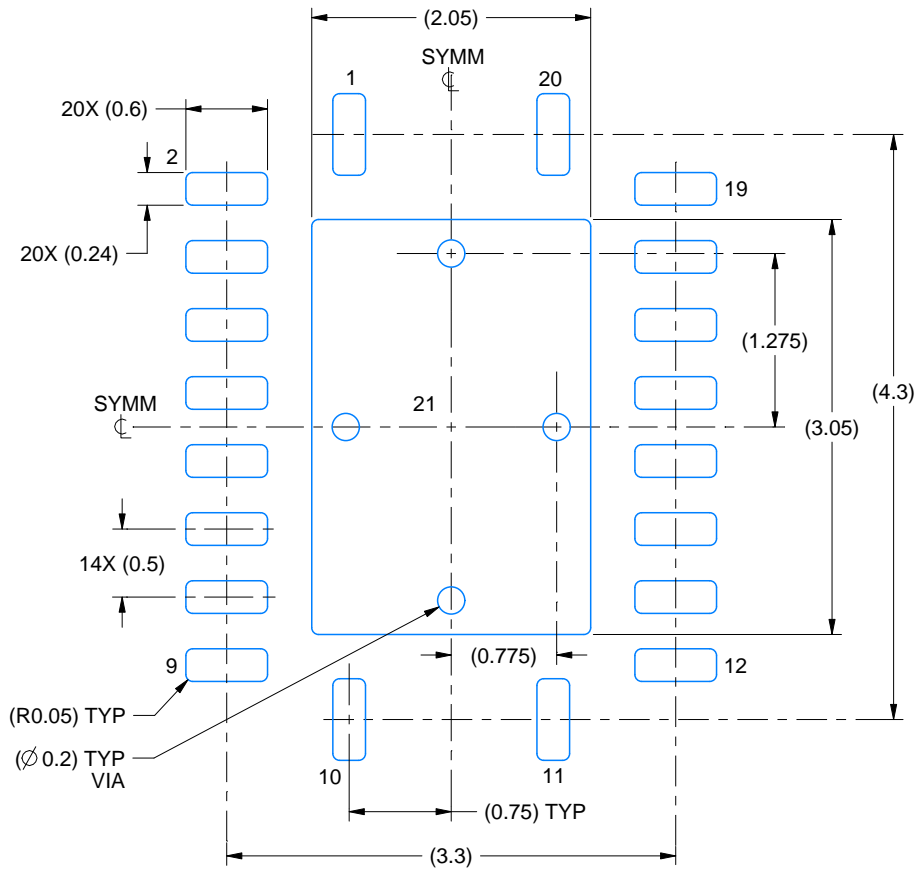
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

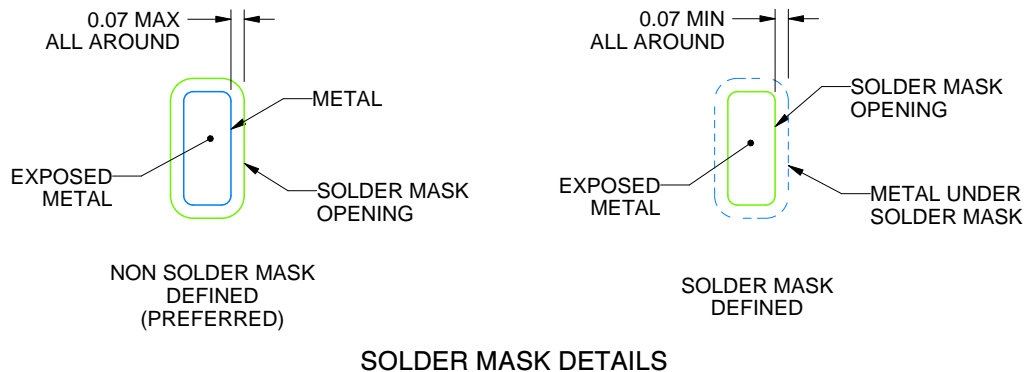
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

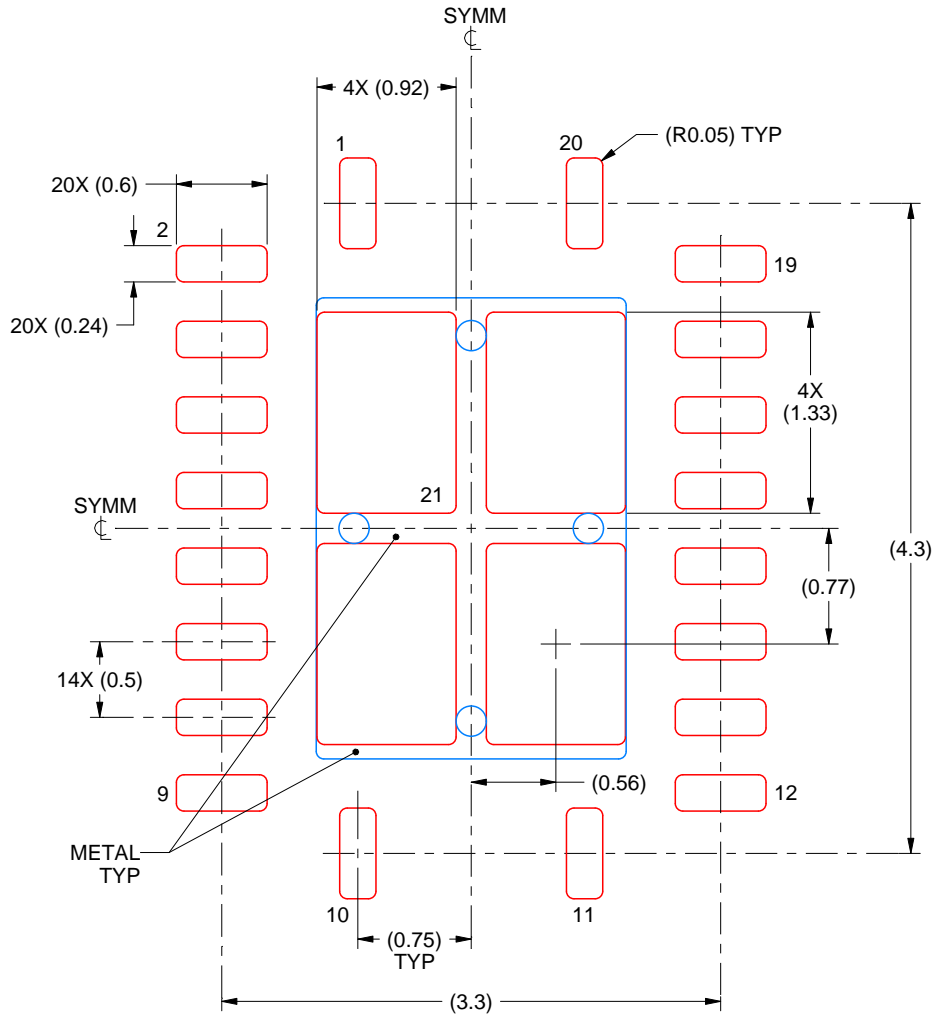
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

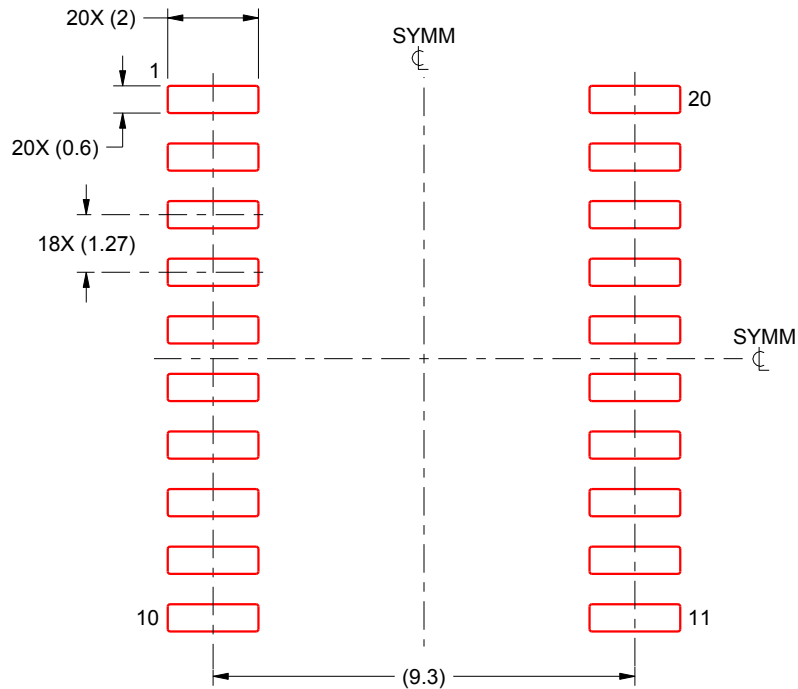
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated