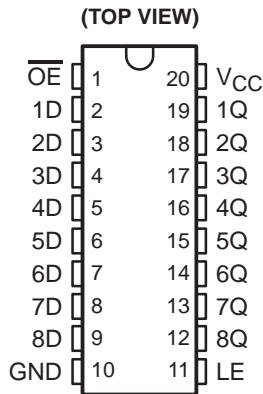


# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

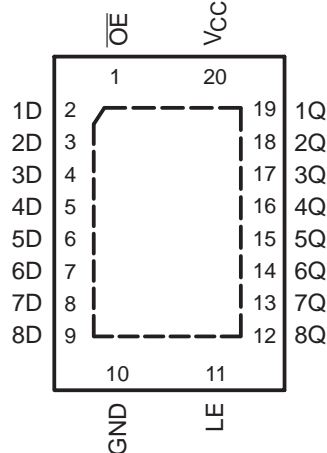
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 8 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

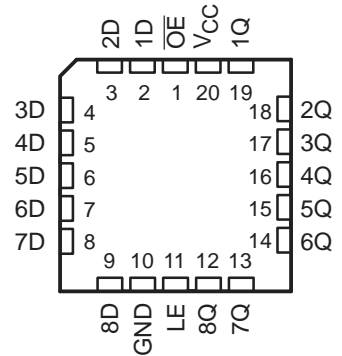
SN54LV573A . . . J OR W PACKAGE  
SN74LV573A . . . DB, DGV, DW, NS,  
OR PW PACKAGE



SN74LV573A . . . RGY PACKAGE  
(TOP VIEW)



SN54LV573A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV573ARGYR	LV573A
	SOIC – DW	Tube of 25	SN74LV573ADW	LV573A
		Reel of 2000	SN74LV573ADWR	
	SOP – NS	Reel of 2000	SN74LV573ANSR	74LV573A
	SSOP – DB	Reel of 2000	SN74LV573ADBR	LV573A
	TSSOP – PW	Tube of 70	SN74LV573APW	LV573A
		Reel of 2000	SN74LV573APWR	
		Reel of 250	SN74LV573APWT	
TVSOP – DGV	Reel of 2000	SN74LV573ADGVR	LV573A	
VFBGA – GQN	Reel of 1000	SN74LV573AGQNR	LV573A	
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV573AJ	SNJ54LV573AJ
	CFP – W	Tube of 85	SNJ54LV573AW	SNJ54LV573AW
	LCCC – FK	Tube of 55	SNJ54LV573AFK	SNJ54LV573AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

The 'LV573A devices are octal transparent D-type latches designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

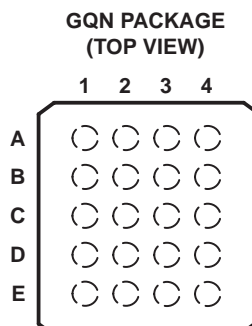
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



## terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	$V_{CC}$	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	LE	8Q

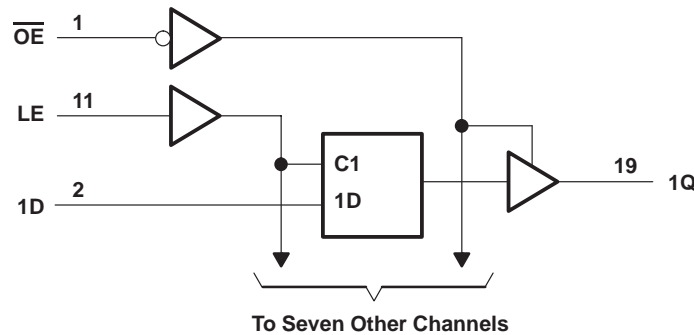
## FUNCTION TABLE (each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**SN54LV573A, SN74LV573A**  
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**logic diagram (positive logic)**



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range applied in the high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±35 mA
Continuous current through $V_{CC}$ or GND .....	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	70°C/W
(see Note 3): DGV package .....	92°C/W
(see Note 3): DW package .....	58°C/W
(see Note 3): GQN package .....	78°C/W
(see Note 3): NS package .....	60°C/W
(see Note 3): PW package .....	83°C/W
(see Note 4): RGY package .....	37°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.  
4. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 5)

		SN54LV573A		SN74LV573A		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5		0.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$		$V_{CC} \times 0.3$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$		$V_{CC} \times 0.3$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$		$V_{CC} \times 0.3$		
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	0	$V_{CC}$	V
		3-state	0	5.5	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	-50		-50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-2		-2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	-8		-8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-16		-16		
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50		50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2		2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	8		8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	16		16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200		200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	100		100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20		20		
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	SN54LV573A			SN74LV573A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			2			
	$I_{OH} = -8\ \text{mA}$	3 V	2.48			2.48			
	$I_{OH} = -16\ \text{mA}$	4.5 V	3.8			3.8			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V	0.1			0.1			V
	$I_{OL} = 2\ \text{mA}$	2.3 V	0.4			0.4			
	$I_{OL} = 8\ \text{mA}$	3 V	0.44			0.44			
	$I_{OL} = 16\ \text{mA}$	4.5 V	0.55			0.55			
$I_I$	$V_I = 5.5\ \text{V or GND}$	0 to 5.5 V	$\pm 1$			$\pm 1$			$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}\ \text{or GND}$	5.5 V	$\pm 5$			$\pm 5$			$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}\ \text{or GND, } I_O = 0$	5.5 V	20			20			$\mu\text{A}$
$I_{off}$	$V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$	0	5			5			$\mu\text{A}$
$C_i$	$V_I = V_{CC}\ \text{or GND}$	3.3 V	1.8			1.8			pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**SN54LV573A, SN74LV573A**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	LE high	6.5		6.5		6.5		ns
$t_{su}$	Setup time	Data before LE↓	5		5		5		ns
$t_h$	Hold time	Data after LE↓	2		2		2		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	LE high	5		5		5		ns
$t_{su}$	Setup time	Data before LE↓	3.5		3.5		3.5		ns
$t_h$	Hold time	Data after LE↓	1.5		1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	LE high	5		5		5		ns
$t_{su}$	Setup time	Data before LE↓	3.5		3.5		3.5		ns
$t_h$	Hold time	Data after LE↓	1.5		1.5		1.5		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	8.9*	15.8*		1*	18*	1	18	ns		
	LE	Q		9.6*	16.2*		1*	19*	1	19			
$t_{en}$	$\overline{OE}$	Q		9.3*	16.2*		1*	19*	1	19			
$t_{dis}$	$\overline{OE}$	Q		6.7*	12.6*		1*	15*	1	15			
$t_{pd}$	D	Q		$C_L = 50\text{ pF}$	10.9	18.7		1	21	1		21	ns
	LE	Q			11.6	19.1		1	23	1		23	
$t_{en}$	$\overline{OE}$	Q	11.4		19		1	22	1	22			
$t_{dis}$	$\overline{OE}$	Q	8.6		17.3		1	19	1	19			
$t_{sk(o)}$						2				2			

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	6.2*	11*	1*	13*	1	13	ns		
	LE	Q		6.8*	11.9*	1*	14*	1	14			
$t_{en}$	$\overline{OE}$	Q		6.6*	11.5*	1*	13.5*	1	13.5			
$t_{dis}$	$\overline{OE}$	Q		4.9*	11*	1*	13*	1	13			
$t_{pd}$	D	Q		$C_L = 50\text{ pF}$	7.7	14.5	1	16.5	1		16.5	ns
	LE	Q			8.2	15.4	1	17.5	1		17.5	
$t_{en}$	$\overline{OE}$	Q	8		15	1	17	1	17			
$t_{dis}$	$\overline{OE}$	Q	6.2		14.5	1	16.5	1	16.5			
$t_{sk(o)}$						1.5			1.5			

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	4.3*	6.8*	1*	8*	1	8	ns		
	LE	Q		4.7*	7.7*	1*	9*	1	9			
$t_{en}$	$\overline{OE}$	Q		4.7*	7.7*	1*	9*	1	9			
$t_{dis}$	$\overline{OE}$	Q		3.5*	7.7*	1*	9*	1	9			
$t_{pd}$	D	Q		$C_L = 50\text{ pF}$	5.3	8.8	1	10	1		10	ns
	LE	Q			5.7	9.7	1	11	1		11	
$t_{en}$	$\overline{OE}$	Q	5.7		9.7	1	11	1	11			
$t_{dis}$	$\overline{OE}$	Q	4.2		9.7	1	11	1	11			
$t_{sk(o)}$						1			1			

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)

PARAMETER		SN74LV573A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.5	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

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**SN54LV573A, SN74LV573A**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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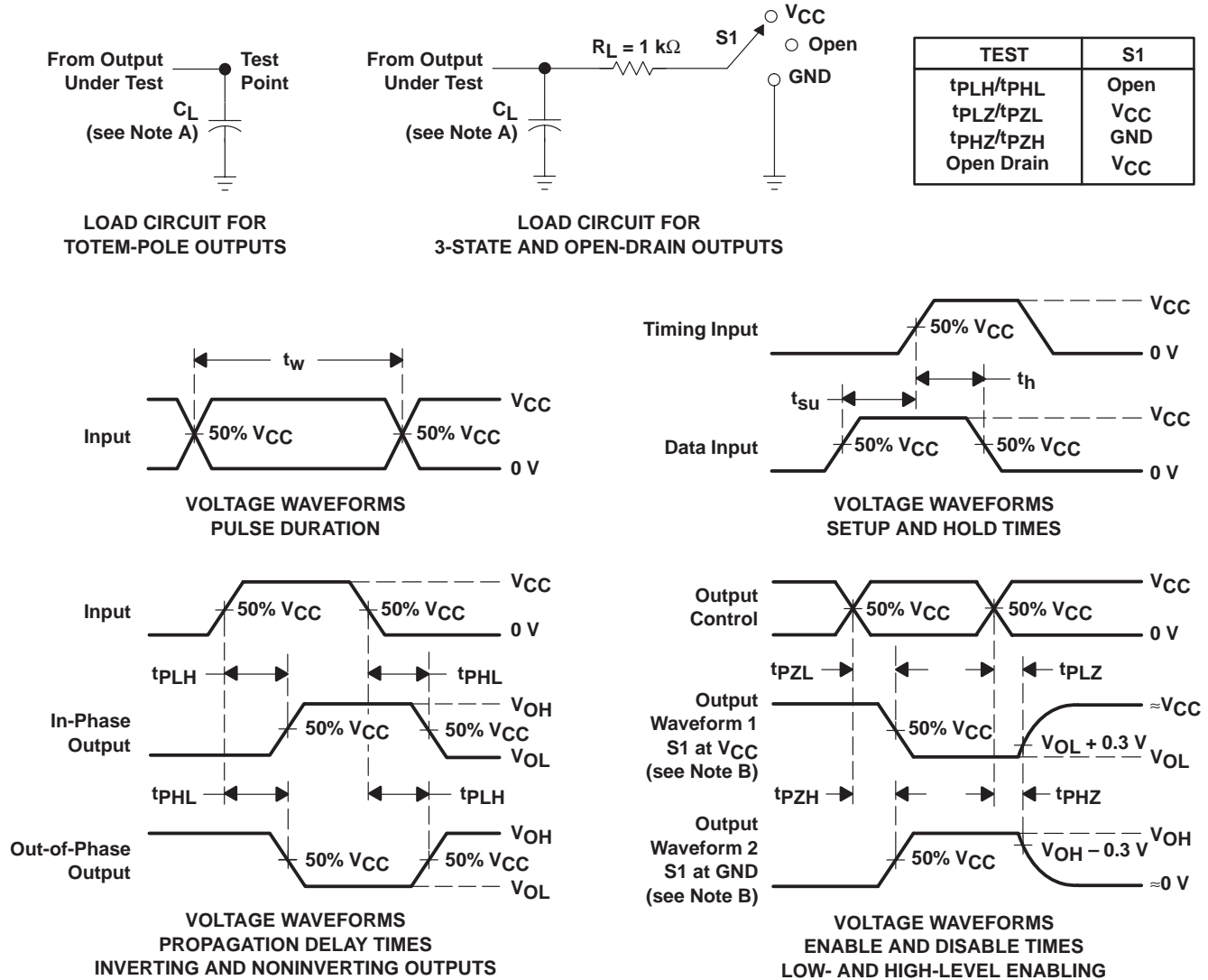
**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 50 pF, f = 10 MHz	3.3 V	16	pF
				5 V	18	
		D to Q		3.3 V	18.2	
				5 V	21.3	
	LE to Q					

# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

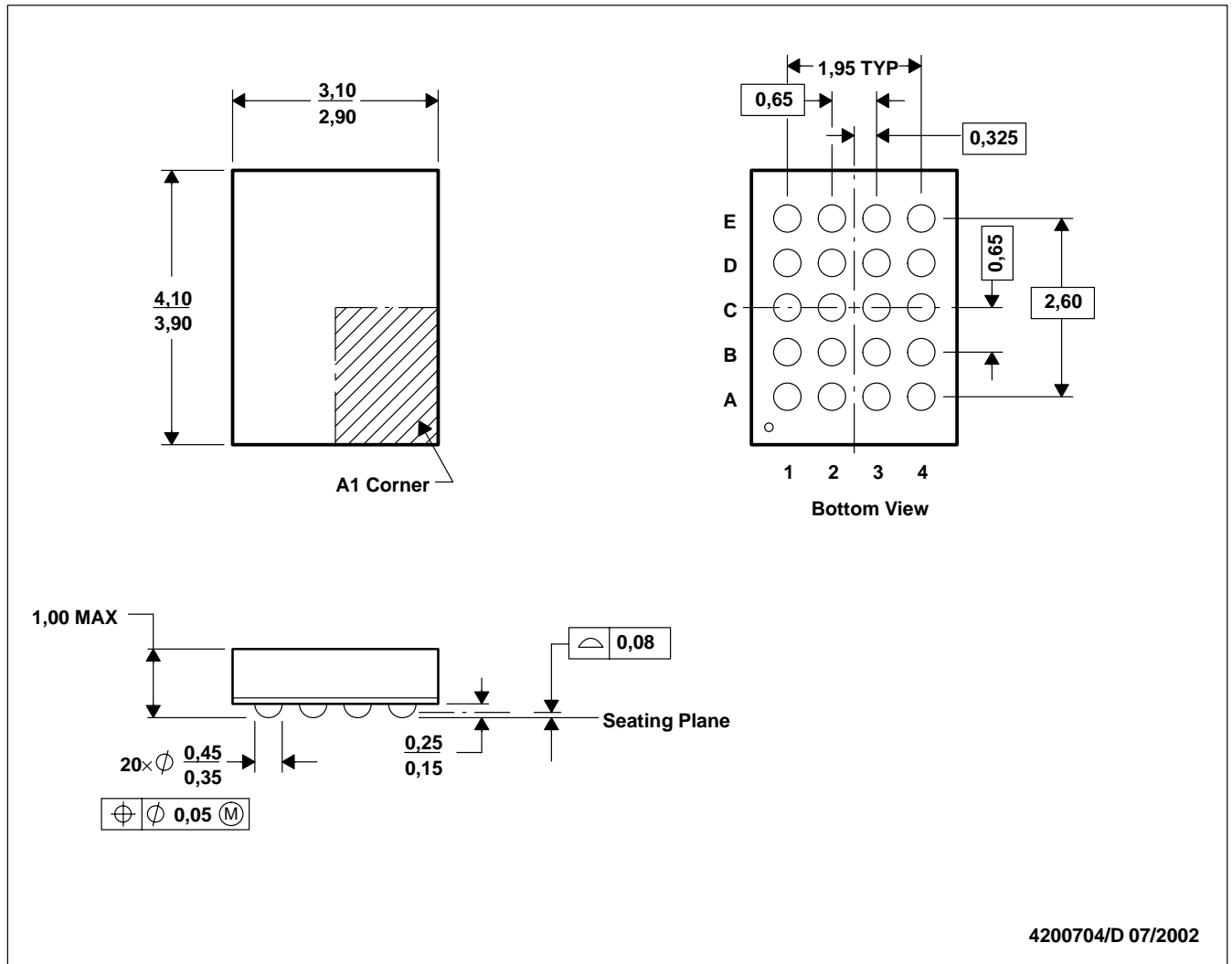


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - MicroStar Junior™ configuration
  - Falls within JEDEC MO-225 variation BC.
  - This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

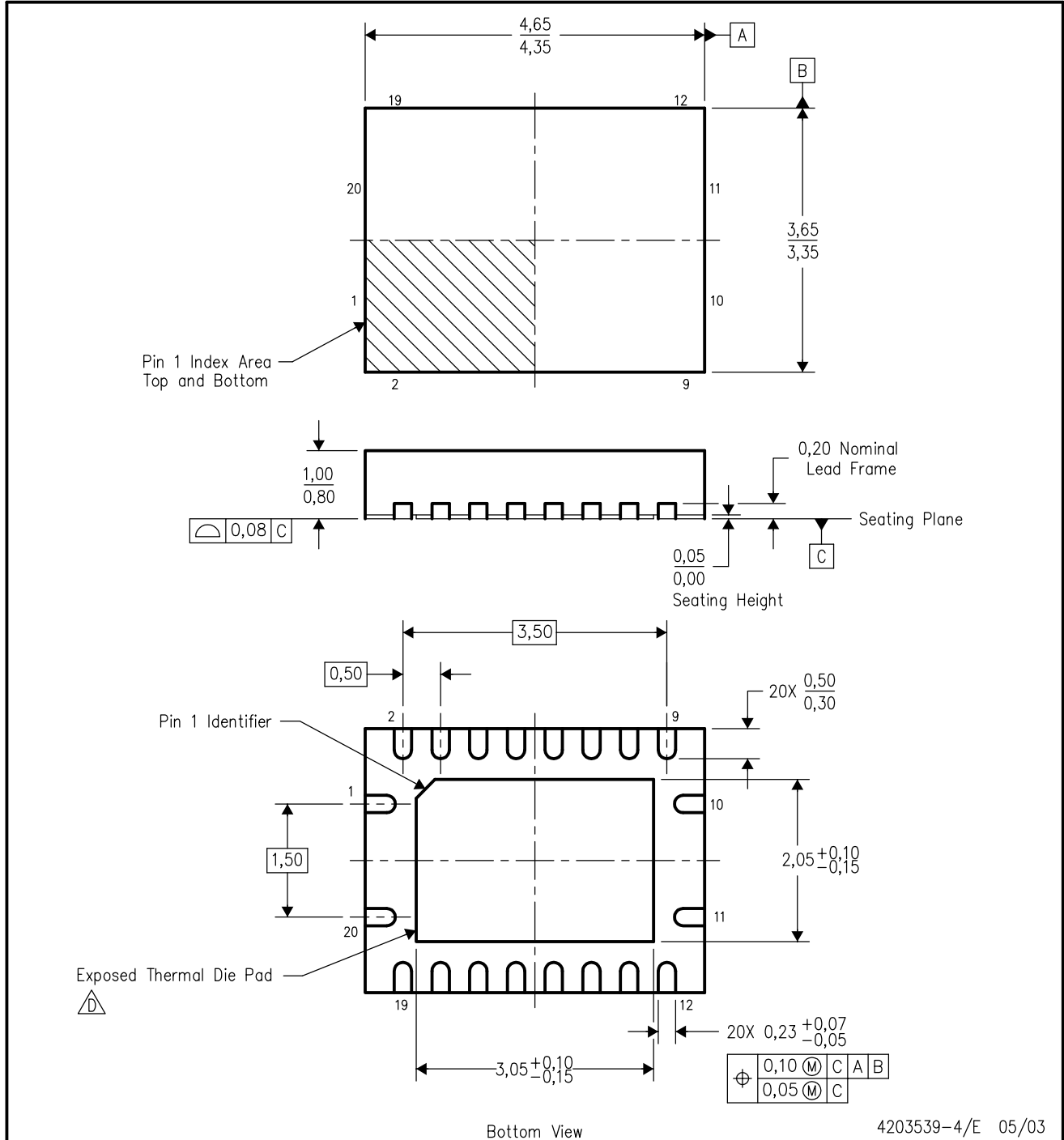


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194


RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



Bottom View

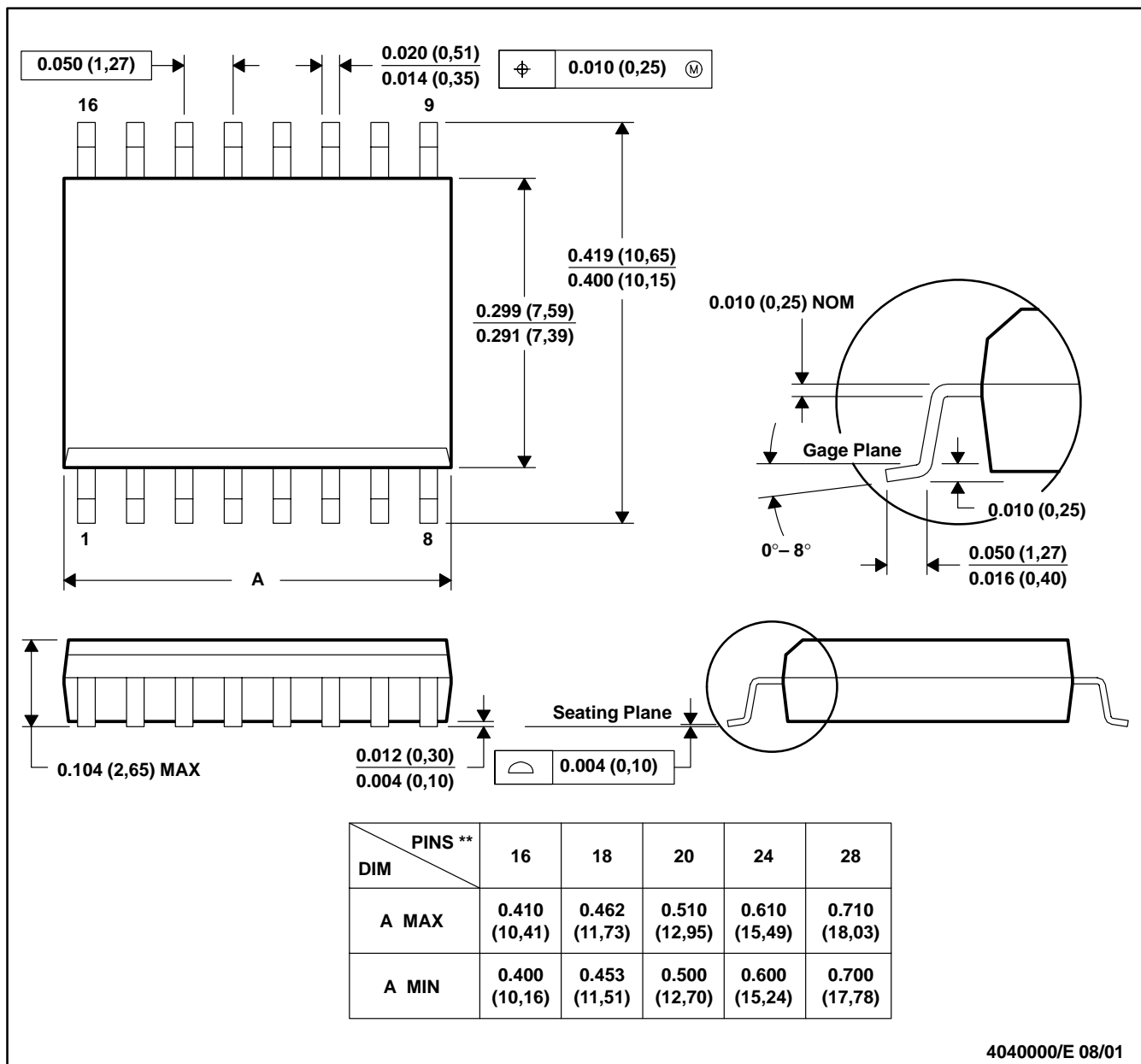
4203539-4/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

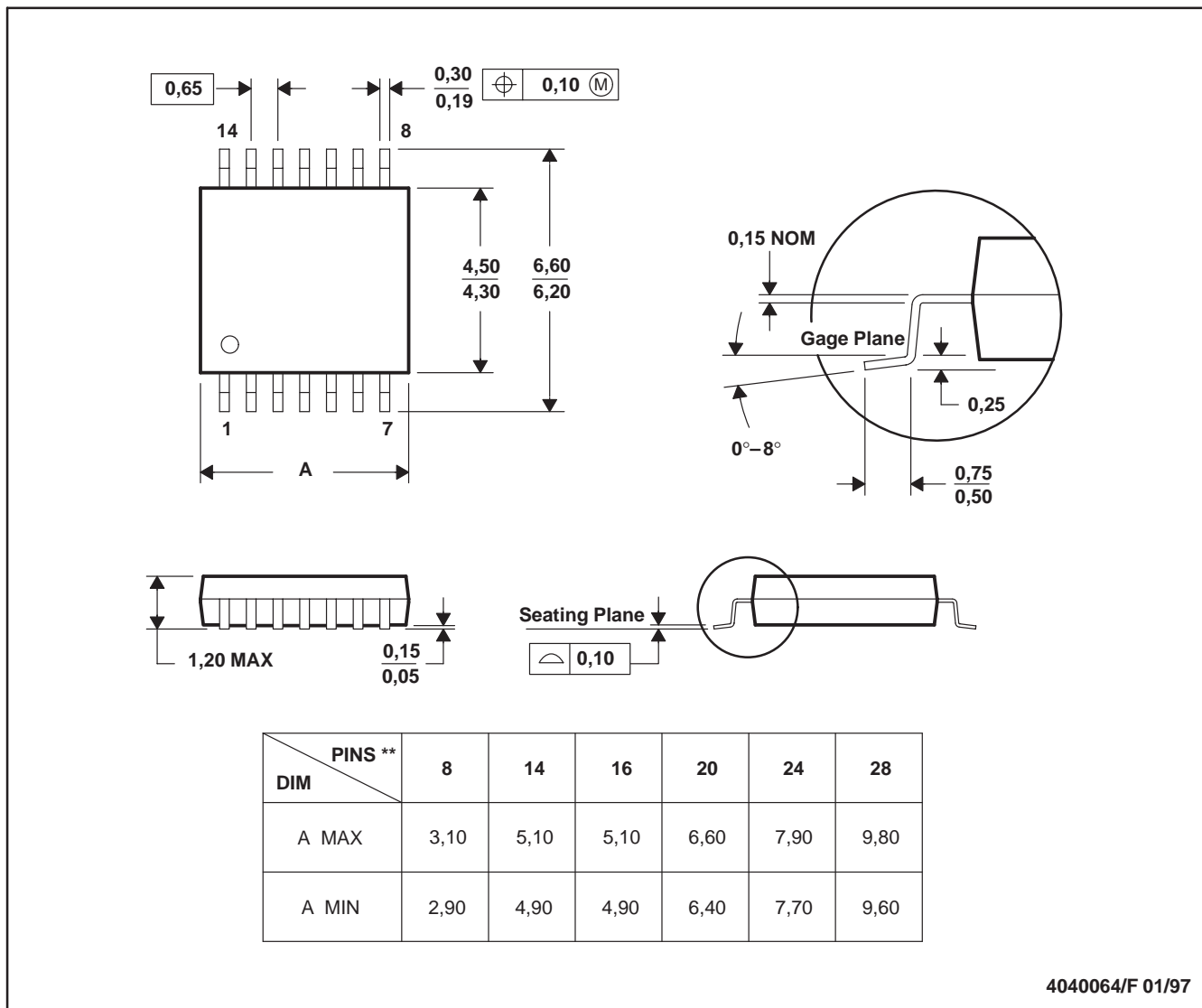


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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