

SN54LV4066A, SN74LV4066A QUADRUPLE BILATERAL ANALOG SWITCHES

SCLS427G – APRIL 1999 – REVISED AUGUST 2003

- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

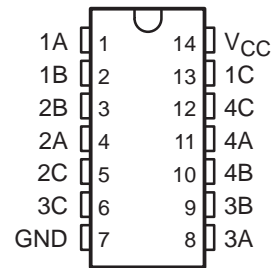
This quadruple silicon-gate CMOS analog switch is designed for 2-V to 5.5-V V_{CC} operation.

These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

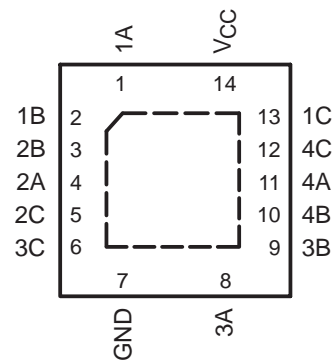
Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

SN54LV4066A . . . J OR W PACKAGE
SN74LV4066A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV4066A . . . RGY PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74LV4066AN	SN74LV4066AN
	QFN – RGY	Reel of 1000	SN74LV4066ARGYR	LW066A
	SOIC – D	Tube of 50	SN74LV4066AD	LV4066A
		Reel of 2500	SN74LV4066ADR	
	SOP – NS	Reel of 2000	SN74LV4066ANSR	74LV4066A
	SSOP – DB	Reel of 2000	SN74LV4066ADBR	LW066A
	TSSOP – PW	Tube of 90	SN74LV4066APW	LW066A
		Reel of 2000	SN74LV4066APWR	
Reel of 250		SN74LV4066APWT		
TVSOP – DGV	Reel of 2000	SN74LV4066ADGVR	LW066A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4066AJ	SNJ54LV4066AJ
	CFP – W	Tube of 150	SNJ54LV4066AW	SNJ54LV4066AW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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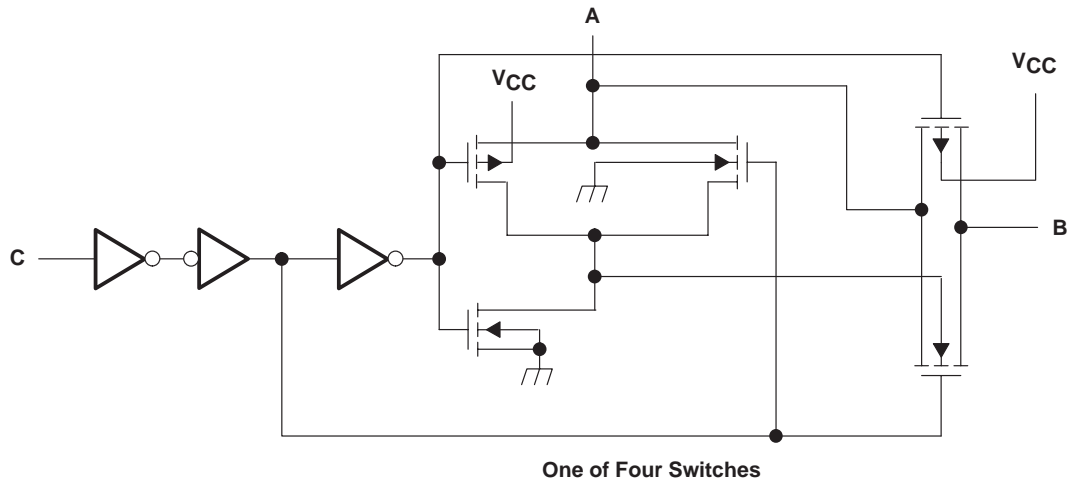
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FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Control-input clamp current, I_{IK} ($V_I < 0$)	-20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)	± 50 mA
On-state switch current, I_T ($V_{IO} = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): DGV package	127°C/W
(see Note 3): N package	80°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

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recommended operating conditions (see Note 5)

		SN54LV4066A		SN74LV4066A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2†	5.5	2†	5.5	V
V _{IH}	High-level input voltage, control inputs	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage, control inputs	V _{CC} = 2 V		0.5	0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	V _{CC} × 0.3	
V _I	Control input voltage	0	5.5	0	5.5	V
V _{IO}	Input/output voltage	0	V _{CC}	0	V _{CC}	V
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	200	ns/V
		V _{CC} = 3 V to 3.6 V		100	100	
		V _{CC} = 4.5 V to 5.5 V		20	20	
T _A	Operating free-air temperature	–55	125	–40	85	°C

† With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV4066A		SN74LV4066A		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
r _{on} On-state switch resistance	I _T = -1 mA, V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 1)	2.3 V		38	180		225		225	Ω	
		3 V		29	150		190		190		
		4.5 V		21	75		100		100		
r _{on(p)} Peak on-state resistance	I _T = -1 mA, V _I = V _{CC} to GND, V _C = V _{IH}	2.3 V		143	500		600		600	Ω	
		3 V		57	180		225		225		
		4.5 V		31	100		125		125		
Δr _{on} Difference in on-state resistance between switches	I _T = -1 mA, V _I = V _{CC} to GND, V _C = V _{IH}	2.3 V		6	30		40		40	Ω	
		3 V		3	20		30		30		
		4.5 V		2	15		20		20		
I _I Control input current	V _I = 5.5 V or GND	0 to 5.5 V					±0.1		±1	±1	μA
I _{S(off)} Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 2)	5.5 V					±0.1		±1	±1	μA
I _{S(on)} On-state switch leakage current	V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 3)	5.5 V					±0.1		±1	±1	μA
I _{CC} Supply current	V _I = V _{CC} or GND	5.5 V							20	20	μA
C _{ic} Control input capacitance				1.5							pF
C _{io} Switch input/output capacitance				5.5							pF
C _F Feed-through capacitance				0.5							pF

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4066A		SN74LV4066A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagat ion delay time	A or B	B or A	C _L = 15 pF, (see Figure 4)		1.2	10		16		16	ns
t _{PZH} t _{PZL}	Switch turn-on time	C	A or B	C _L = 15 pF, R _L = 1 kΩ (see Figure 5)		3.3	15		20		20	ns
t _{PLZ} t _{PHZ}	Switch turn-off time	C	A or B	C _L = 15 pF, R _L = 1 kΩ (see Figure 5)		6	15		23		23	ns
t _{PLH} t _{PHL}	Propagat ion delay time	A or B	B or A	C _L = 50 pF, (see Figure 4)		2.6	12		18		18	ns
t _{PZH} t _{PZL}	Switch turn-on time	C	A or B	C _L = 50 pF, R _L = 1 kΩ (see Figure 5)		4.2	25		32		32	ns
t _{PLZ} t _{PHZ}	Switch turn-off time	C	A or B	C _L = 50 pF, R _L = 1 kΩ (see Figure 5)		9.6	25		32		32	ns

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T _A = 25°C			SN54LV4066A		SN74LV4066A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagat ion delay time	A or B	B or A	C _L = 15 pF, (see Figure 4)		0.8	6		10		10	ns
t _{PZH} t _{PZL}	Switch turn-on time	C	A or B	C _L = 15 pF, R _L = 1 kΩ (see Figure 5)		2.3	11		15		15	ns
t _{PLZ} t _{PHZ}	Switch turn-off time	C	A or B	C _L = 15 pF, R _L = 1 kΩ (see Figure 5)		4.5	11		15		15	ns
t _{PLH} t _{PHL}	Propagat ion delay time	A or B	B or A	C _L = 50 pF, (see Figure 4)		1.5	9		12		12	ns
t _{PZH} t _{PZL}	Switch turn-on time	C	A or B	C _L = 50 pF, R _L = 1 kΩ (see Figure 5)		3	18		22		22	ns
t _{PLZ} t _{PHZ}	Switch turn-off time	C	A or B	C _L = 50 pF, R _L = 1 kΩ (see Figure 5)		7.2	18		22		22	ns

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV4066A		SN74LV4066A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH tPHL Propagation delay time	A or B	B or A	$C_L = 15\text{ pF}$, (see Figure 4)	0.3	4		7		7	ns	
tPZH tPZL Switch turn-on time	C	A or B	$C_L = 15\text{ pF}$, $R_L = 1\text{ k}\Omega$ (see Figure 5)	1.6	7		10		10	ns	
tPLZ tPHZ Switch turn-off time	C	A or B	$C_L = 15\text{ pF}$, $R_L = 1\text{ k}\Omega$ (see Figure 5)	3.2	7		10		10	ns	
tPLH tPHL Propagation delay time	A or B	B or A	$C_L = 50\text{ pF}$, (see Figure 4)	0.6	6		8		8	ns	
tPZH tPZL Switch turn-on time	C	A or B	$C_L = 50\text{ pF}$, $R_L = 1\text{ k}\Omega$ (see Figure 5)	2.1	12		16		16	ns	
tPLZ tPHZ Switch turn-off time	C	A or B	$C_L = 50\text{ pF}$, $R_L = 1\text{ k}\Omega$ (see Figure 5)	5.1	12		16		16	ns	

analog switch characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) $20\log_{10}(V_O/V_I) = -3\text{ dB}$ (see Figure 6)	2.3 V	30			MHz
				3 V	35			
				4.5 V	50			
Crosstalk (between any switches)	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 7)	2.3 V	-45			dB
				3 V	-45			
				4.5 V	-45			
Crosstalk (control input to signal output)	C	A or B	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8)	2.3 V	15			mV
				3 V	20			
				4.5 V	50			
Feed-through attenuation (switch off)	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (see Figure 9)	2.3 V	-40			dB
				3 V	-40			
				4.5 V	-40			
Sine-wave distortion	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10)	$V_I = 2\text{ V}_{p-p}$	2.3 V	0.1		%
				$V_I = 2.5\text{ V}_{p-p}$	3 V	0.1		
				$V_I = 4\text{ V}_{p-p}$	4.5 V	0.1		

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	4.5	pF

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PARAMETER MEASUREMENT INFORMATION

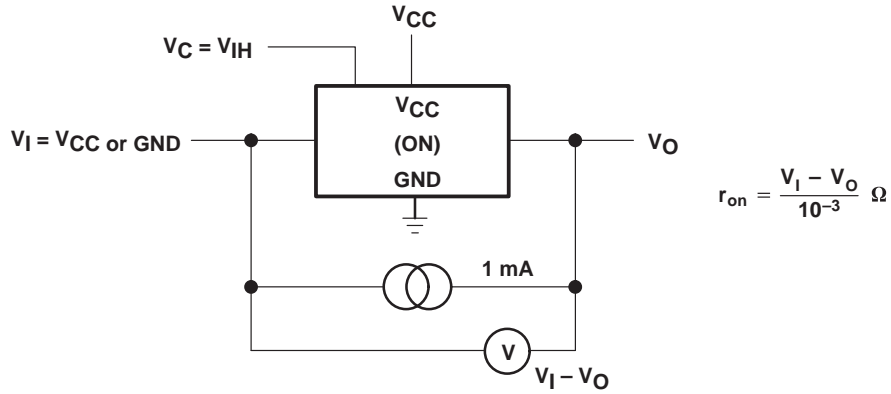


Figure 1. On-State Resistance Test Circuit

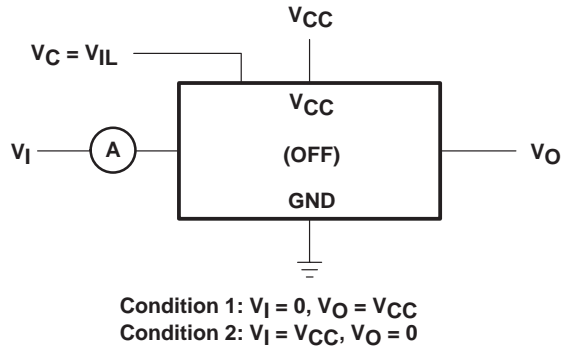


Figure 2. Off-State Switch Leakage-Current Test Circuit

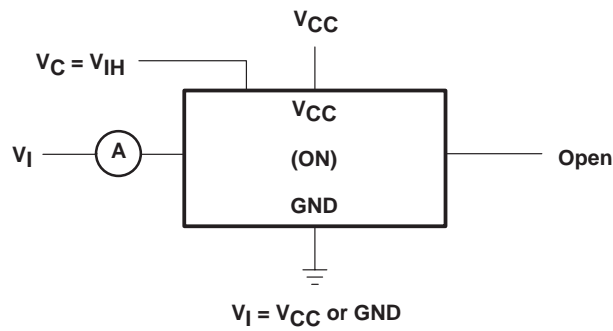


Figure 3. On-State Leakage-Current Test Circuit

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PARAMETER MEASUREMENT INFORMATION

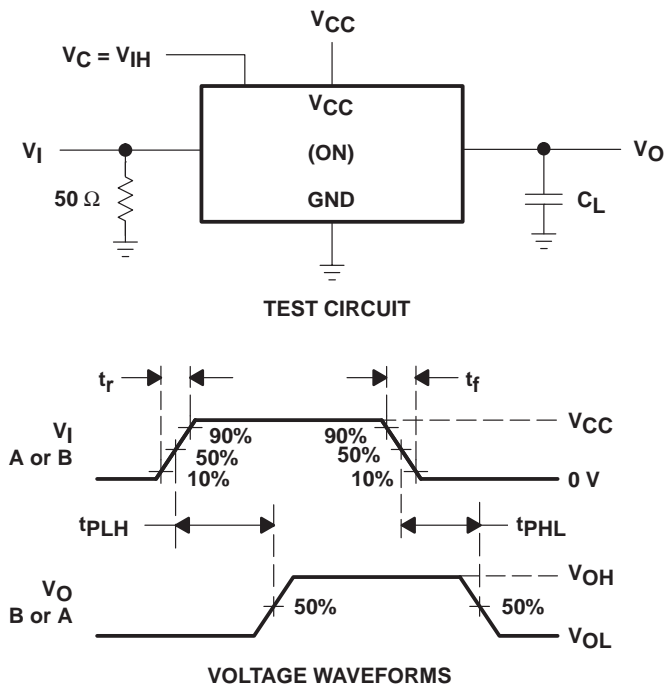
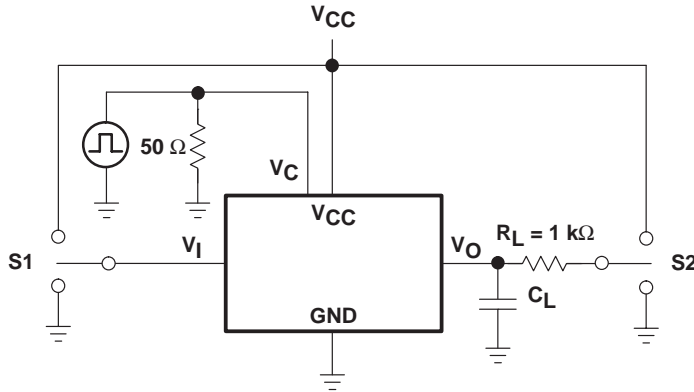


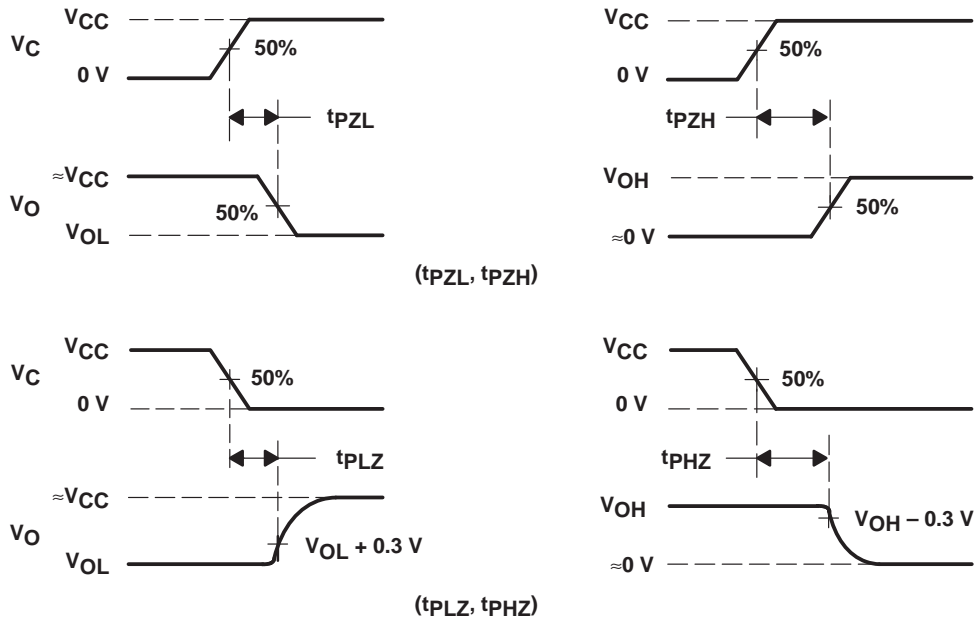
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST	S1	S2
t _{PZL}	GND	V _{CC}
t _{PZH}	V _{CC}	GND
t _{PLZ}	GND	V _{CC}
t _{PHZ}	V _{CC}	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

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PARAMETER MEASUREMENT INFORMATION

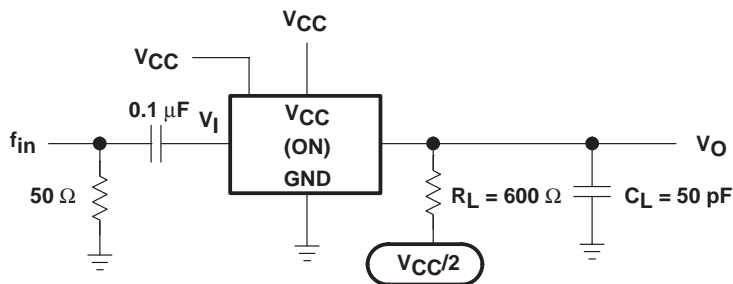


Figure 6. Frequency Response (Switch On)

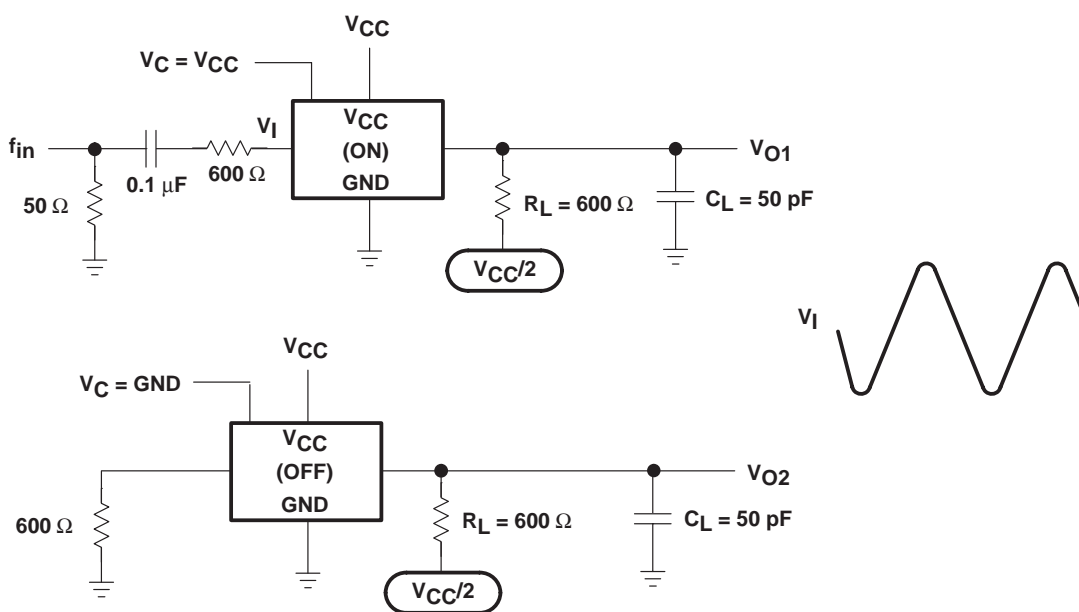


Figure 7. Crosstalk Between Any Two Switches

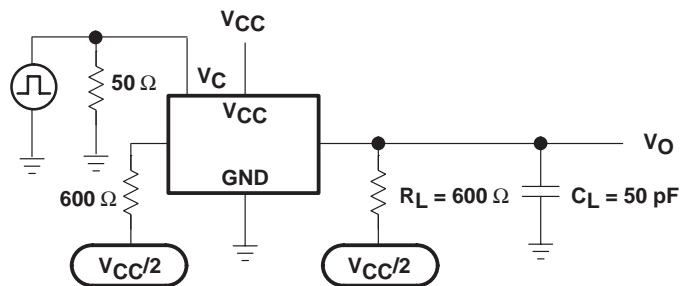


Figure 8. Crosstalk (Control Input – Switch Output)

PARAMETER MEASUREMENT INFORMATION

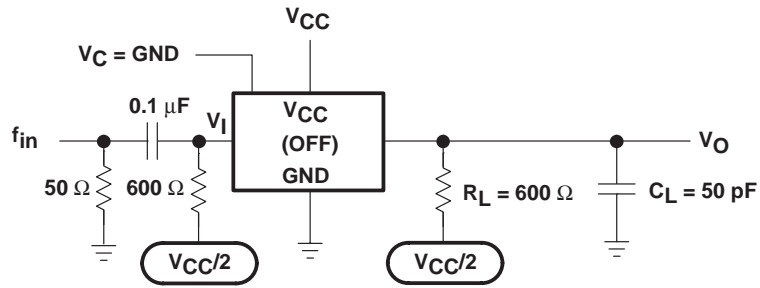


Figure 9. Feed-Through Attenuation (Switch Off)

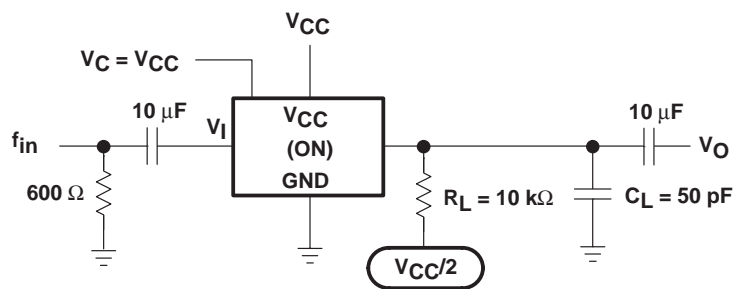


Figure 10. Sine-Wave Distortion

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

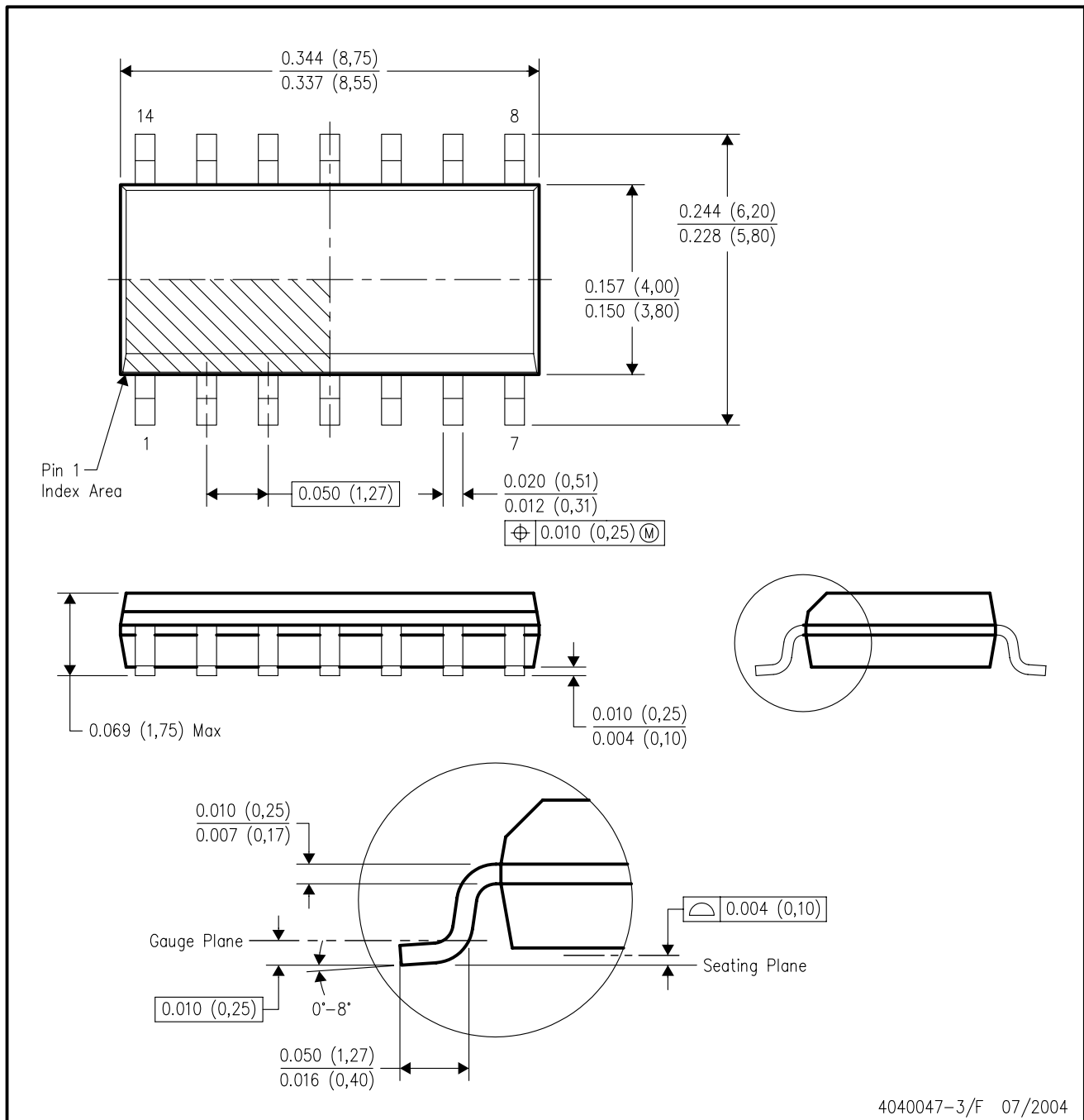
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

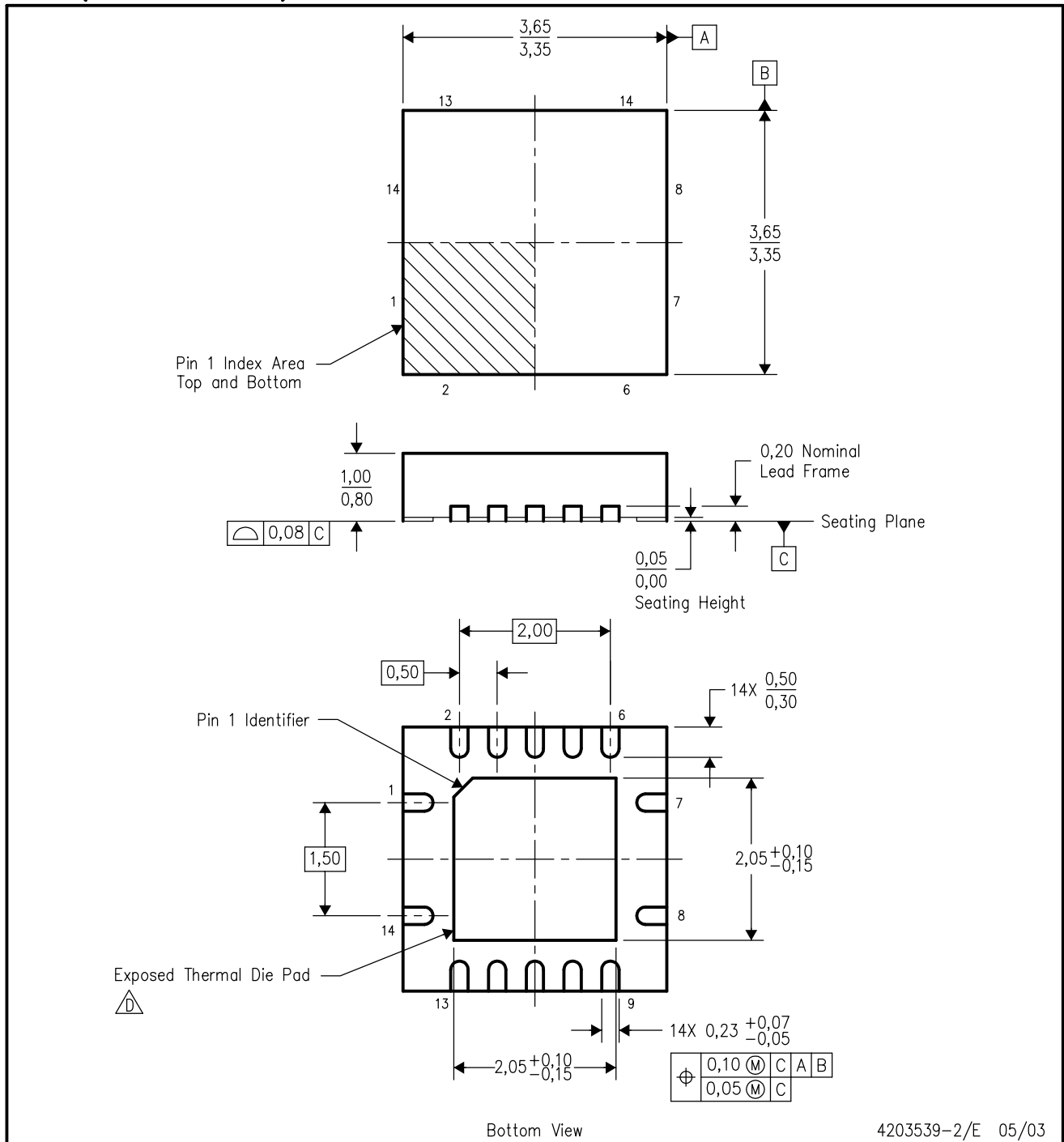
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - \triangle D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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