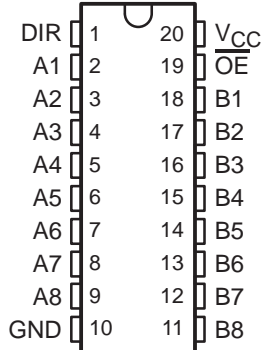


SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

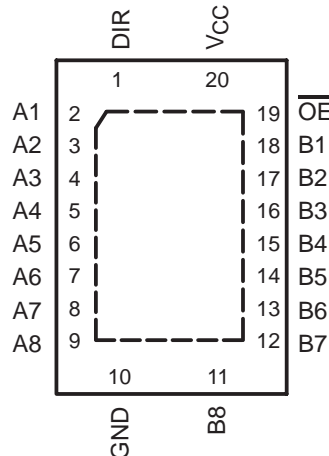
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

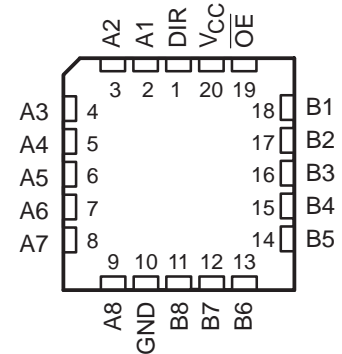
SN54LV245A . . . J OR W PACKAGE
SN74LV245A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV245A . . . RGY PACKAGE
(TOP VIEW)



SN54LV245A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV245ARGYR	LV245A	
	SOIC – DW	Tube of 25	SN74LV245ADW	LV245A	
		Reel of 2000	SN74LV245ADWR		
	SOP – NS	Reel of 2000	SN74LV245ANSR	74LV245A	
	SSOP – DB	Tube of 70	Reel of 2000	SN74LV245ADBR	LV245A
			Reel of 2000	SN74LV245APW	
		TSSOP – PW	Reel of 2000	SN74LV245APWR	LV245A
			Reel of 250	SN74LV245APWT	
TVSOP – DGV	Reel of 2000	SN74LV245ADGVR	LV245A		
VFBGA – GQN	Reel of 1000	SN74LV245AGQNR	LV245A		
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV245AJ	SNJ54LV245AJ	
	CFP – W	Tube of 85	SNJ54LV245AW	SNJ54LV245AW	
	LCCC – FK	Tube of 55	SNJ54LV245AFK	SNJ54LV245AFK	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

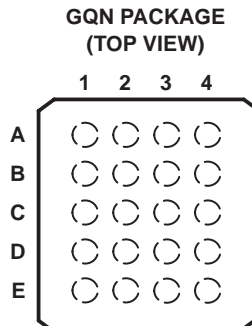
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description/ordering information (continued)

The 'LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.



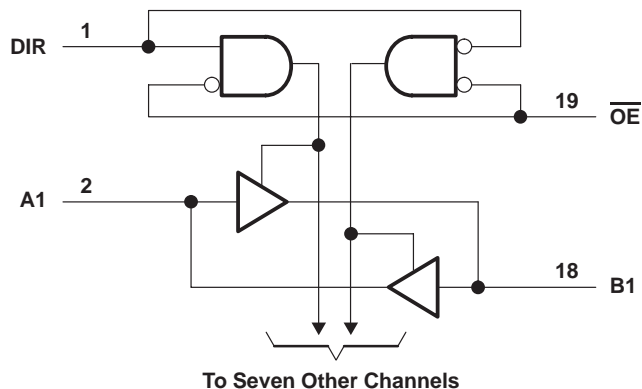
terminal assignments

	1	2	3	4
A	A1	DIR	V_{CC}	\overline{OE}
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

SN54LV245A, SN74LV245A
OCTAL BUS TRANSCEIVERS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I : Except I/O ports (see Note 1)	-0.5 V to 7 V
I/O ports (see Notes 1 and 2)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.



SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 5)

		SN54LV245A		SN74LV245A		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	2	5.5	2	5.5	V	
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	0.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
V_I	Input voltage	0	5.5	0	5.5	V	
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2	-2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-8	-8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16	-16		
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	μA	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2	2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		8	8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16	16		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200	200	ns/V	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100	100		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	20		
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV245A			SN74LV245A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -8 mA	3 V	2.48			2.48			
	I _{OH} = -16 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V				0.1			V
	I _{OL} = 2 mA	2.3 V				0.4			
	I _{OL} = 8 mA	3 V				0.44			
	I _{OL} = 16 mA	4.5 V				0.55			
I _I	Control inputs	V _I = 5.5 V or GND	0 to 5.5 V			±1			μA
I _{OZ}	A or B port	V _O = V _{CC} or GND	5.5 V			±5			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			20			μA
I _{off}		V _I or V _O = 0 to 5.5 V	0			5			μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			3			pF
			5 V			3			
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V			5.5			pF
			5 V			5.5			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	C _L = 15 pF	8.3*	13*		1*	15*	1	15	ns
t _{en}	\overline{OE}	A or B		11.8*	19.9*		1*	22*	1	22	
t _{dis}	\overline{OE}	A or B		11.8*	18.1*		1*	20*	1	20	
t _{pd}	A or B	B or A	C _L = 50 pF	11.2	15.9		1	18	1	18	ns
t _{en}	\overline{OE}	A or B		14.1	22.7		1	26	1	26	
t _{dis}	\overline{OE}	A or B		17.6	23.1		1	25	1	25	
t _{sk(o)}						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	C _L = 15 pF	5.9*	8.4*		1*	10*	1	10	ns
t _{en}	\overline{OE}	A or B		8.2*	13.2*		1*	15.5*	1	15.5	
t _{dis}	\overline{OE}	A or B		9.6*	16.5*		1*	19.5*	1	19.5	
t _{pd}	A or B	B or A	C _L = 50 pF	7.9	11.9		1	13.5	1	13.5	ns
t _{en}	\overline{OE}	A or B		9.9	16.7		1	19	1	19	
t _{dis}	\overline{OE}	A or B		13.9	19.8		1	22	1	22	
t _{sk(o)}						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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SN54LV245A, SN74LV245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV245A		SN74LV245A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	$C_L = 15\text{ pF}$	4.3*	5.5*		1*	6.5*	1	6.5	ns
t_{en}	\overline{OE}	A or B		5.7*	8.5*		1*	10.6*	1	10	
t_{dis}	\overline{OE}	A or B		7.8*	12.8*		1*	14.7*	1	14.2	
t_{pd}	A or B	B or A	$C_L = 50\text{ pF}$	5.6	7.5		1	8.5	1	8.5	ns
t_{en}	\overline{OE}	A or B		7	10.6		1	12	1	12	
t_{dis}	\overline{OE}	A or B		10.9	14.7		1	16	1	16	
$t_{sk(o)}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

PARAMETER		SN74LV245A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

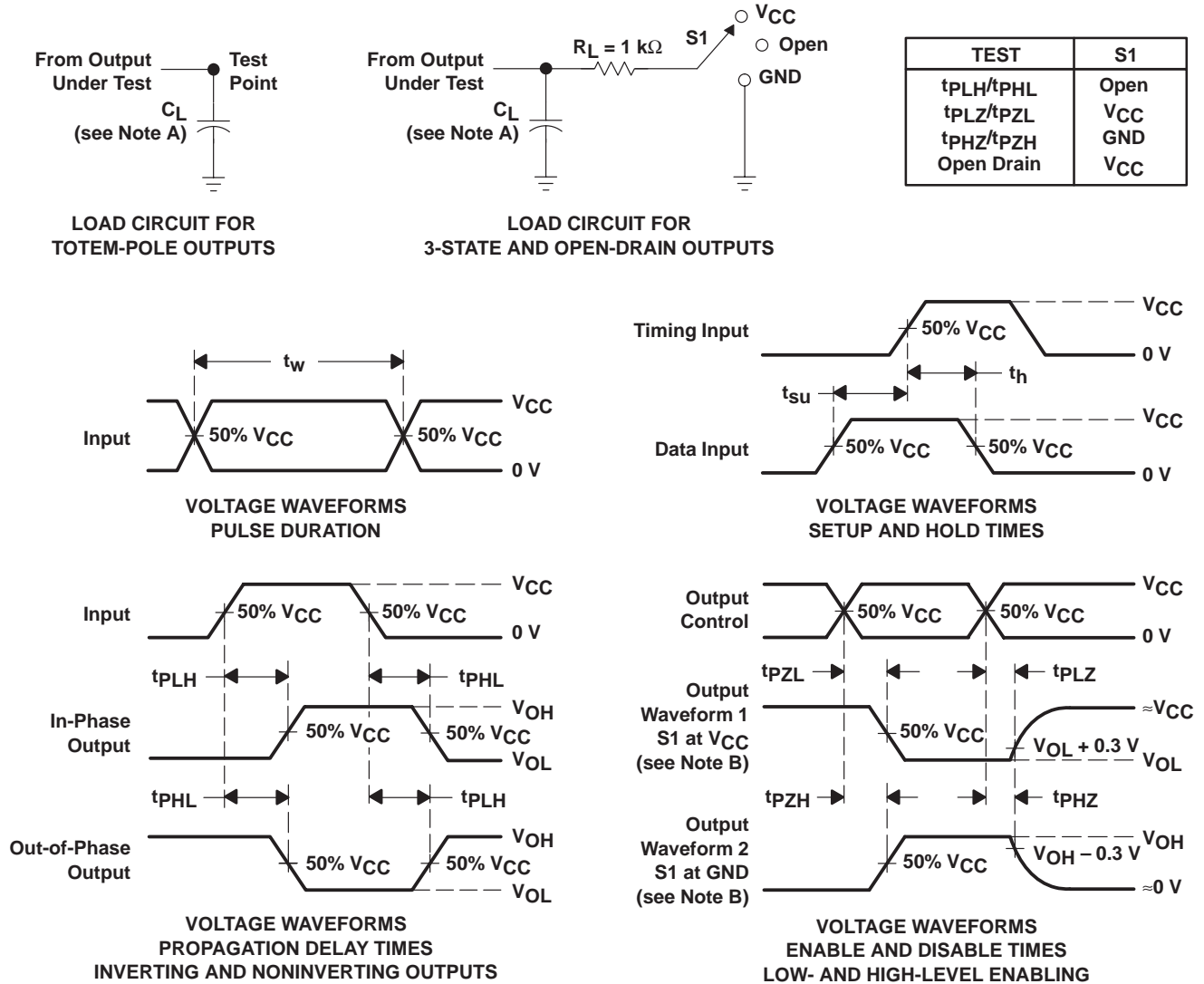
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V 5 V	20 25	pF

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PARAMETER MEASUREMENT INFORMATION

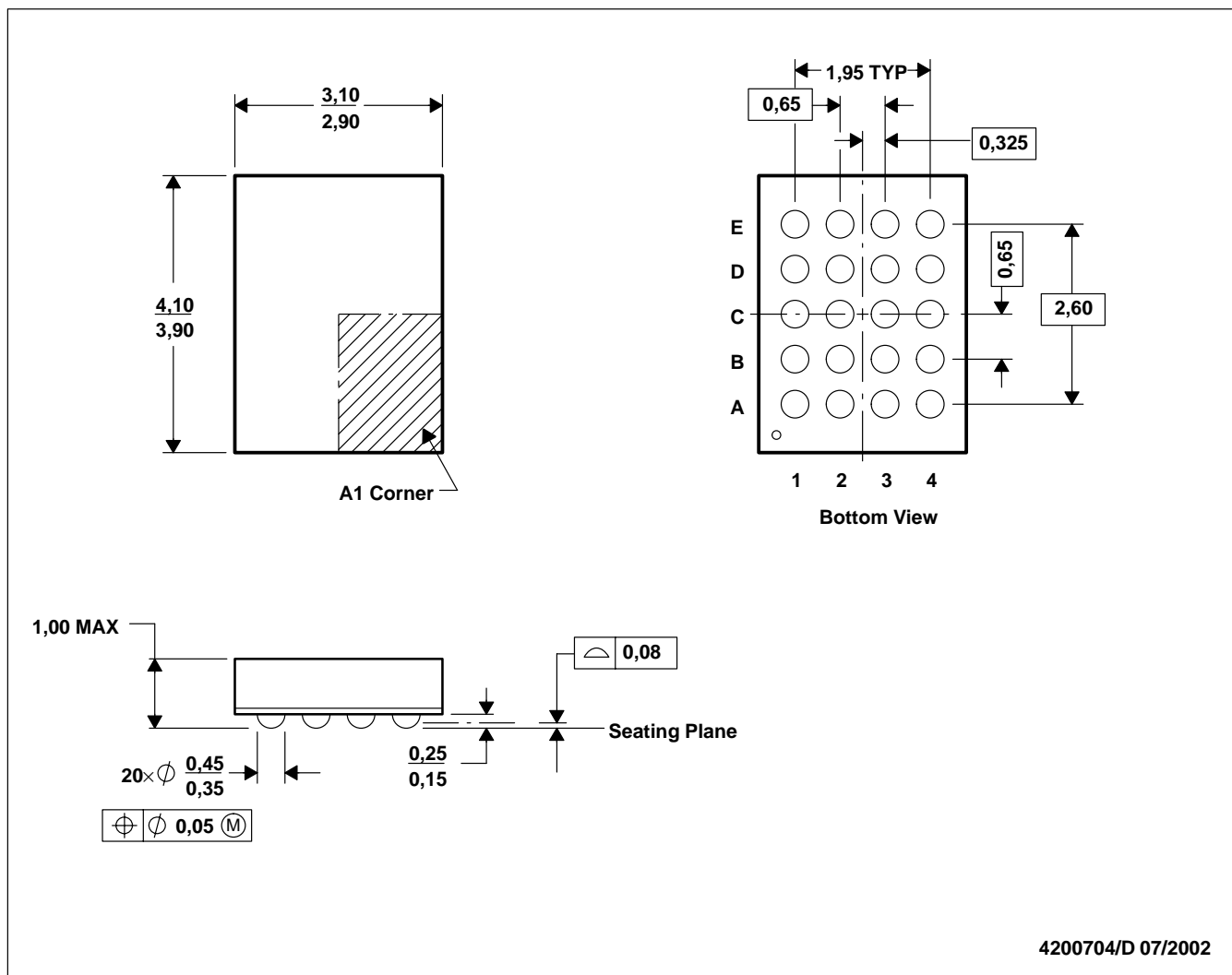


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PHL} and t_{PLH} are the same as t_{pd}.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ configuration
 - D. Falls within JEDEC MO-225 variation BC.
 - E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

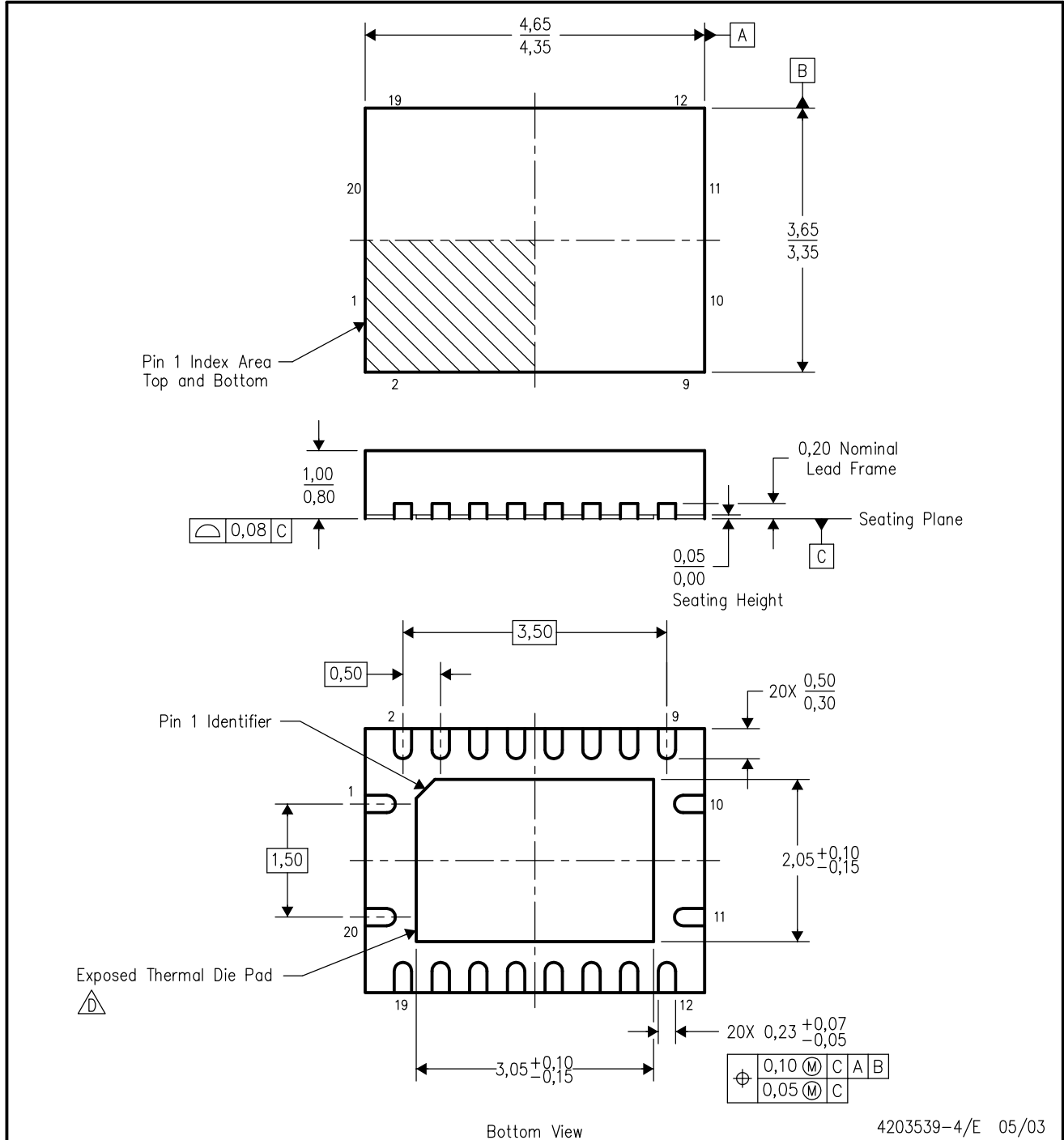
24 PINS SHOWN




- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK

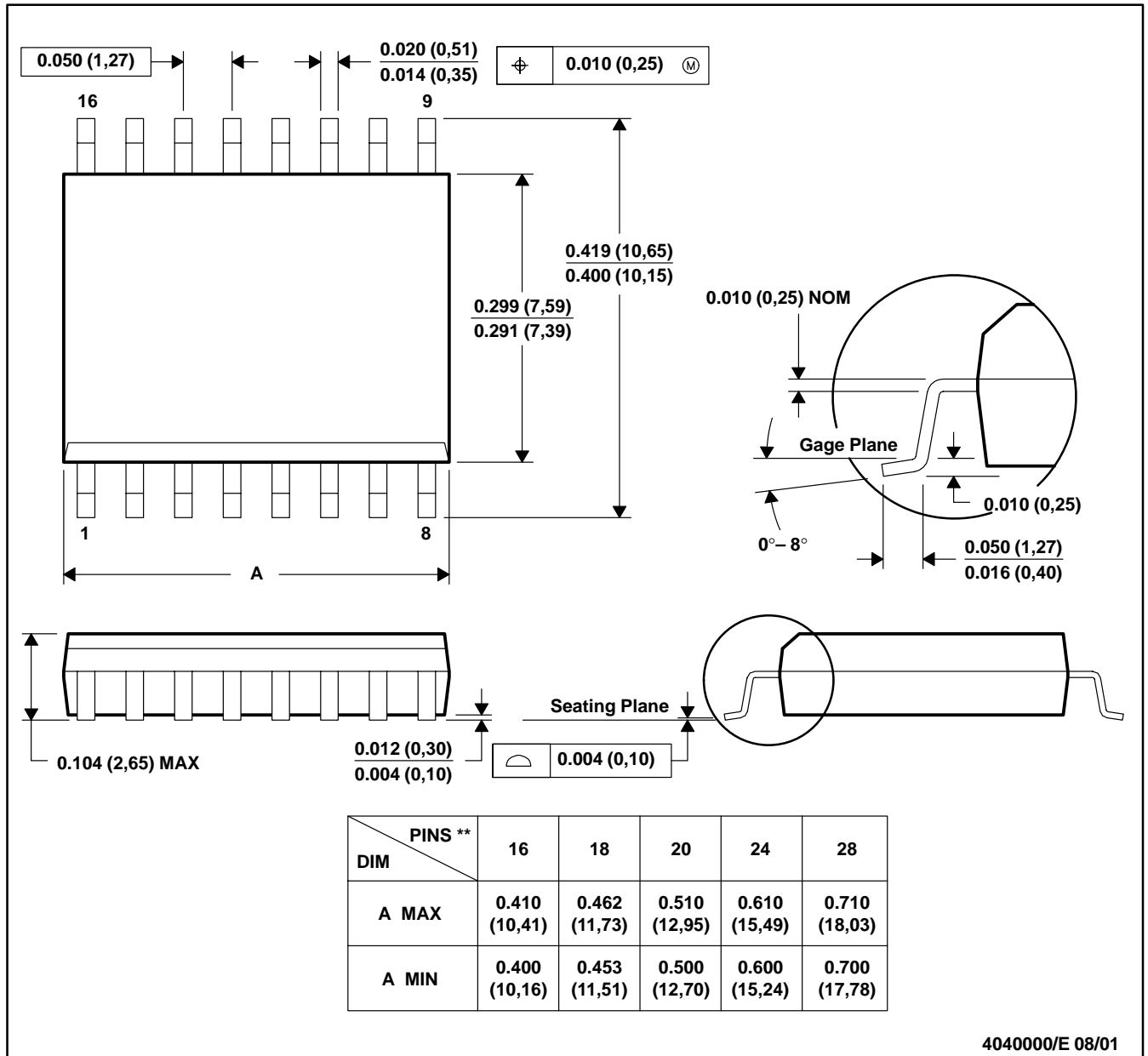


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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