

SN54LV240, SN74LV240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS193B – FEBRUARY 1993 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

description

These octal buffers/drivers are designed for 2.7-V to 5.5-V V_{CC} operation.

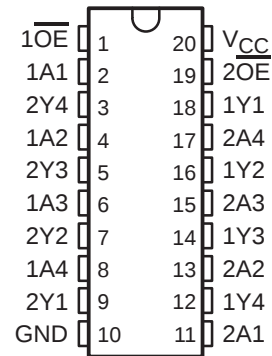
The 'LV240 are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'LV240 are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

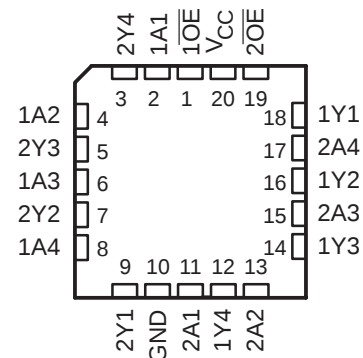
The SN74LV240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV240 is characterized for operation from -40°C to 85°C .

SN54LV240 . . . J OR W PACKAGE
SN74LV240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LV240 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	L
L	L	H
H	X	Z



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**TEXAS
INSTRUMENTS**

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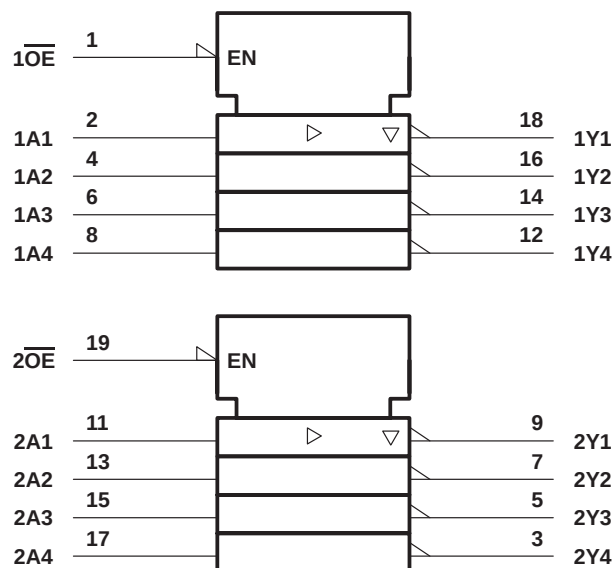
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OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCLS193B – FEBRUARY 1993 – REVISED APRIL 1996

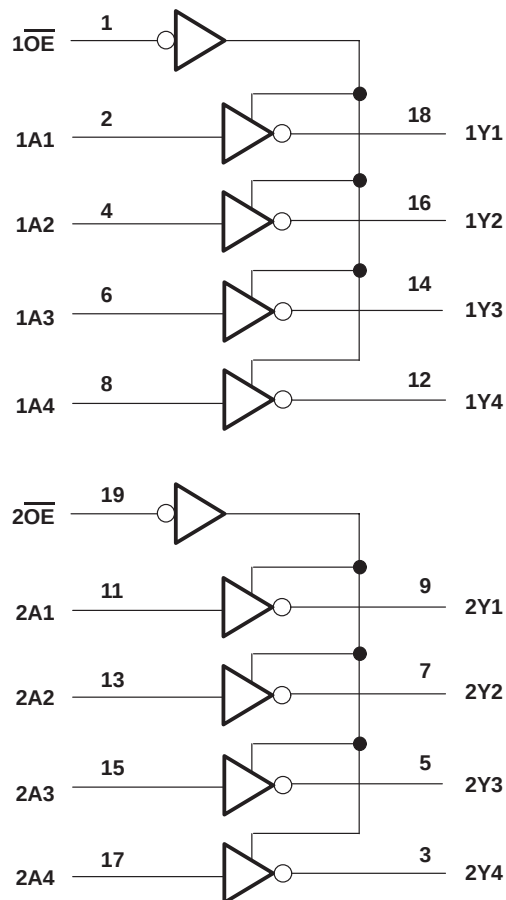
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DB, DW, J, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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SCLS193B – FEBRUARY 1993 – REVISED APRIL 1996

recommended operating conditions (see Note 4)

			SN54LV240		SN74LV240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	5.5	2.7	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		2		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3.15		3.15		
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8		0.8	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		–8		–8	mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		–16		–16	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		8		8	mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	100	0	100	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	SN54LV240			SN74LV240			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −100 μA	MIN to MAX	V _{CC} − 0.2			V _{CC} − 0.2			V
	I _{OH} = −8 mA	3 V	2.4			2.4			
	I _{OH} = −16 mA	4.5 V	3.6			3.6			
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2			0.2			V
	I _{OL} = 8 mA	3 V	0.4			0.4			
	I _{OL} = 16 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±1			±1			μA
		5.5 V	±1			±1			
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±5			±5			μA
		5.5 V	±5			±5			
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			20			μA
		5.5 V	20			20			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	3			3			pF
		5 V	3			3			
C _O	V _O = V _{CC} or GND	3.3 V	8			8			pF
		5 V	8			8			

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV240								UNIT
			V _{CC} = 5 V ± 0.5 V			V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	7	13		9	16		18	ns	
t _{en}	$\overline{OE}$	Y	11	18		14	24		28	ns	
t _{dis}	$\overline{OE}$	Y	12	23		14	24		25	ns	

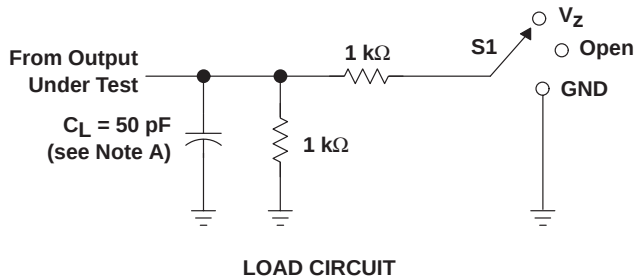
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV240								UNIT
			V _{CC} = 5 V ± 0.5 V			V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y		7	13		9	16		18	ns
t _{en}	$\overline{\text{OE}}$	Y		11	18		14	24		28	ns
t _{dis}	$\overline{\text{OE}}$	Y		12	23		14	24		25	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

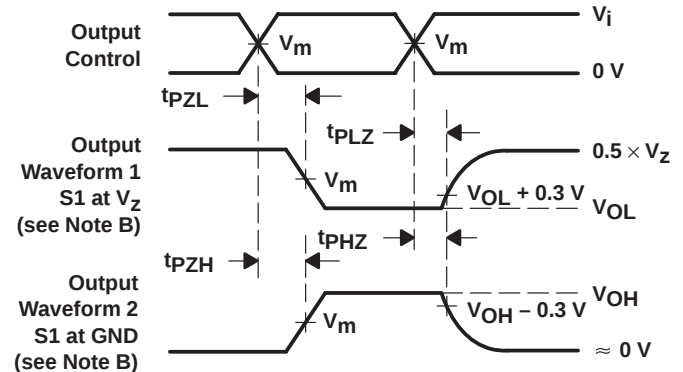
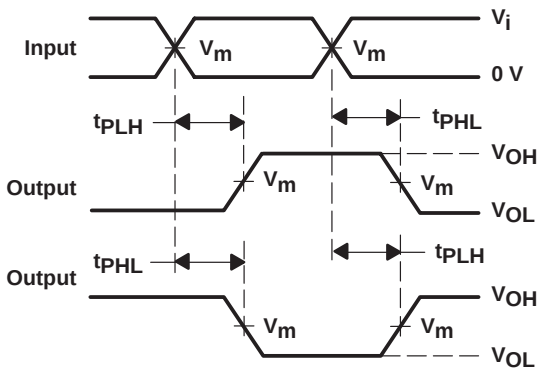
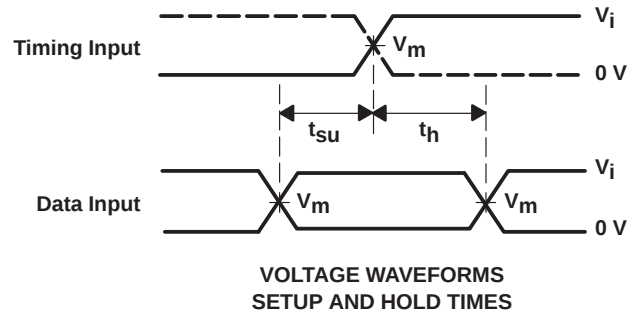
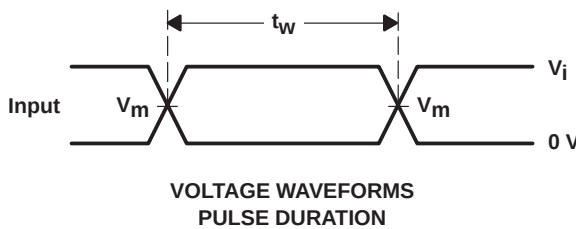
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	45	pF
	Outputs disabled			2.5	
	Outputs enabled		5 V	78	
	Outputs disabled			3	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _Z
t _{PHZ} /t _{PZH}	GND

WAVEFORM CONDITION	V _{CC} = 4.5 V to 5.5 V	V _{CC} = 2.7 V to 3.6 V
V _m	0.5 × V _{CC}	1.5 V
V _i	V _{CC}	2.7 V
V _Z	2 × V _{CC}	6 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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