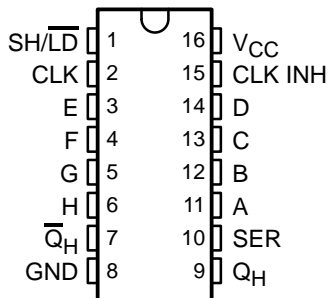


SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

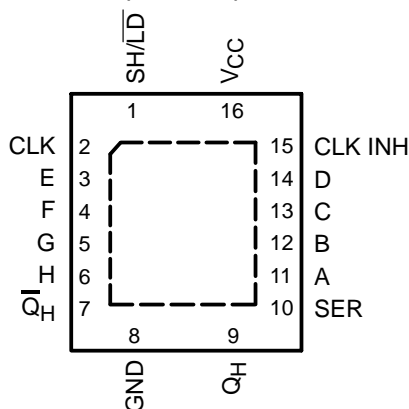
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10.5 ns at 5 V
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

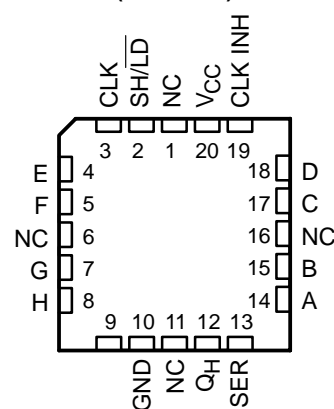
SN54LV165A . . . J OR W PACKAGE
SN74LV165A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV165A . . . RGY PACKAGE
(TOP VIEW)



SN54LV165A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

When the devices are clocked, data is shifted toward the serial output Q_H . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load ($\overline{SH/LD}$) input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output, \overline{Q}_H .

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV165ARGYR	LV165A
	SOIC – D	Tube of 40	SN74LV165AD	LV165A
		Reel of 2500	SN74LV165ADR	
	SOP – NS	Reel of 2000	SN74LV165ANSR	74LV165A
	SSOP – DB	Reel of 2000	SN74LV165ADBR	LV165A
	TSSOP – PW	Tube of 90	SN74LV165APW	LV165A
		Reel of 2000	SN74LV165APWR	
Reel of 250		SN74LV165APWT		
TVSOP – DGV	Reel of 2000	SN74LV165ADGVR	LV165A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV165AJ	SNJ54LV165AJ
	CFP – W	Tube of 150	SNJ54LV165AW	SNJ54LV165AW
	LCCC – FK	Tube of 55	SNJ54LV165AFK	SNJ54LV165AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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description/ordering information (continued)

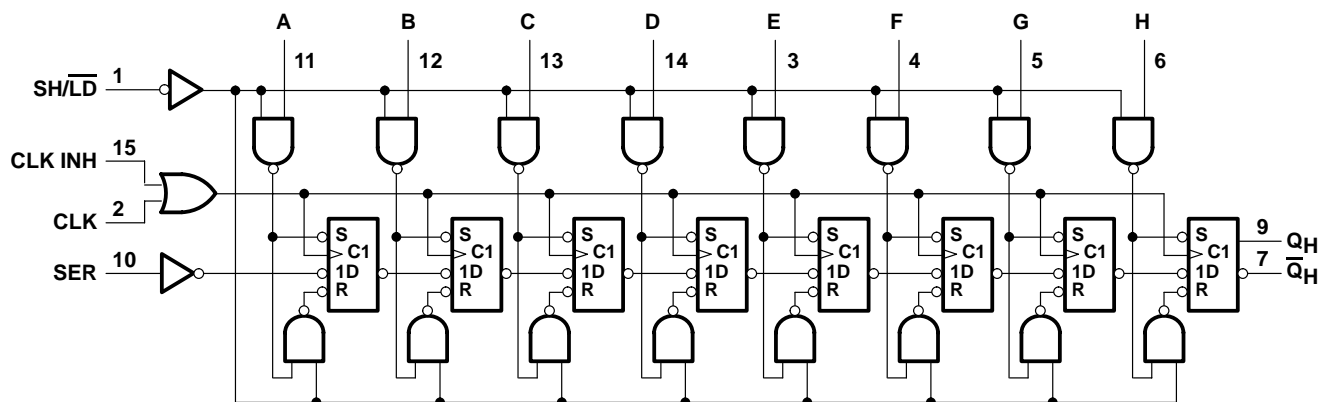
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{SH/LD}$ is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when $\overline{SH/LD}$ is held high. The parallel inputs to the register are enabled while $\overline{SH/LD}$ is held low, independently of the levels of CLK, CLK INH, or SER.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

INPUTS			OPERATION
$\overline{SH/LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	Q_0
H	X	H	Q_0
H	L	↑	Shift
H	↑	L	Shift

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

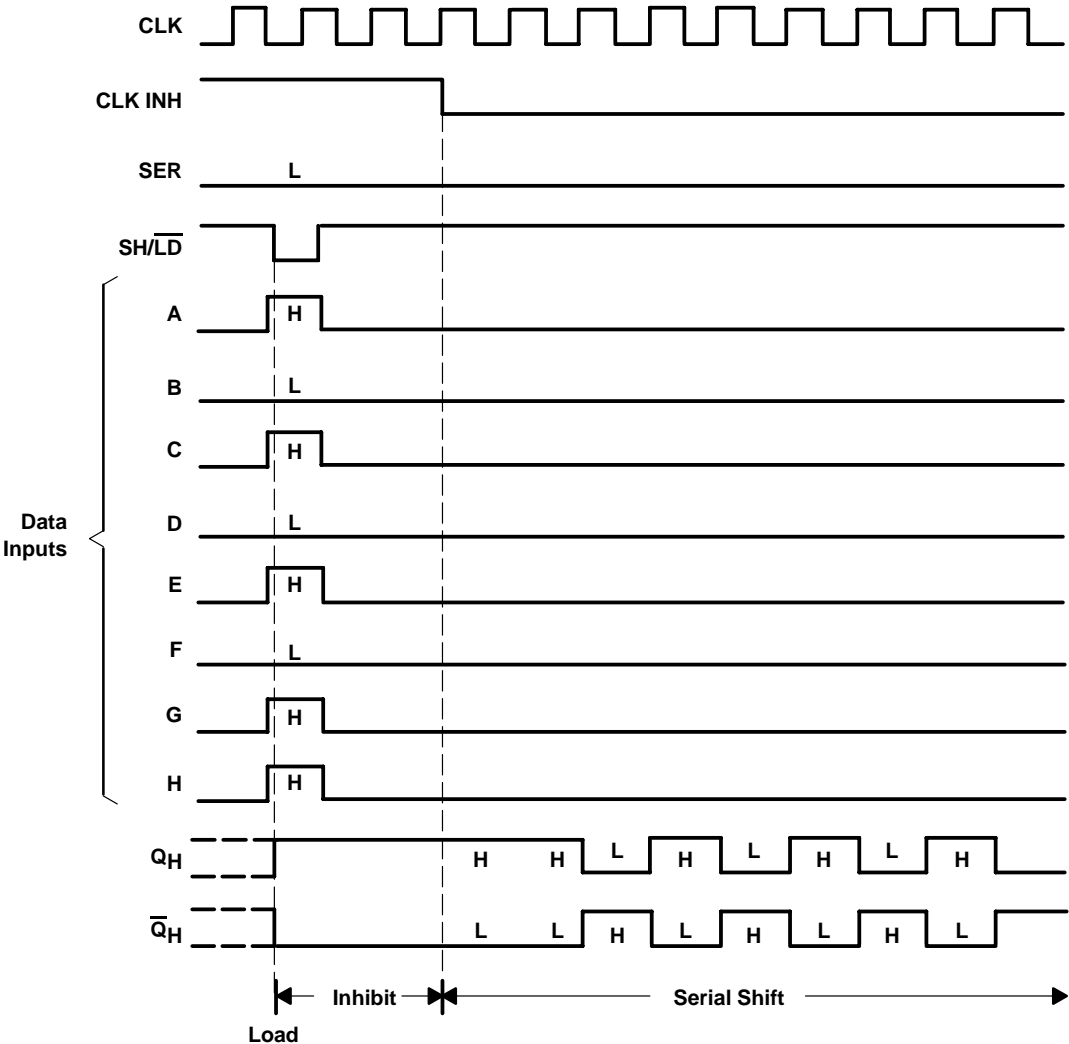


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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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typical shift, load, and inhibit sequences



SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): NS package	67°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.



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recommended operating conditions (see Note 5)

		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA
		V _{CC} = 2.3 V to 2.7 V		-2	-2	mA
		V _{CC} = 3 V to 3.6 V		-6	-6	
		V _{CC} = 4.5 V to 5.5 V		-12	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA
		V _{CC} = 2.3 V to 2.7 V		2	2	mA
		V _{CC} = 3 V to 3.6 V		6	6	
		V _{CC} = 4.5 V to 5.5 V		12	12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	200	ns/V
		V _{CC} = 3 V to 3.6 V		100	100	
		V _{CC} = 4.5 V to 5.5 V		20	20	
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV165A			SN74LV165A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 6 mA	3 V			0.44			0.44	
	I _{OL} = 12 mA	4.5 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		1.7			1.7		pF

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5 V \pm 0.2 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	8.5		9		9	ns
		SH/LD low	11		13		13	
t_{su}	Setup time	SH/LD high before CLK \uparrow	7		8.5		8.5	ns
		SER before CLK \uparrow	8.5		9.5		9.5	
		CLK INH before CLK \uparrow	7		7		7	
		Data before SH/LD \uparrow	11.5		12		12	
t_h	Hold time	SER data after CLK \uparrow	-1		0		0	ns
		Parallel data after SH/LD \uparrow	0		0.5		0.5	
		SH/LD high after CLK \uparrow	0		0		0	

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	6		7		7	ns
		SH/LD low	7.5		9		9	
t_{su}	Setup time	SH/LD high before CLK \uparrow	5		6		6	ns
		SER before CLK \uparrow	5		6		6	
		CLK INH before CLK \uparrow	5		5		5	
		Data before SH/LD \uparrow	7.5		8.5		8.5	
t_h	Hold time	SER data after CLK \uparrow	0		0		0	ns
		Parallel data after SH/LD \uparrow	0.5		0.5		0.5	
		SH/LD high after CLK \uparrow	0		0		0	

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	4		4		4	ns
		SH/LD low	5		6		6	
t_{su}	Setup time	SH/LD high before CLK \uparrow	4		4		4	ns
		SER before CLK \uparrow	4		4		4	
		CLK INH before CLK \uparrow	3.5		3.5		3.5	
		Data before SH/LD \uparrow	5		5		5	
t_h	Hold time	SER data after CLK \uparrow	0.5		0.5		0.5	ns
		Parallel data after SH/LD \uparrow	1		1		1	
		SH/LD high after CLK \uparrow	0.5		0.5		0.5	

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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15\text{ pF}$	50*	80*		45*		45		MHz
			$C_L = 50\text{ pF}$	40	65		35		35		
t_{pd}	CLK	Q_H or \bar{Q}_H	$C_L = 15\text{ pF}$		12.2*	19.8*	1*	22*	1	22	ns
	SH/ \bar{LD}				13.1*	21.5*	1*	23.5*	1	23.5	
	H				12.9*	21.7*	1*	24*	1	24	
t_{pd}	CLK	Q_H or \bar{Q}_H	$C_L = 50\text{ pF}$		15.3	23.3	1	26	1	26	ns
	SH/ \bar{LD}				16.1	25.1	1	28	1	28	
	H				15.9	25.3	1	28	1	28	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15\text{ pF}$	65*	115*		55*		55		MHz
			$C_L = 50\text{ pF}$	60	90		50		50		
t_{pd}	CLK	Q_H or \bar{Q}_H	$C_L = 15\text{ pF}$		8.6*	15.4*	1*	18*	1	18	ns
	SH/ \bar{LD}				9.1*	15.8*	1*	18.5*	1	18.5	
	H				8.9*	14.1*	1*	16.5*	1	16.5	
t_{pd}	CLK	Q_H or \bar{Q}_H	$C_L = 50\text{ pF}$		10.9	14.9	1	16.9	1	16.9	ns
	SH/ \bar{LD}				11.3	19.3	1	22	1	22	
	H				11.1	17.6	1	20	1	20	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15\text{ pF}$	110*	165*		90*		90		MHz
			$C_L = 50\text{ pF}$	95	125		85		85		
t_{pd}	CLK	Q_H or \bar{Q}_H	$C_L = 15\text{ pF}$		6*	9.9*	1*	11.5*	1	11.5	ns
	SH/ \bar{LD}				6*	9.9*	1*	11.5*	1	11.5	
	H				6*	9*	1*	10.5*	1	10.5	
t_{pd}	CLK	Q_H or \bar{Q}_H	$C_L = 50\text{ pF}$		7.7	11.9	1	13.5	1	13.5	ns
	SH/ \bar{LD}				7.7	11.9	1	13.5	1	13.5	
	H				7.6	11	1	12.5	1	12.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	36.1	pF
		5 V	37.5	

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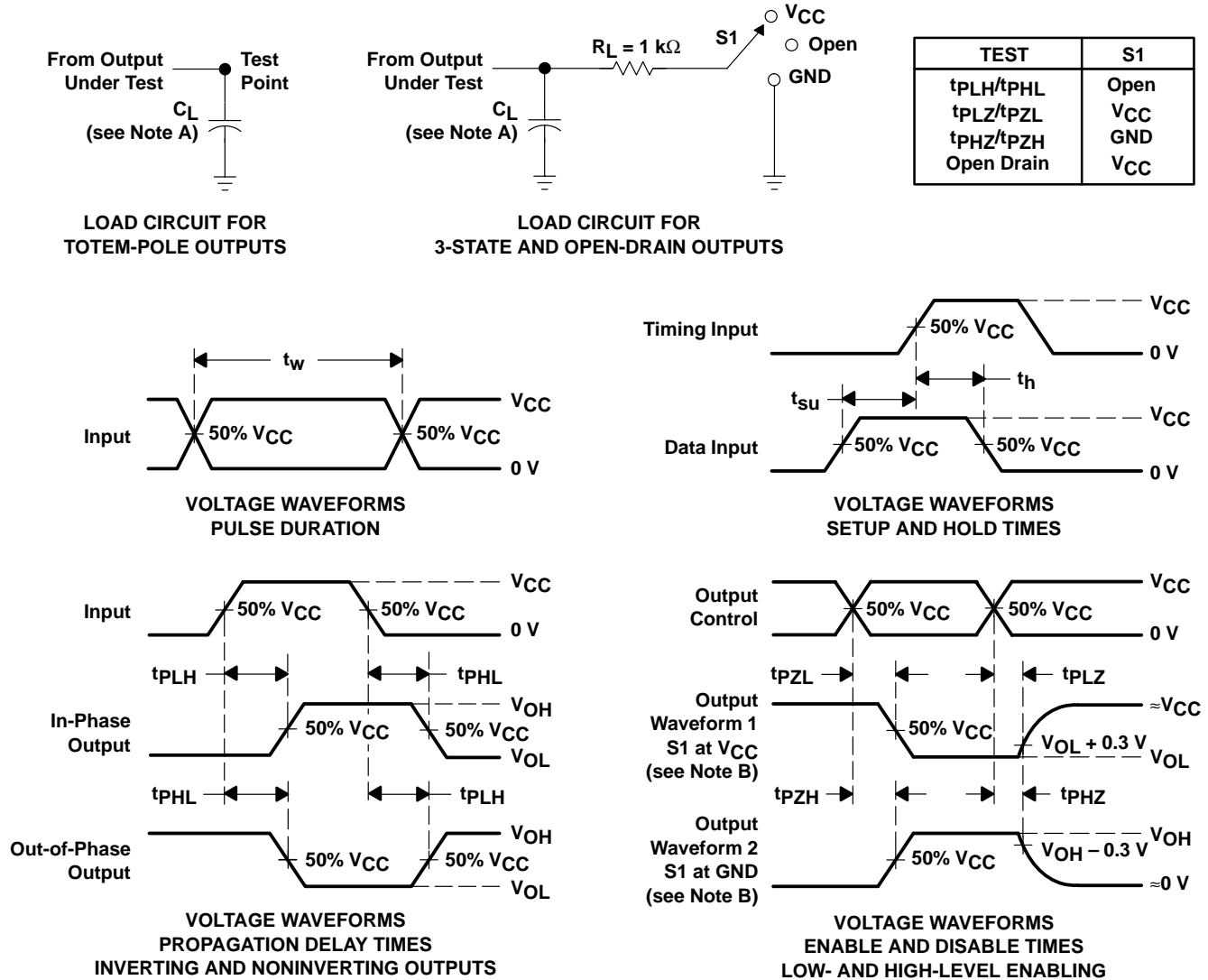


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SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

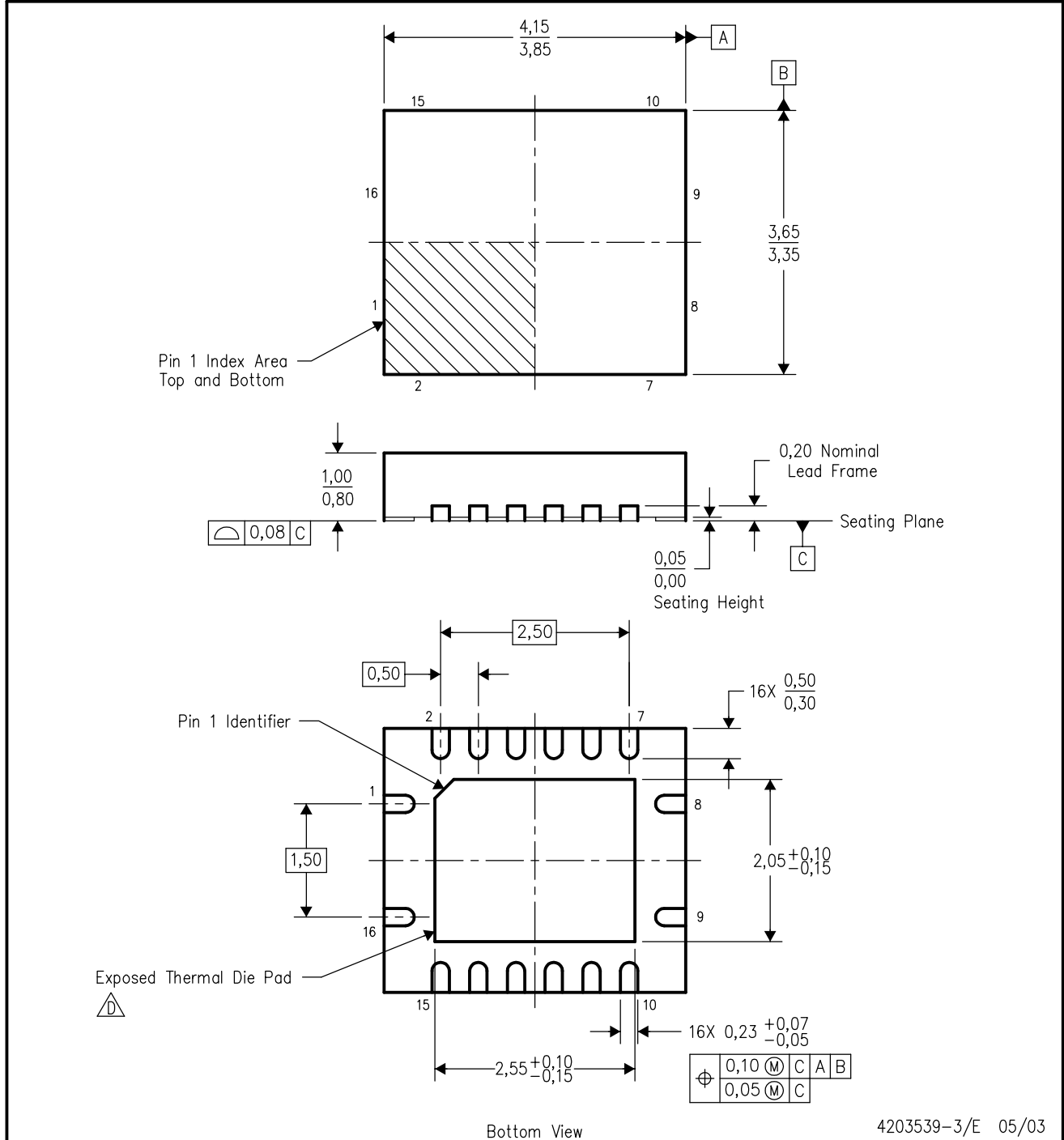
PLASTIC SMALL-OUTLINE PACKAGE




- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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