

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

'93A, 'LS93 . . . 4-Bit Binary Counters

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

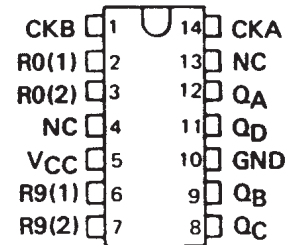
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A .

SN5490A, SN54LS90 . . . J OR W PACKAGE

SN7490A . . . N PACKAGE

SN74LS90 . . . D OR N PACKAGE

(TOP VIEW)

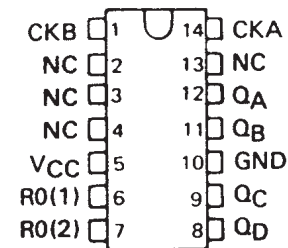


SN5492A, SN54LS92 . . . J OR W PACKAGE

SN7492A . . . N PACKAGE

SN74LS92 . . . D OR N PACKAGE

(TOP VIEW)

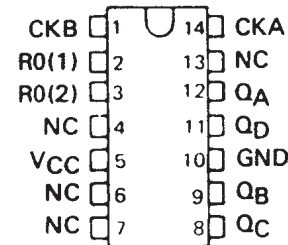


SN5493A, SN54LS93 . . . J OR W PACKAGE

SN7493 . . . N PACKAGE

SN74LS93 . . . D OR N PACKAGE

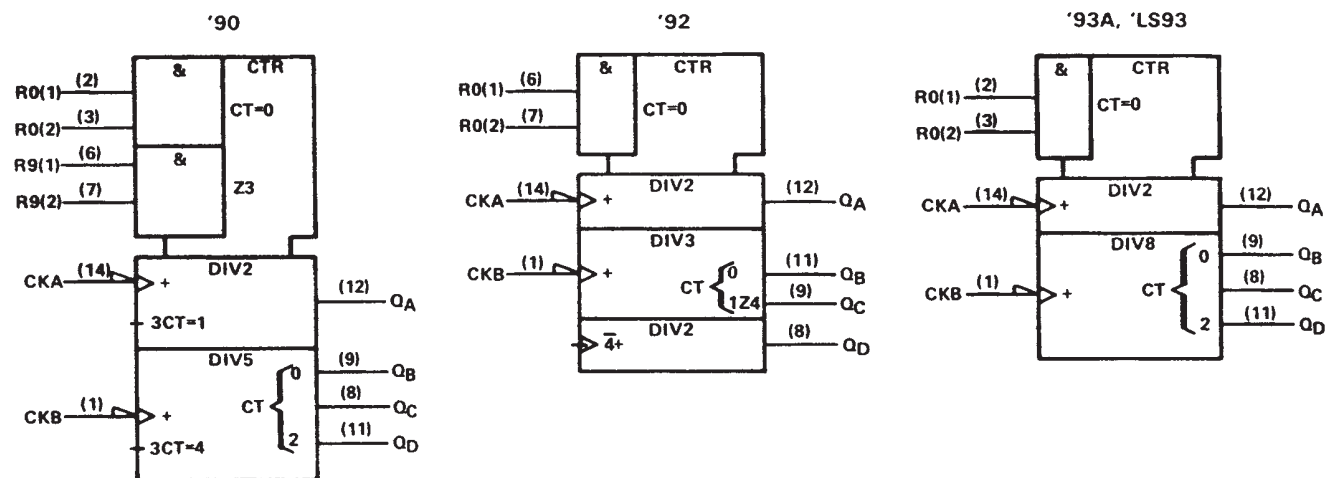
(TOP VIEW)



SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

'90A, 'LS90
 BCD COUNT SEQUENCE
 (See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90
 BI-QUINARY (5-2)
 (See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
 COUNT SEQUENCE
 (See Note C)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'LS90
 RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'93A, 'LS93
 COUNT SEQUENCE
 (See Note C)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'92A, 'LS92, '93A, 'LS93
 RESET/COUNT FUNCTION TABLE

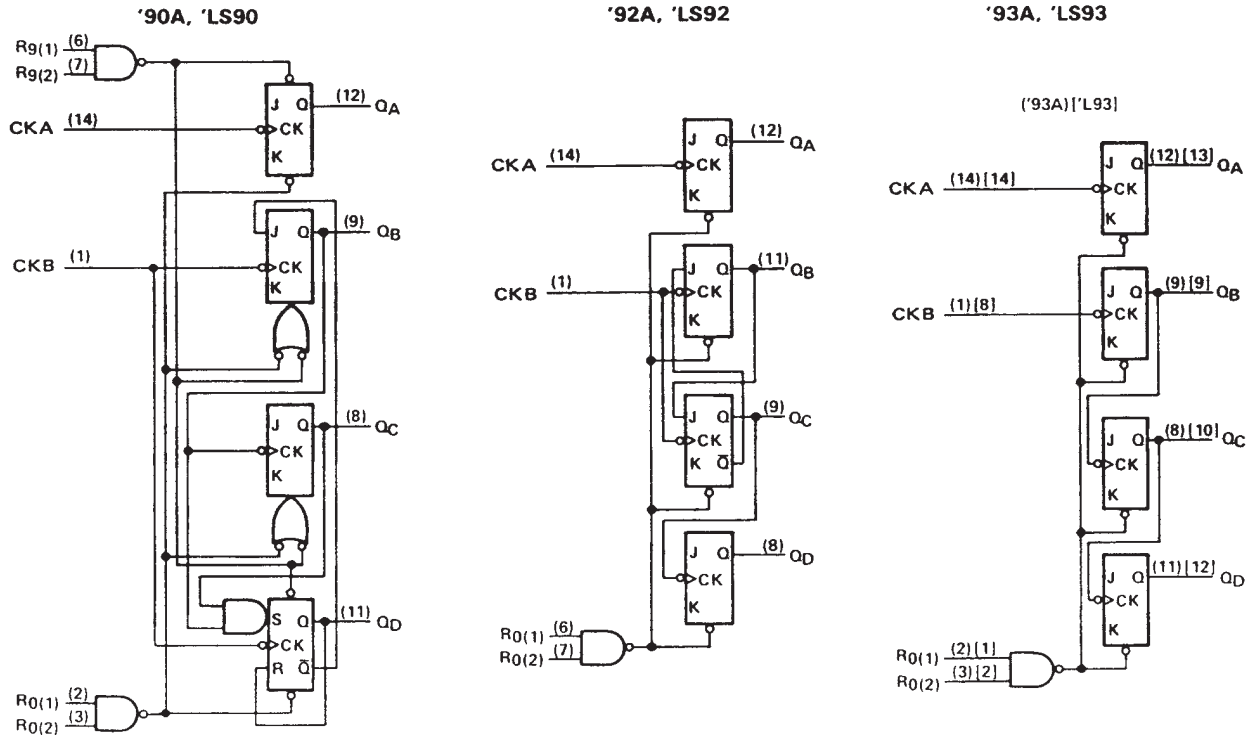
RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

- NOTES: A. Output Q_A is connected to input CKB for BCD count.
 B. Output Q_D is connected to input CKA for bi-quinary count.
 C. Output Q_A is connected to input CKB.
 D. H = high level, L = low level, X = irrelevant

SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

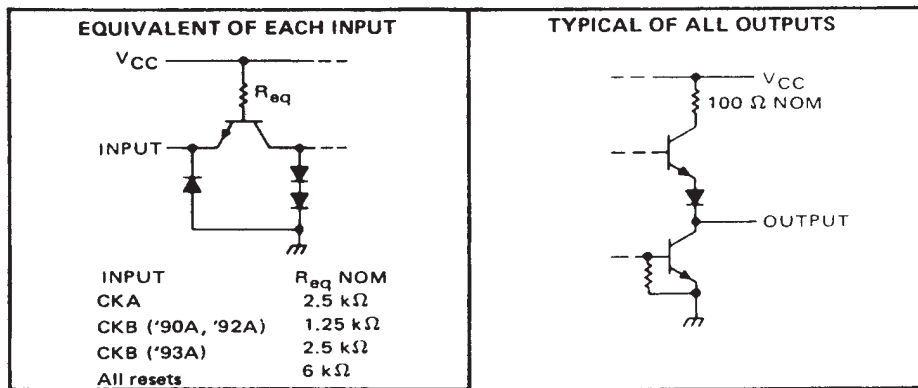
logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level. Pin numbers shown in () are for the 'LS93 and '93A and pin numbers shown in [] are for the 54L93.

schematics of inputs and outputs

'90A, '92A, '93A

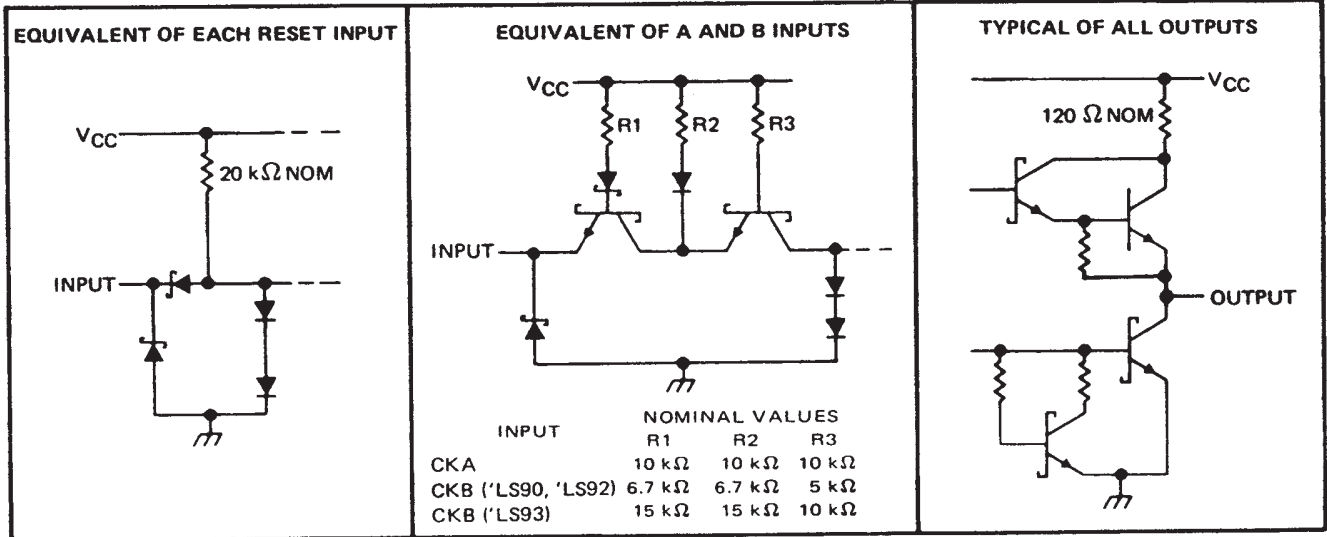


SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

schematics of inputs and outputs (continued)

'LS90, 'LS92, 'LS93



SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A	-55°C to 125°C
SN7490A, SN7492A, SN7493A	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_0 inputs.

recommended operating conditions

	SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0	32	0		32	MHz
	B input	0	16	0		16	
Pulse width, t_w	A input	15		15			ns
	B input	30		30			
	Reset inputs	15		15			
Reset inactive-state setup time, t_{su}		25			25		ns
Operating free-air temperature, T_A		-55	125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER [¶]	TEST CONDITIONS [†]	'90A		'92A		'93A		UNIT			
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		MIN	TYP [‡]	MAX
V_{IH} High-level input voltage		2			2		2		V		
V_{IL} Low-level input voltage				0.8		0.8		0.8	V		
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5		-1.5		-1.5	V		
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		2.4	3.4	V	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}^{\parallel}$		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		1		1		mA	
I_{IH} High-level input current	Any reset			40		40		40		μ A	
	CKA	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		80		80		80			
	CKB			120		120		80			
I_{IL} Low-level input current	Any reset			-1.6		-1.6		-1.6		mA	
	CKA	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-3.2		-3.2		-3.2			
	CKB			-4.8		-4.8		-3.2			
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54'	-20	-57	-20	-57	-20	-57		mA	
		SN74'	-18	-57	-18	-57	-18	-57			
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		29	42		26	39		26	39	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

[¶] '90A outputs are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	CKA	Q_A	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A		10	16		10	16		10	16		ns
t_{PHL}				12	18		12	18		12	18		
t_{PLH}	CKA	Q_D		32	48		32	48		46	70		ns
t_{PHL}				34	50		34	50		46	70		
t_{PLH}	CKB	Q_B		10	16		10	16		10	16		ns
t_{PHL}				14	21		14	21		14	21		
t_{PLH}	CKB	Q_C		21	32		10	16		21	32		ns
t_{PHL}				23	35		14	21		23	35		
t_{PLH}	CKB	Q_D		21	32		21	32		34	51		ns
t_{PHL}				23	35		23	35		34	51		
t_{PHL}	Set-to-0	Any		26	40		26	40		26	40		ns
t_{PLH}	Set-to-9	Q_A, Q_D		20	30								ns
t_{PHL}		Q_B, Q_C		26	40								

† f_{\max} = maximum count frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output



**SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS**

SDLS940A – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: R inputs	7 V
A and B inputs	5.5 V
Operating free-air temperature range: SN54LS' Circuits	-55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Count frequency, f_{count} (see Figure 1)	A input	0	32	0		32	MHz
	B input	0	16	0		16	
Pulse width, t_w	A input	15		15			ns
	B input	30		30			
	Reset inputs	30		30			
Reset inactive-state setup time, t_{su}	25			25			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA} \text{ ¶}$ $I_{OL} = 8 \text{ mA} \text{ ¶}$	0.25	0.4		0.25	0.4		V
					0.35	0.5		
I_I Input current at maximum input voltage	Any reset			0.1			0.1	mA
	CKA			0.2			0.2	
	CKB			0.4			0.4	
I_{IH} High-level input current	Any reset			20			20	μ A
	CKA			40			40	
	CKB			80			80	
I_{IL} Low-level input current	Any reset			-0.4			-0.4	mA
	CKA			-2.4			-2.4	
	CKB			-3.2			-3.2	
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3	'LS90	9	15	9	15		mA
		'LS92	9	15	9	15		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ I_{OL} outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS93			SN74LS93			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA¶			0.25 0.4			V
			I _{OL} = 8 mA¶			0.35 0.5			
I _I	Input current at maximum input voltage	Any reset	V _{CC} = MAX, V _I = 7 V			0.1			mA
		CKA or CKB	V _{CC} = MAX, V _I = 5.5 V			0.2			
I _{IH}	High-level input current	Any reset	V _{CC} = MAX, V _I = 2.7 V			20			μA
		CKA or CKB				40			
I _{IL}	Low-level input current	Any reset	V _{CC} = MAX, V _I = 0.4 V			-0.4			mA
		CKA				-2.4			
		CKB				-1.6			
I _{OS}	Short-circuit output current §	V _{CC} = MAX	-20	-100	-20	-100			mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 3	9	15	9	15			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R₀ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS92			'LS93			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	CKA	Q _A	C _L = 15 pF, R _L = 2 kΩ See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q _B		16			16			16			
t _{PLH}	CKA	Q _A		10	16		10	16		10	16		ns
				12	18		12	18		12	18		
t _{PLH}	CKA	Q _D		32	48		32	48		46	70		ns
				34	50		34	50		46	70		
t _{PLH}	CKB	Q _B		10	16		10	16		10	16		ns
				14	21		14	21		14	21		
t _{PLH}	CKB	Q _C		21	32		10	16		21	32		ns
				23	35		14	21		23	35		
t _{PLH}	CKB	Q _D		21	32		21	32		34	51		ns
				23	35		23	35		34	51		
t _{PHL}	Set-to-0	Any		26	40		26	40		26	40		ns
t _{PLH}	Set-to-9	Q _A , Q _D		20	30								ns
		Q _B , Q _C		26	40								

#f_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

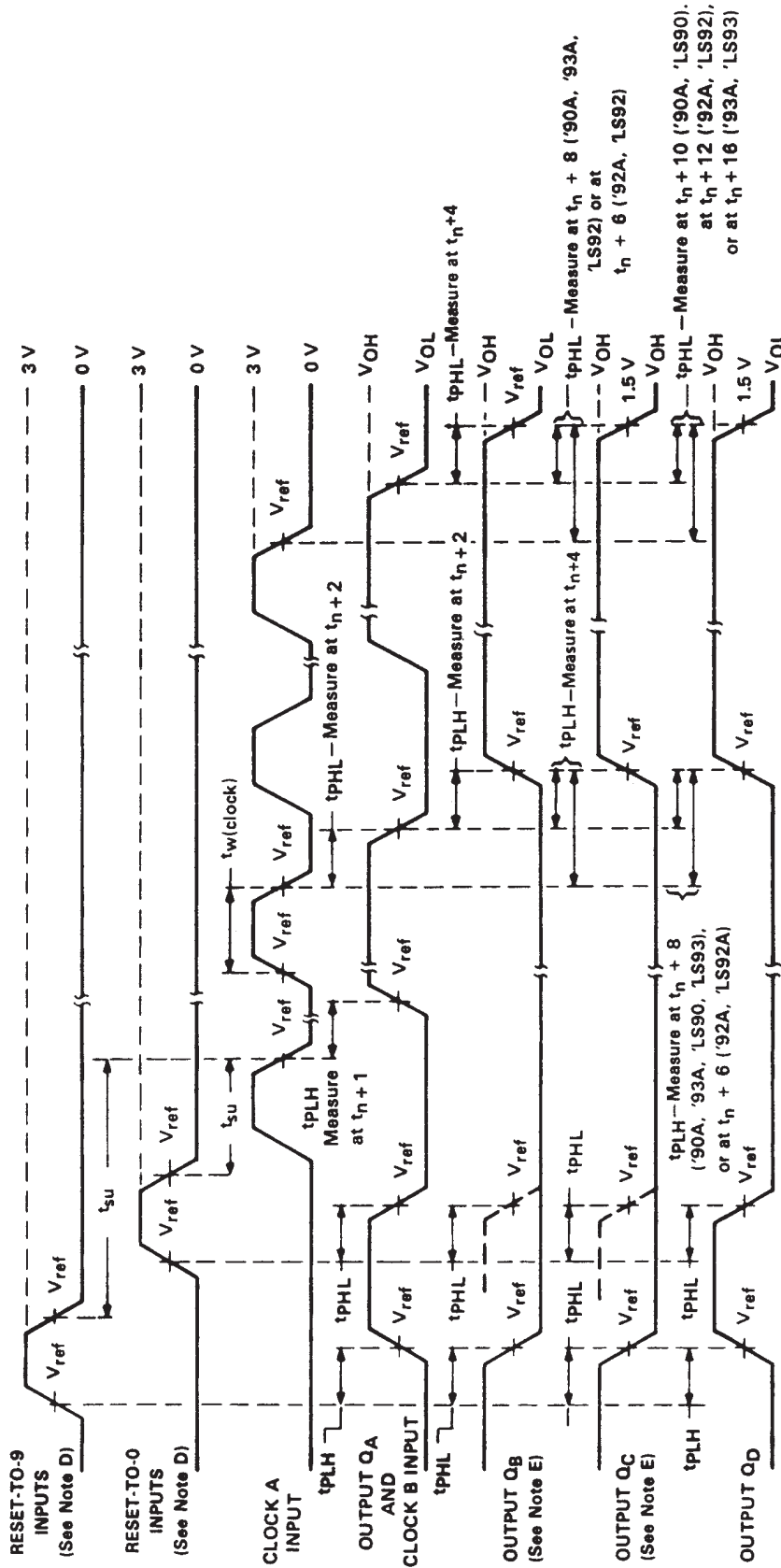
t_{PHL} = propagation delay time, high-to-low-level output



SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93
 SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
 DECADE, DIVIDE-BY-TWELVE AND BINARY COUNTERS

SDLS940A - MARCH 1974 - REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



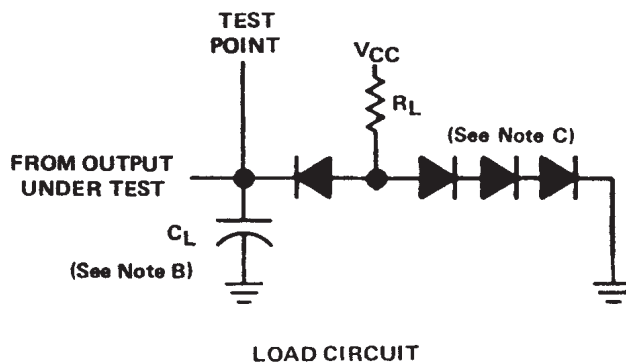
NOTES: A. Input pulses are supplied by a generator having the following characteristics:

- for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
- for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. Each reset input is tested separately with the other reset at 4.5 V.
- E. Reference waveforms are shown with dashed lines.
- F. For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

FIGURE 1A



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. Each reset input is tested separately with the other reset at 4.5 V.
- E. Reference waveforms are shown with dashed lines.
- F. For '90A, '92A, and '93A; $V_{ref} = 1.5$ V. For 'LS90, 'LS92, and 'LS93; $V_{ref} = 1.3$ V.

FIGURE 1B

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
7603201CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
7603201DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
7700101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
7700101DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/31501BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/31501BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/31502BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
JM38510/31502BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN5490AJ	LIFEBUY	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN5492AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54LS90J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54LS93J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN7490AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7492AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7493AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS90D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS90DE4	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS90DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS90DRE4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS90N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS90NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS92D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92DE4	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92DRE4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS92N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS92NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92NSRE4	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93DE4	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93DR	ACTIVE	SOIC	D	14	2500	Pb-Free	CU NIPDAU	Level-2-260C-1 YEAR/

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						(RoHS)		Level-1-235C-UNLIM
SN74LS93DRE4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS93N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS93NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS93NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93NSRE4	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ5490AJ	LIFEBUY	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ5490AW	LIFEBUY	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ5492AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ5492AW	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54LS90J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS90W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS93J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS93W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265