

SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

SDLS004

D2633, JANUARY 1981 — REVISED MARCH 1988

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Accurate Counter Frequency: DC to 20 MHz

description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going \overline{RCO} pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to CCK of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (CCKEN, \overline{CCKEN}) inputs. A register clock enable (RCKEN) is also provided.

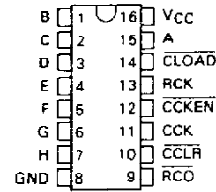
OUTPUT ENABLE CONTROL ('593 ONLY)

G	\overline{G}	A/Q _A thru H/Q _H
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

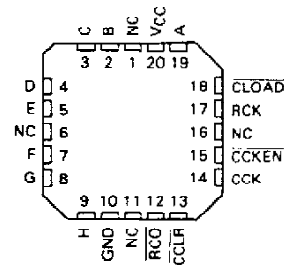
COUNTER CLOCK ENABLE CONTROL

CCKEN	\overline{CCKEN}	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

SN54LS592 . . . J OR W PACKAGE SN74LS592 . . . N PACKAGE (TOP VIEW)

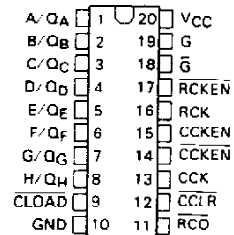


SN54LS592 . . . FK PACKAGE (TOP VIEW)

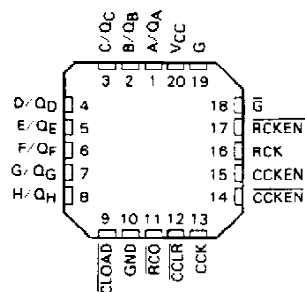


NC — No internal connection

SN54LS593 . . . J OR W PACKAGE SN74LS593 . . . DW OR N PACKAGE (TOP VIEW)



SN54LS593 . . . FK PACKAGE (TOP VIEW)



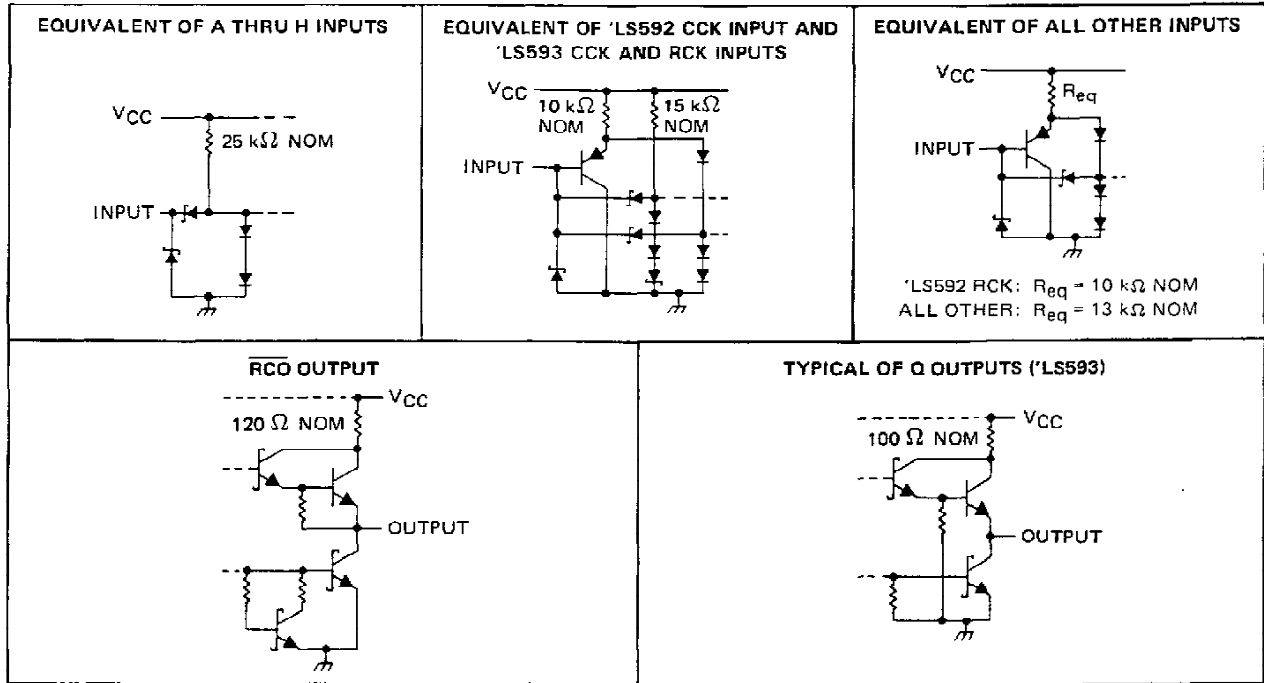
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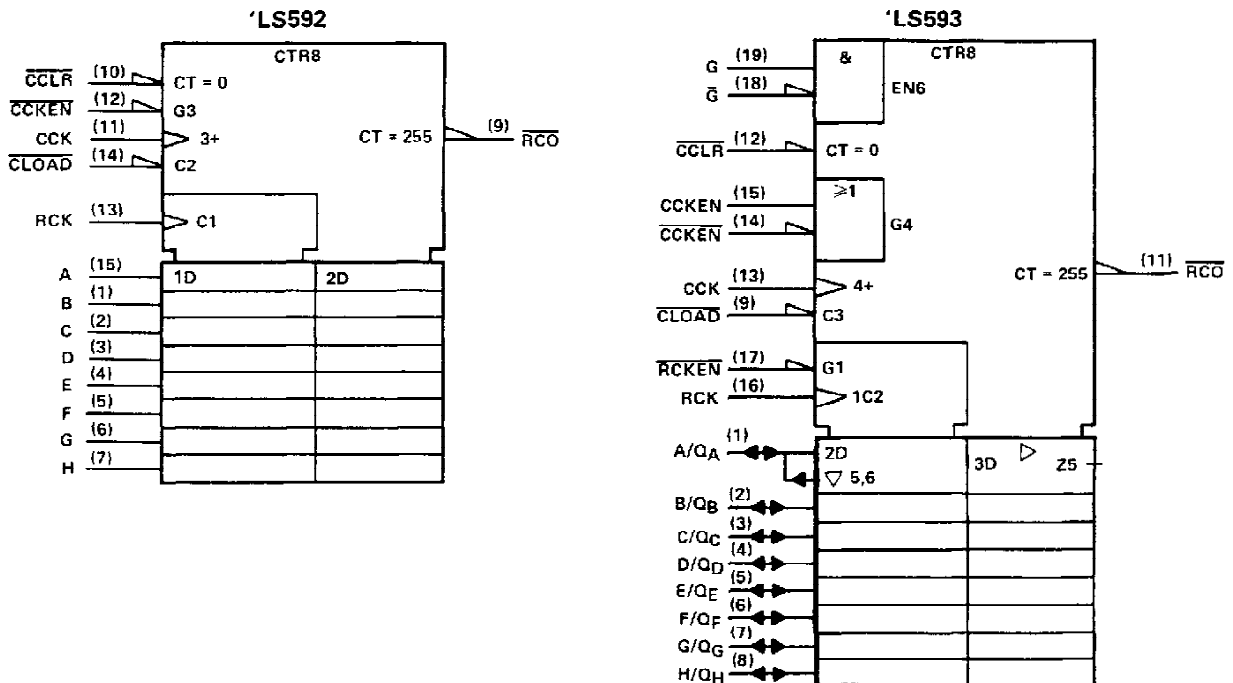
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SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

schematics of inputs and outputs



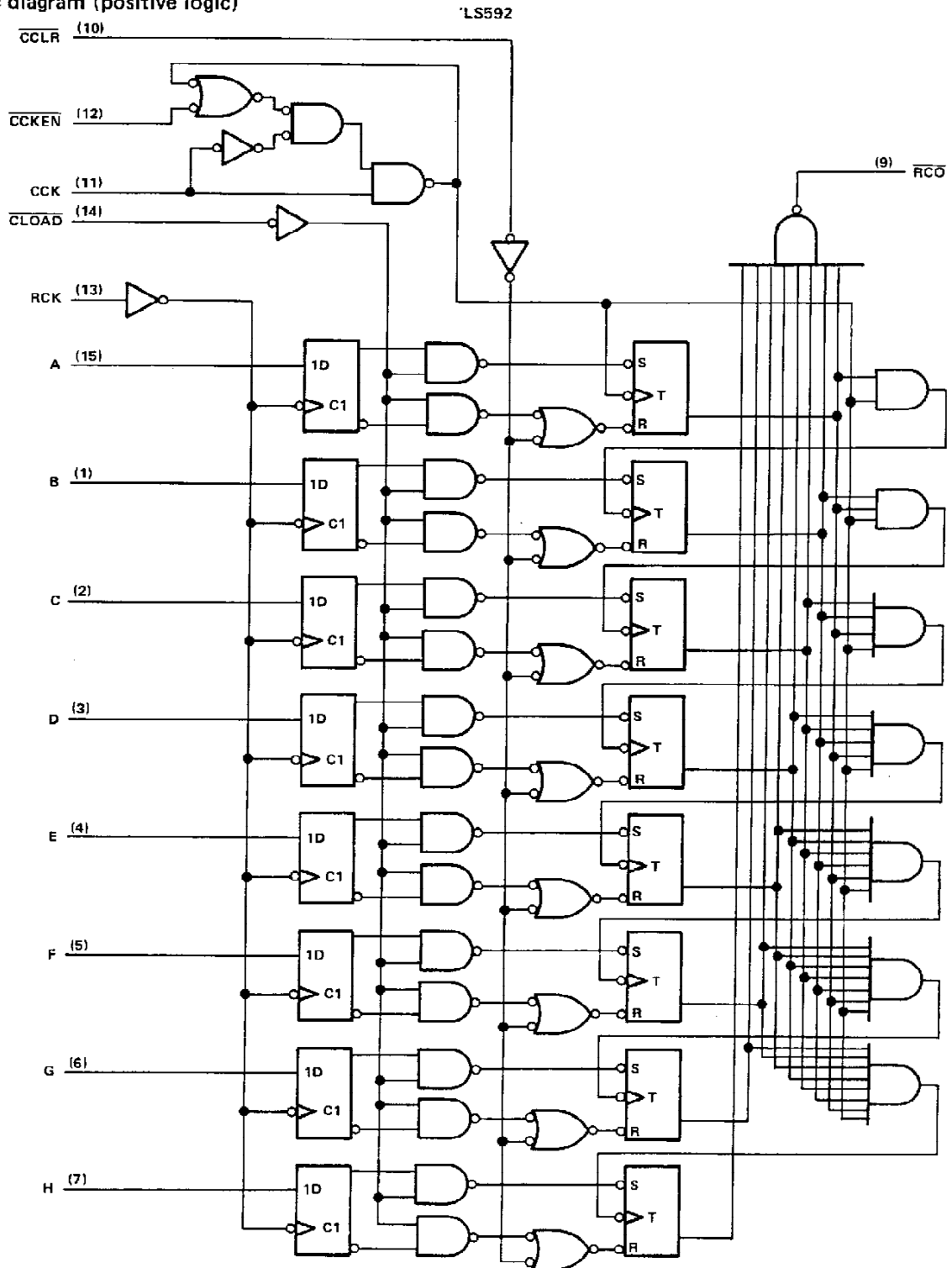
logic symbols †



† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

SN54LS592, SN74LS592 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

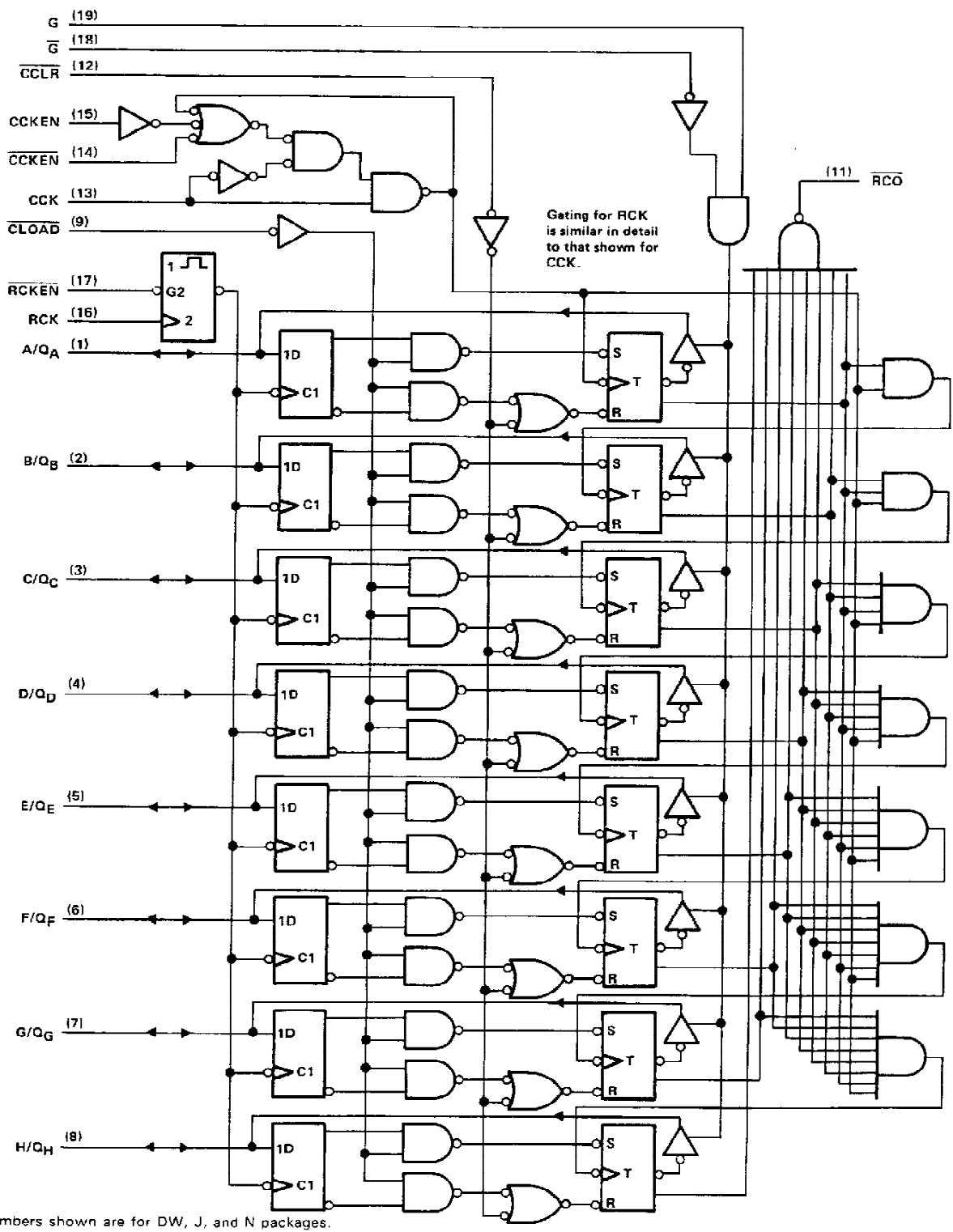


Pin numbers shown are for J, N, and W packages.

SN54LS593, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic diagram (positive logic)

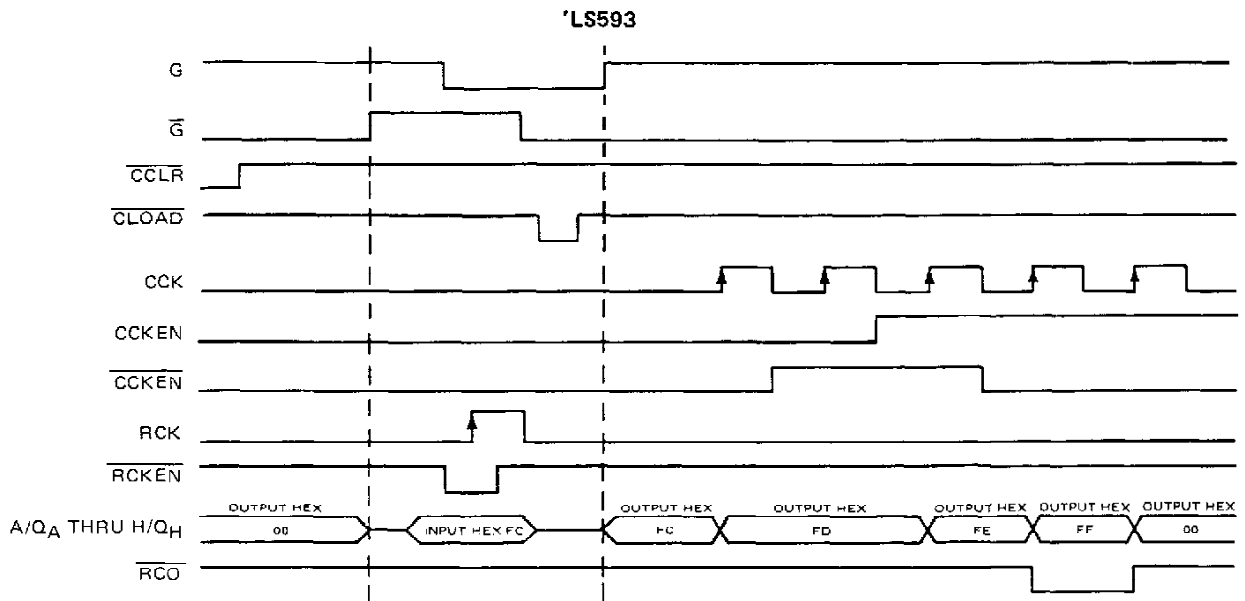
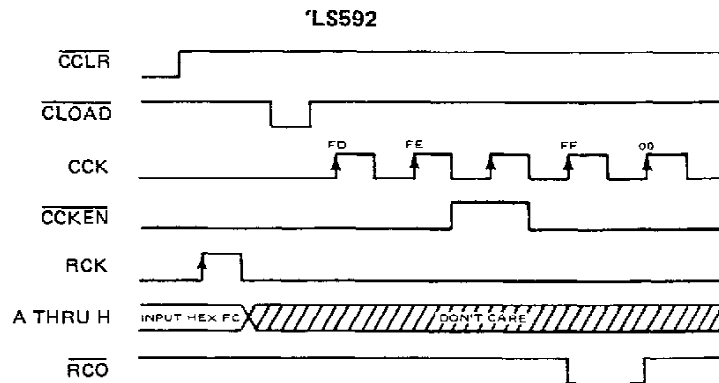
'LS593



Pin numbers shown are for DW, J, and N packages.

**SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS**

typical operating sequences



SN54LS592, SN54LS593, SN74LS592, SN74LS593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593	-55°C to 125°C
SN74LS592, SN74LS593	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current	\overline{RCK}		-1	\overline{RCK}		-1	mA
		Q 'LS593 only		-1	Q 'LS593 only		-2.6	
I_{OL}	Low-level output current	\overline{RCK}		8	\overline{RCK}		16	mA
		Q 'LS593 only		12	Q 'LS593 only		24	
f_{CCK}	Counter clock frequency	0		20	0		20	MHz
$t_w(\overline{CCK})$	Duration of counter clock pulse	25			25			ns
$t_w(\overline{CCLR})$	Duration of counter clear pulse	20			20			ns
$t_w(\overline{RCK})$	Duration of register clock pulse	20			20			ns
$t_w(\overline{CLOAD})$	Duration of counter load pulse	40			40			ns
t_{su}	Register enable setup time	\overline{RCKEN} low to $\overline{RCK} \uparrow$, 'LS593		20	\overline{RCKEN} low to $\overline{RCK} \uparrow$, 'LS593		20	ns
t_{su}	Counter enable setup time before $\overline{CCK} \uparrow$	\overline{CCKEN} low, 'LS592		30	\overline{CCKEN} low, 'LS592		30	ns
		\overline{CCKEN} low or \overline{CCKEN} high, 'LS593		30	\overline{CCKEN} low or \overline{CCKEN} high, 'LS593		30	
t_{su}	Setup time	\overline{CCLR} inactive before $\overline{CCK} \uparrow$		20	\overline{CCLR} inactive before $\overline{CCK} \uparrow$		20	ns
		\overline{CLOAD} inactive before $\overline{CCK} \uparrow$		20	\overline{CLOAD} inactive before $\overline{CCK} \uparrow$		20	
		$\overline{RCK} \uparrow$ before $\overline{CLOAD} \uparrow$ (see Note 2)		30	$\overline{RCK} \uparrow$ before $\overline{CLOAD} \uparrow$ (see Note 2)		30	
		Data A thru H before $\overline{RCK} \uparrow$		20	Data A thru H before $\overline{RCK} \uparrow$		20	
t_h	Hold time	Data A thru H after $\overline{RCK} \uparrow$		0	Data A thru H after $\overline{RCK} \uparrow$		0	ns
		All others		0	All others		0	
T_A	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: This time insures the data saved by $\overline{RCK} \uparrow$ will also be loaded into the counter.



SN54LS592, SN54LS593, SN74LS592, SN74LS593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
		MIN	TYP‡	MAX	MIN	
V_{IK}	$V_{CC} = \text{MIN.}, I_I = -18 \text{ mA}$					V
V_{OH}	$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX.}$	$I_{OH} = -1 \text{ mA}$				V
		$I_{OH} = -2.6 \text{ mA}$		2.4 3.1		
		$I_{OH} = -1 \text{ mA}$		2.4 3.2		
V_{OL}	$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V.}$ $V_{IL} = \text{MAX.}$	$I_{OL} = 12 \text{ mA}$		0.25 0.4		V
		$I_{OL} = 24 \text{ mA}$		0.35 0.5		
		$I_{OL} = 8 \text{ mA}$		0.25 0.4		
		$I_{OL} = 16 \text{ mA}$		0.35 0.5		
I_{OZH}	$V_{CC} = \text{MAX.}, V_{IH} = 2 \text{ V.}$ $V_O = 2.7 \text{ V}$			20		μA
I_{OZL}	$V_{CC} = \text{MAX.}, V_{IH} = 2 \text{ V.}$ $V_O = 0.4 \text{ V}$			-0.4		mA
I_I	$V_{CC} = \text{MAX.}$	$V_I = 5.5 \text{ V}$		0.1		mA
		$V_I = 7 \text{ V}$		0.1		
I_{IH}	$V_{CC} = \text{MAX.}, V_I = 2.7 \text{ V}$			20		μA
I_{IL}	$V_{CC} = \text{MAX.}, V_I = 0.4 \text{ V}$	CCK		-0.8		mA
		RCK	'LS592	-0.2		
			'LS593	-0.8		
		A thru H		-0.4		
		Others		-0.2		
I_{OS}^{\S}	$V_{CC} = \text{MAX.}, V_O = 0 \text{ V}$	'LS593 Q		-30 -130		mA
		RCO		-20 -100		
I_{CC}	$V_{CC} = \text{MAX.}$ All possible inputs grounded, All outputs open	'LS592	I_{CCH}	40 60		mA
			I_{CCL}	40 60		
		'LS593	I_{CCH}	47 70		
			I_{CCL}	53 80		
			I_{CCZ}	57 85		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V.}, T_A = 25^\circ\text{C.}$

§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS592			'LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK ↑	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	20	35		20	35		MHz
t_{PLH}	CCK ↑	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$				14	21		ns
t_{PHL}	CCK ↑	Q					26	39		ns
t_{PLH}	\overline{CLOAD} ↓	Q					34	51		ns
t_{PHL}	\overline{CLOAD} ↓	Q					28	42		ns
t_{PHL}	\overline{CCLR} ↓	Q					25	38		ns
t_{PZH}	G ↑	Q					31	47		ns
t_{PZL}	G ↑	Q					27	40		ns
t_{PZH}	\overline{G} ↓	Q					29	45		ns
t_{PZL}	\overline{G} ↓	Q					31	47		ns
t_{PHZ}	G ↓	Q					33	50		ns
t_{PLZ}	G ↓	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$				35	52		ns
t_{PHZ}	\overline{G} ↑	Q					26	39		ns
t_{PLZ}	\overline{G} ↑	Q					28	42		ns
t_{PLH}	CCK ↑	\overline{RCO}								
t_{PHL}	CCK ↑	\overline{RCO}	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	15	23		14	21		ns
t_{PLH}	\overline{CLOAD} ↓	\overline{RCO}		20	30		20	30		ns
t_{PHL}	\overline{CLOAD} ↓	\overline{RCO}		31	47		31	47		ns
t_{PLH}	\overline{CCLR} ↓	\overline{RCO}		27	41		27	41		ns
t_{PHL}	\overline{CCLR} ↓	\overline{RCO}		30	45		30	45		ns
t_{PLH}	RCK ↑	\overline{RCO}	$R_L = 1\text{ k}\Omega$; $C_L = 30\text{ pF}$ $\overline{CLOAD} = L$	35	53		42	63		ns
t_{PHL}	RCK ↑	\overline{RCO}		30	45		33	50		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-87621012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS592N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS592NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS592NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS593N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS593NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS593NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS593W	OBSOLETE			20		TBD	Call TI	Call TI
SNJ54LS593W	OBSOLETE			20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

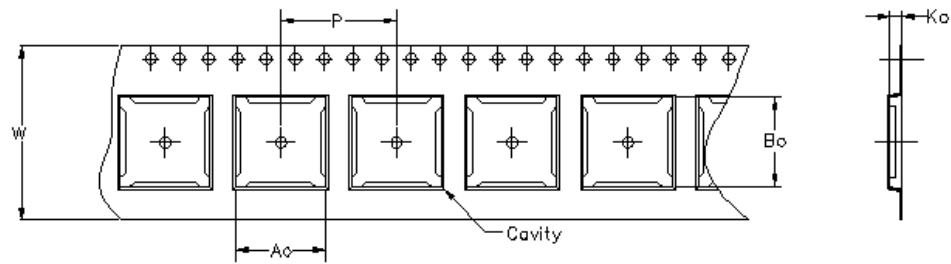
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

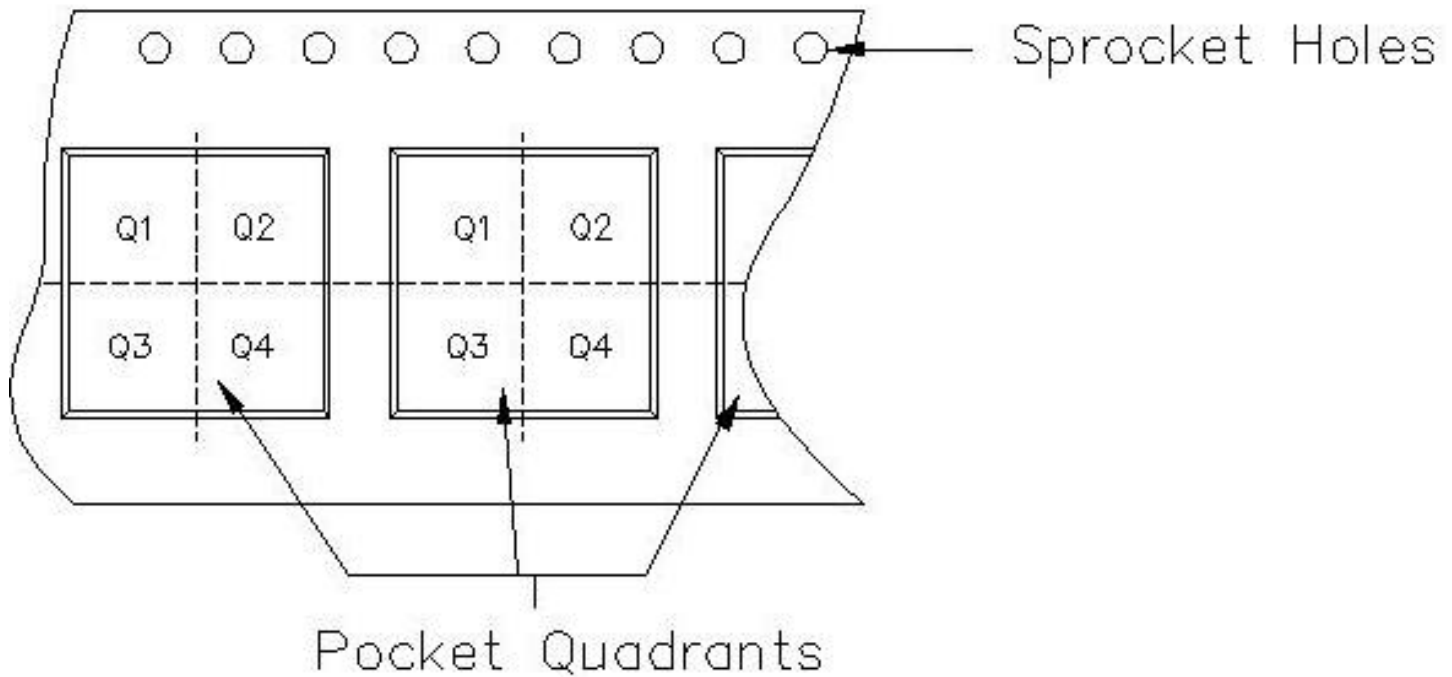
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



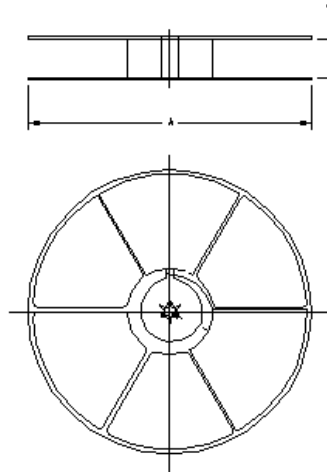
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



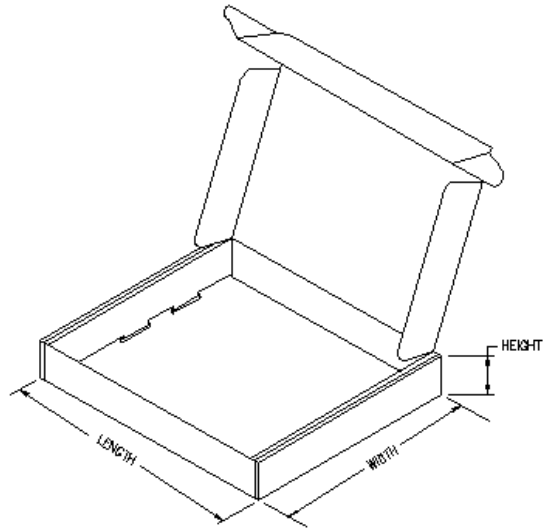
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS592DR	D	16	FMX	330	16	6.5	10.3	2.1	8	16	Q1
SN74LS592NSR	NS	16	MLA	330	16	8.2	10.5	2.5	12	16	Q1
SN74LS593DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74LS593NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LS592DR	D	16	FMX	342.9	336.6	28.58
SN74LS592NSR	NS	16	MLA	342.9	336.6	28.58
SN74LS593DWR	DW	20	MLA	333.2	333.2	31.75
SN74LS593NSR	NS	20	MLA	333.2	333.2	31.75



J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

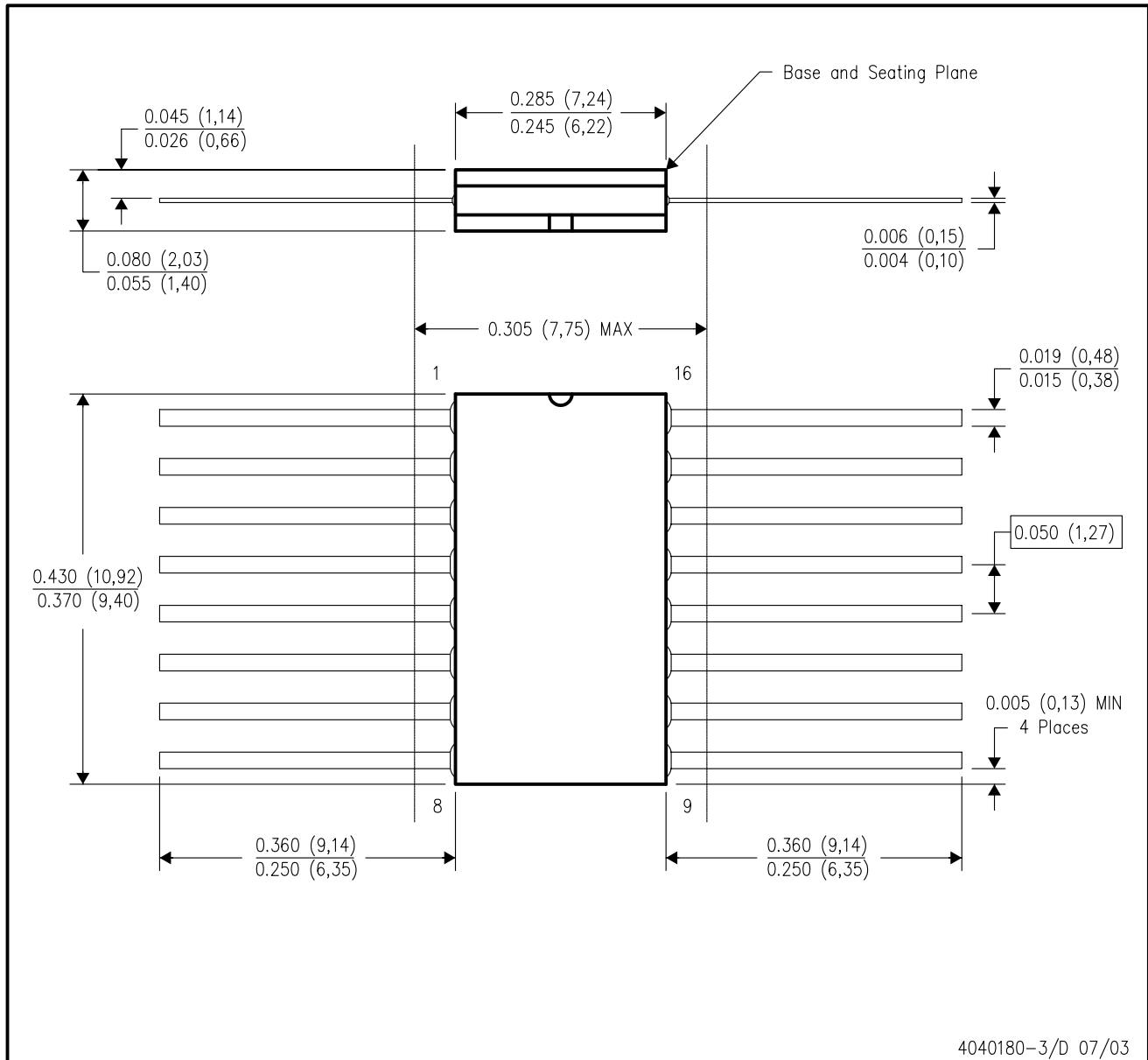


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-87621012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS592N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS592NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS592NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS593N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS593NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS593NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS593NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS593W	OBSOLETE			20		TBD	Call TI	Call TI
SNJ54LS593W	OBSOLETE			20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

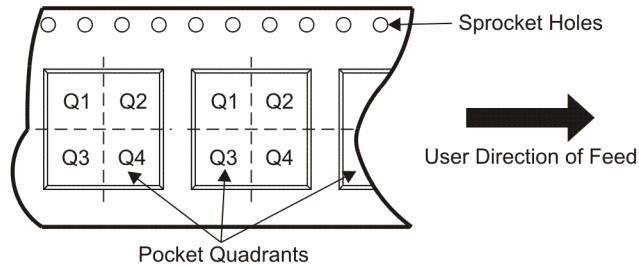
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TAPE AND REEL INFORMATION



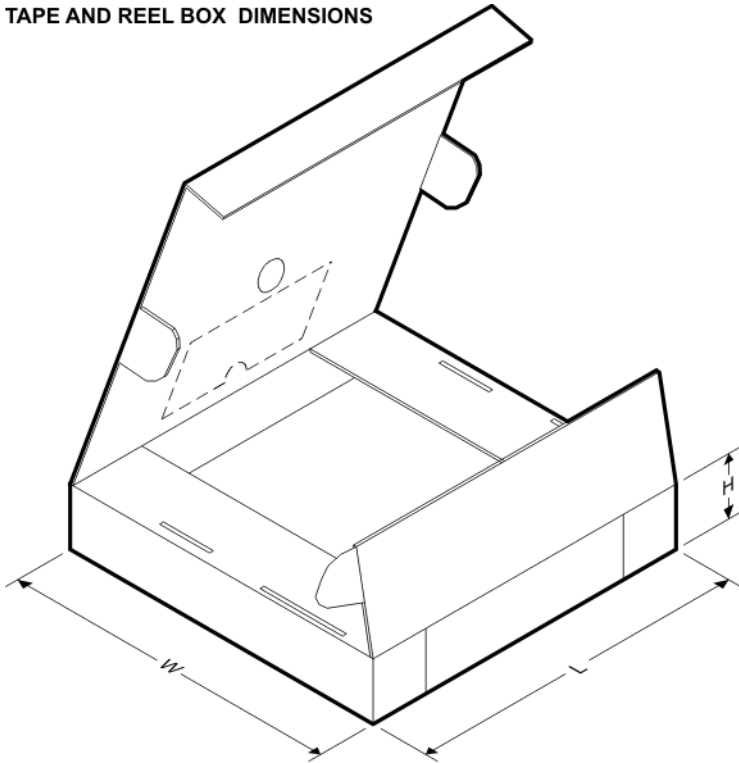
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS592DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS592NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS593DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS593NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



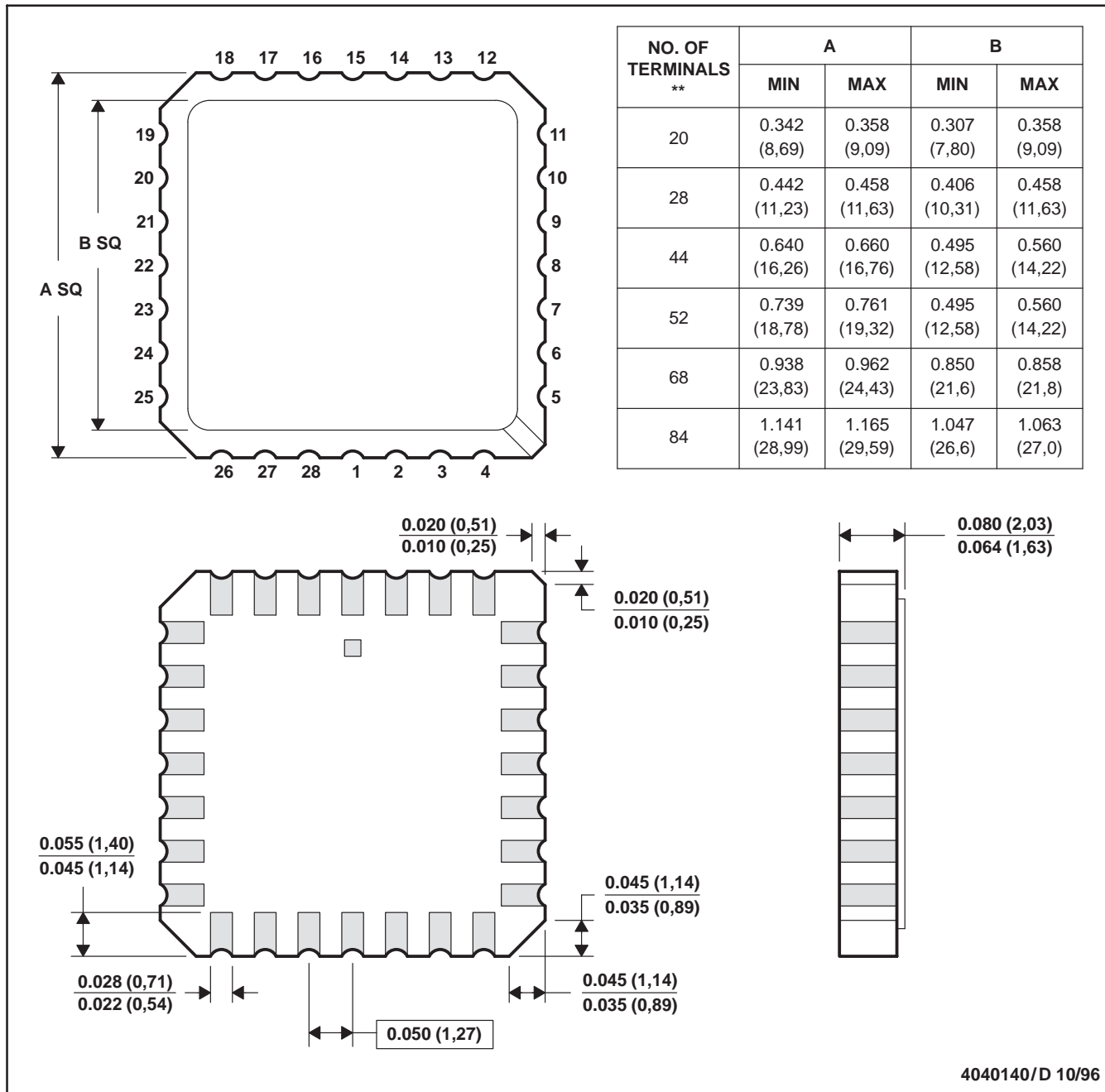
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS592DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS592NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LS593DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LS593NSR	SO	NS	20	2000	346.0	346.0	41.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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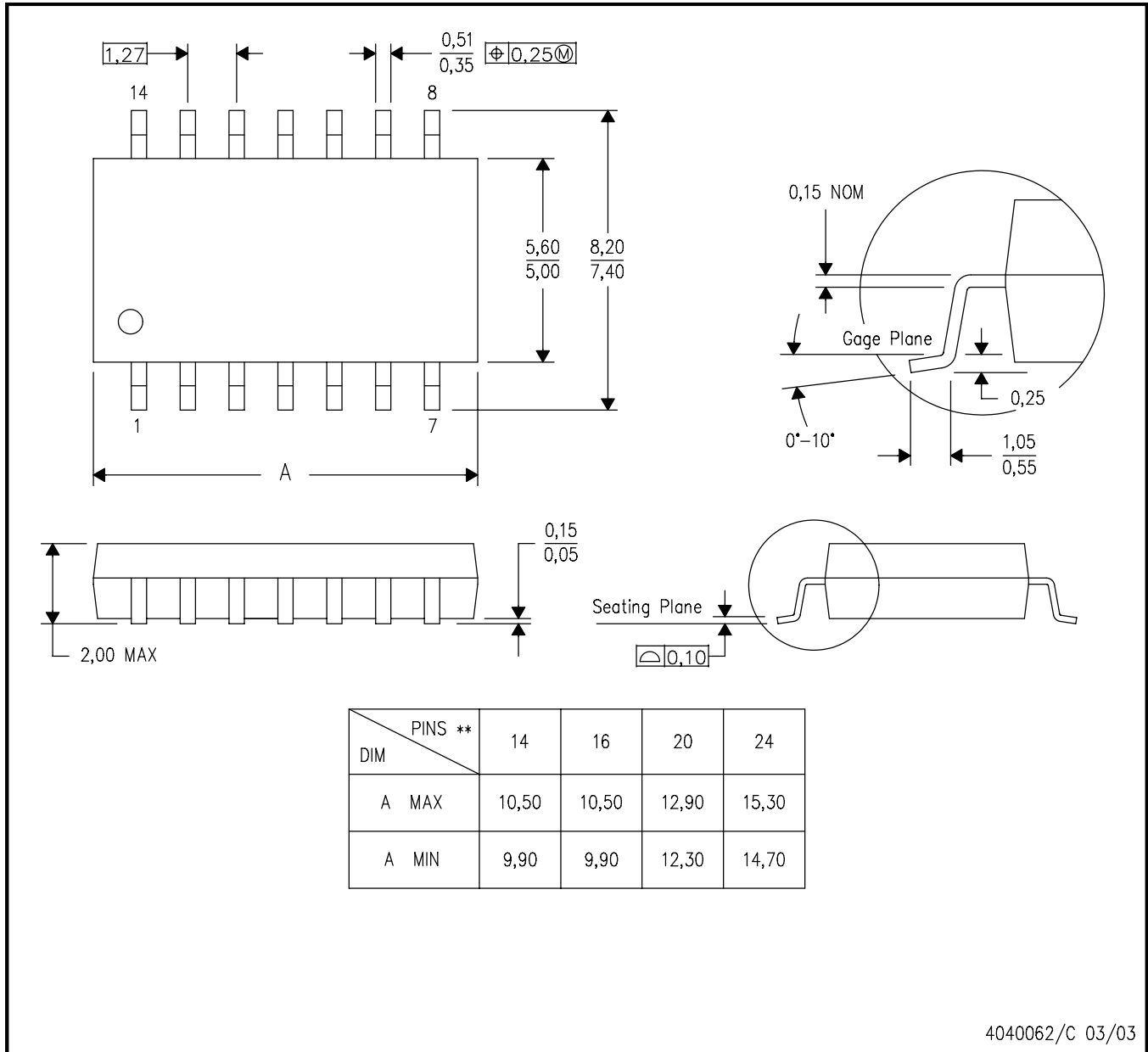
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

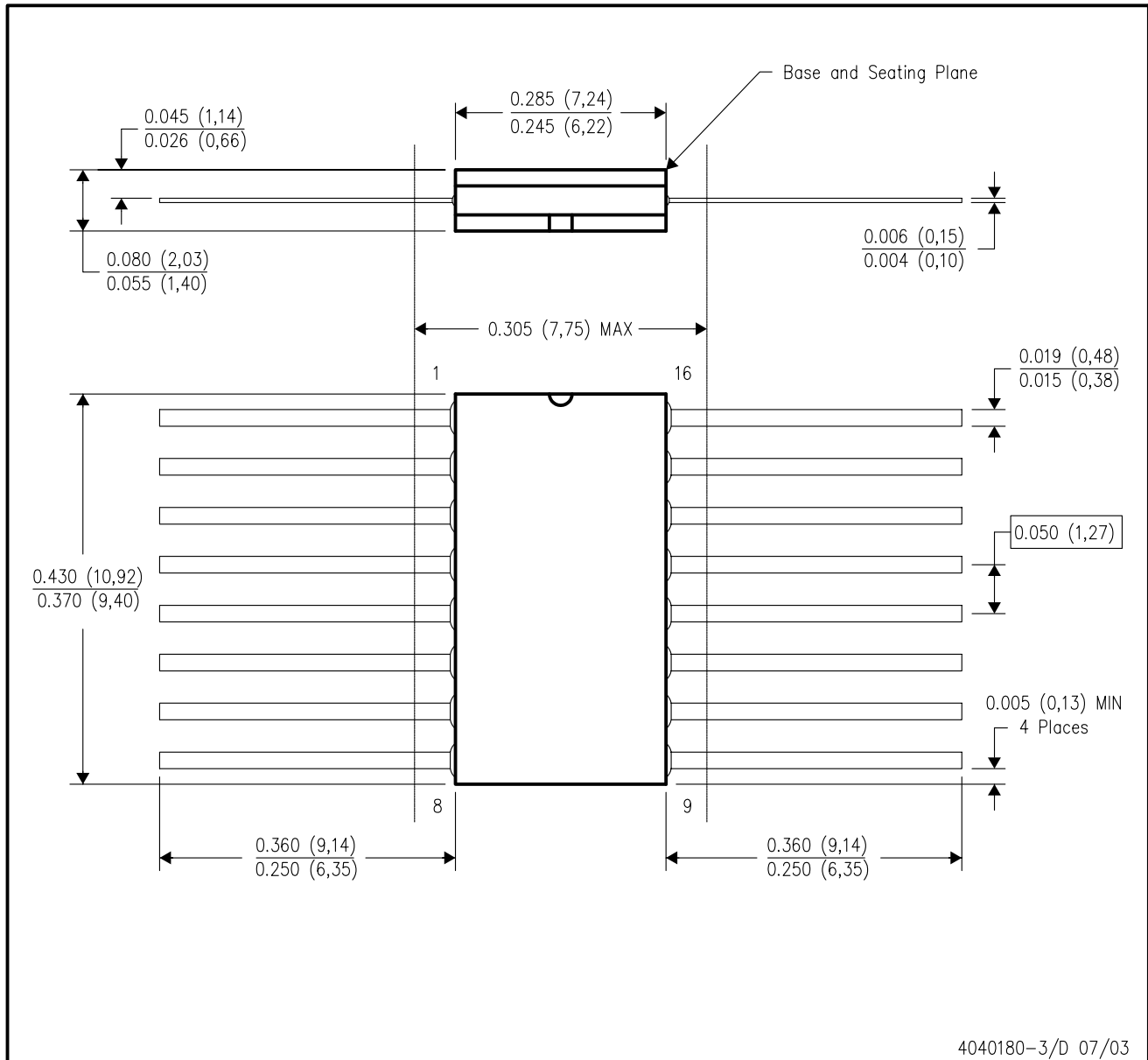
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

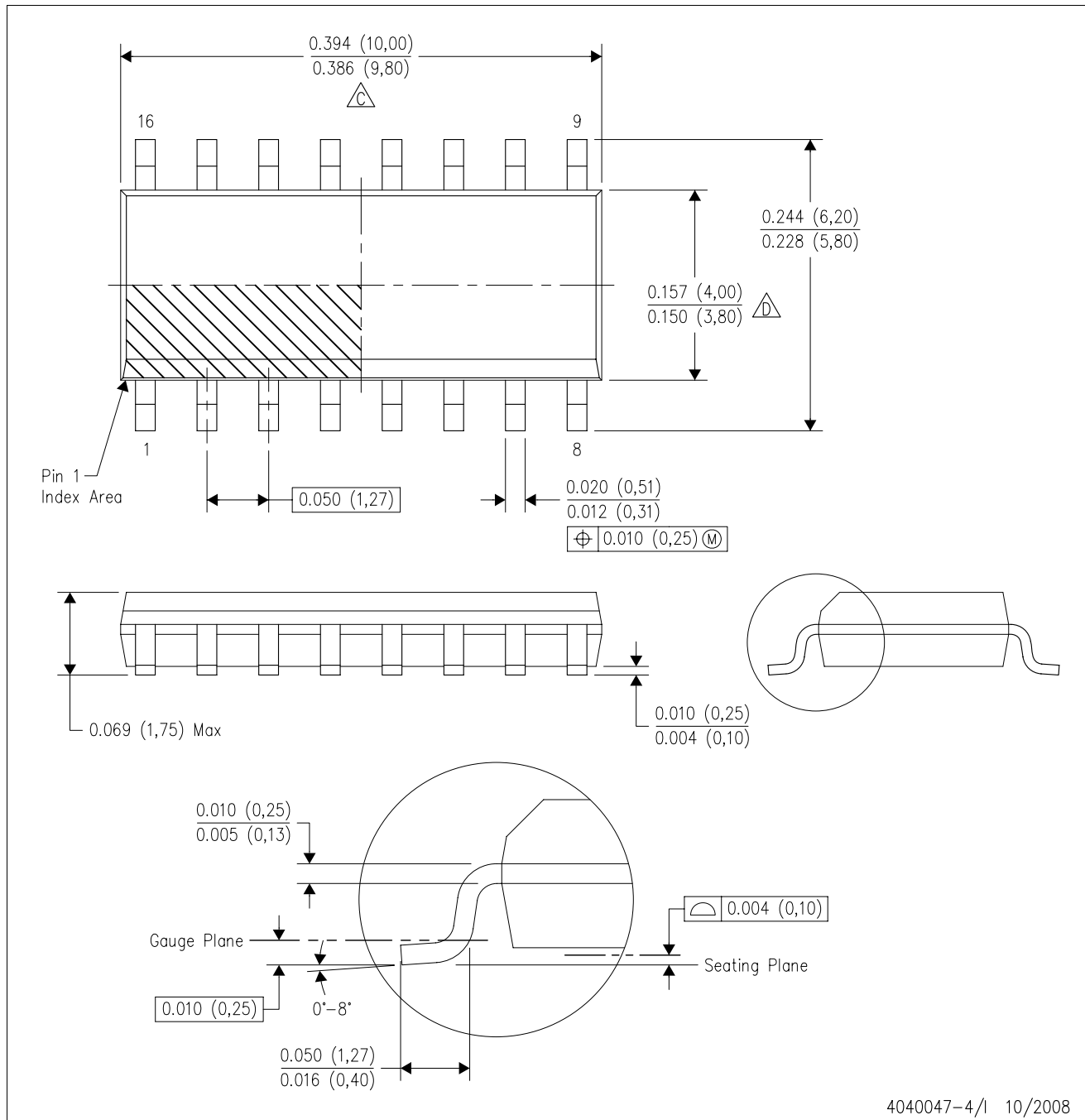
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

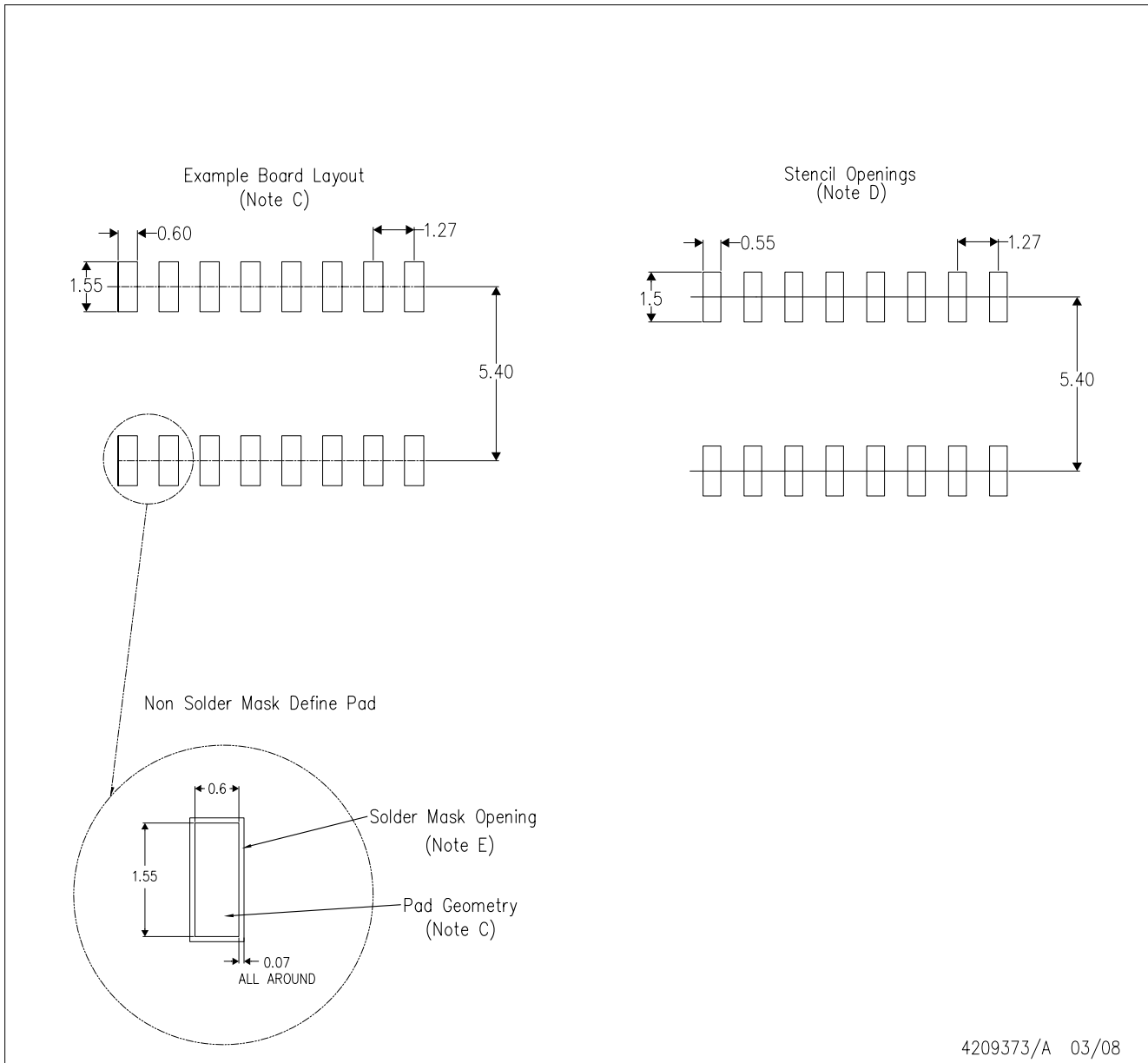
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)

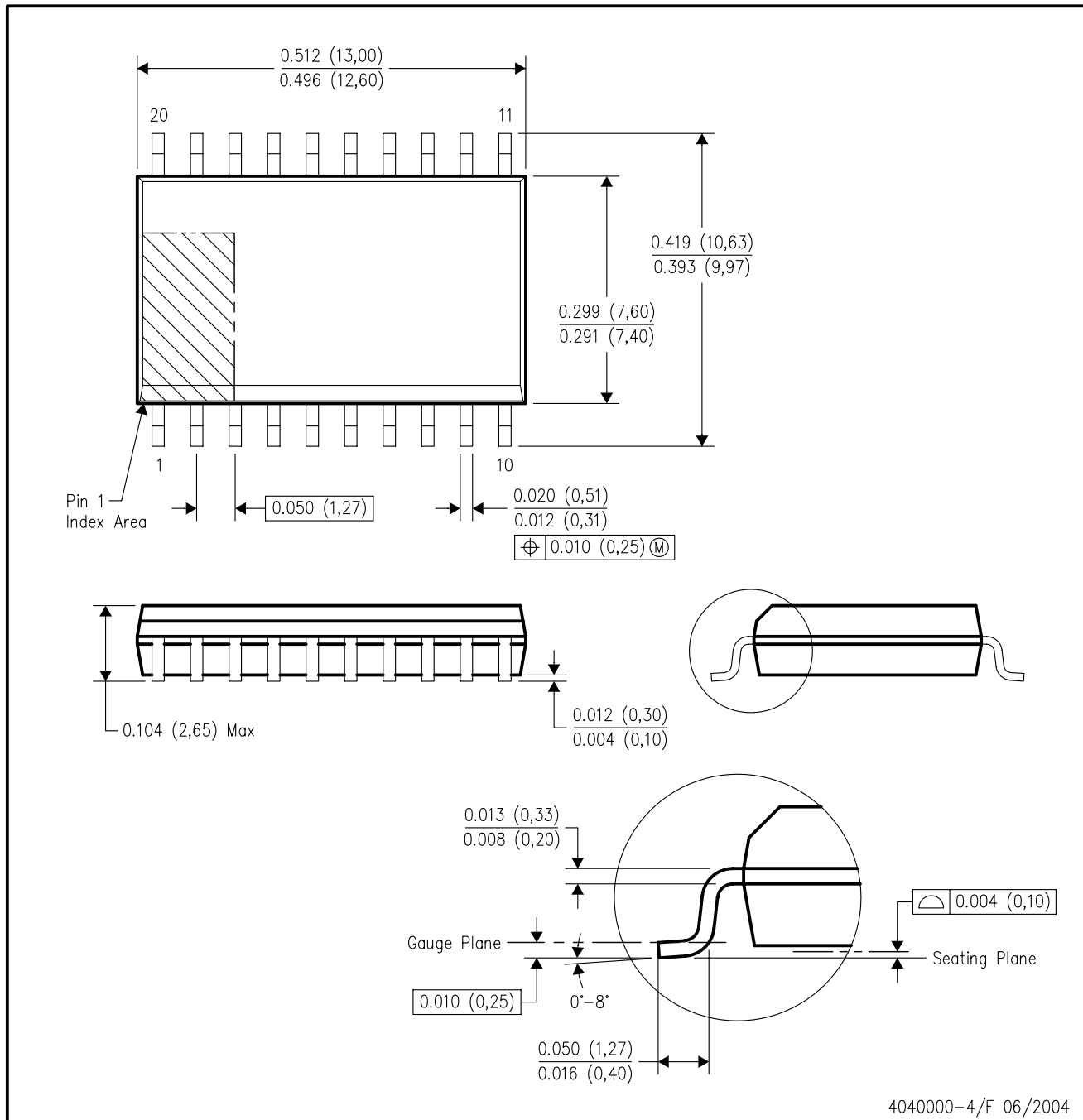


4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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