

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

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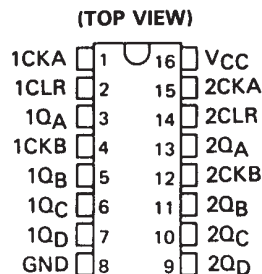
- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual $\div 2$ and $\div 5$ Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

description

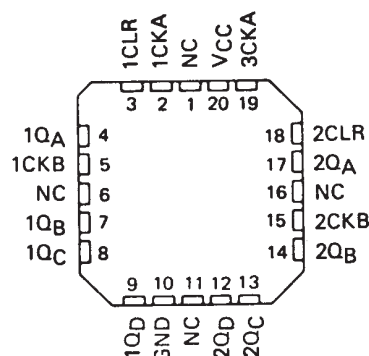
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C .

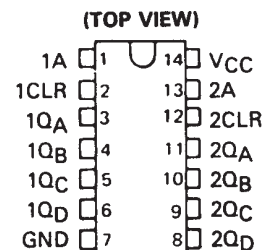
SN54390, SN54LS390 . . . J OR W PACKAGE SN74390 . . . N PACKAGE SN74LS390 . . . D OR N PACKAGE



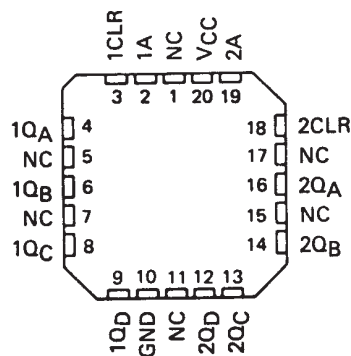
SN54LS390 . . . FK PACKAGE



SN54393, SN54LS393 . . . J OR W PACKAGE SN74393 . . . N PACKAGE SN74LS393 . . . D OR N PACKAGE



SN54LS393 . . . FK PACKAGE



NC - No internal connection

SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

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'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

FUNCTION TABLES
'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

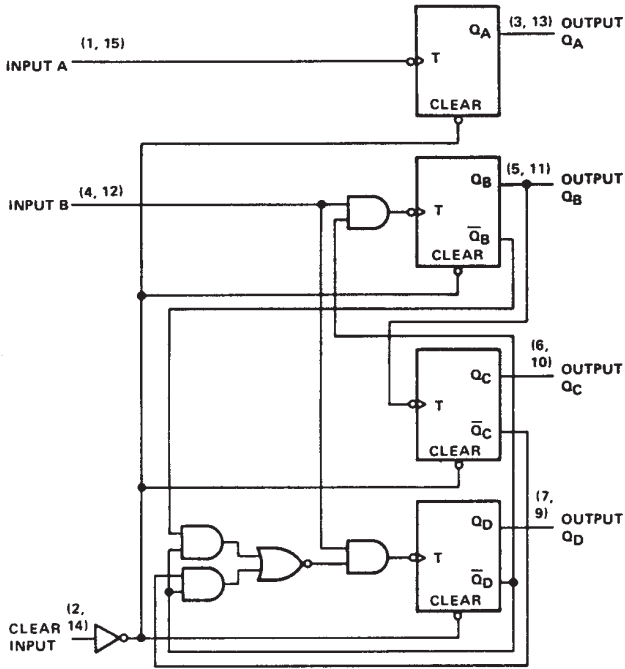
'393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

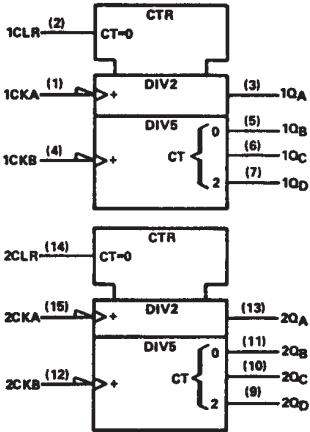
logic diagrams (positive logic)

'390, 'LS390

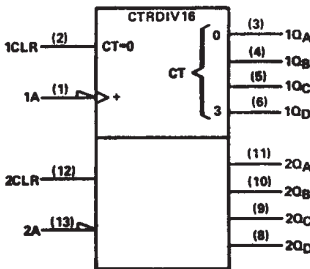


logic symbols†

'390, 'LS390



'393, 'LS393



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

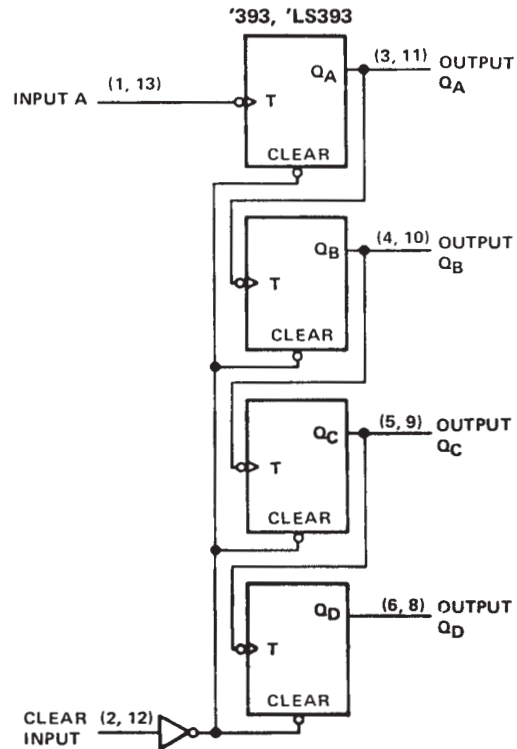
Pin numbers shown are for D, J, N, and W packages.



SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

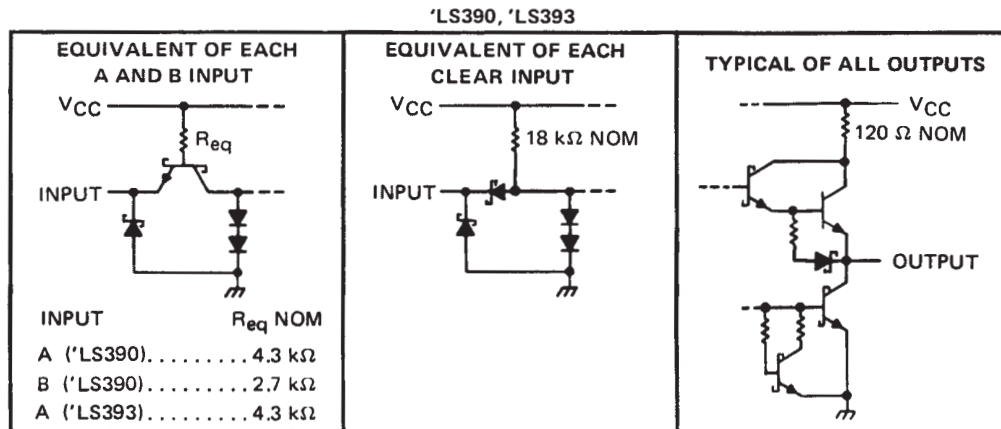
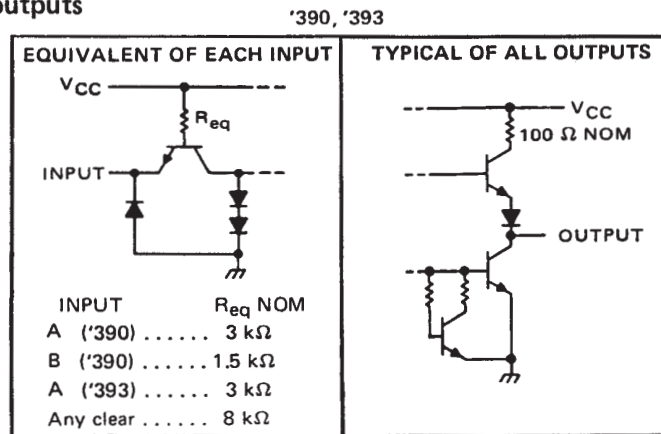
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logic diagrams (continued)



Pin numbers shown are for D, J, N and W packages.

schematics of inputs and outputs



SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	–55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54390 SN54393			SN74390 SN74393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–800			–800	μ A
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		20	0		20	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	25			25			
	Clear high	20			20			
Clear inactive-state setup time, t_{su}		25↓			25↓			ns
Operating free-air temperature, T_A		–55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'390			'393			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				–1.5			–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}¶$			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
I_{IH}	High-level input current	Clear				40			40	μ A
		Input A	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			80			80	
		Input B				120				
I_{IL}	Low-level input current	Clear				–1			–1	mA
		Input A	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–3.2			–3.2	
		Input B				–4.8				
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54'	–20		–57	–20		–57	mA
			SN74'	–18		–57	–18		–57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		42		69	38		64	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ The Q_A outputs of the '390 are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

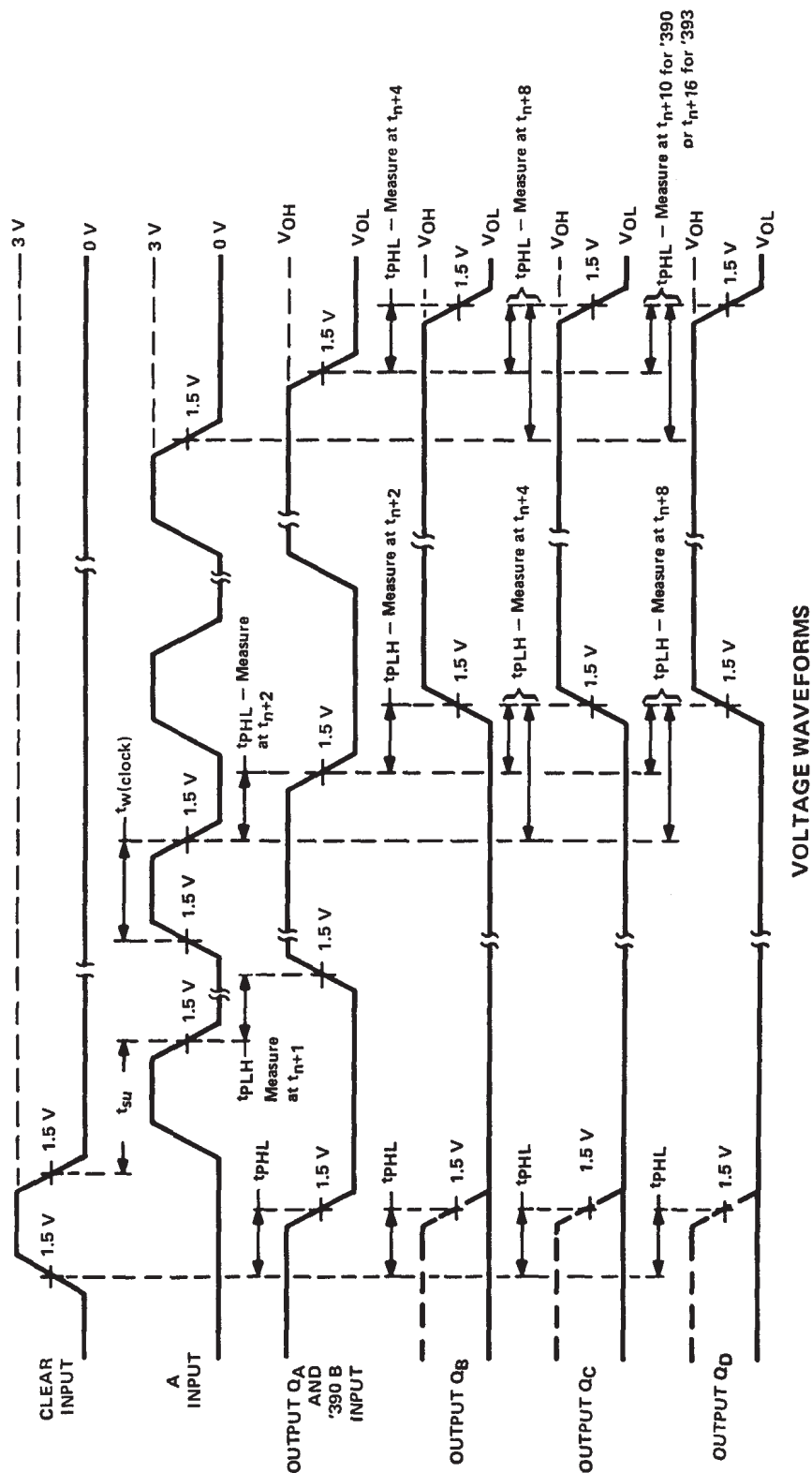
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 400 Ω, See Note 3 and Figure 1	25	35		25	35		MHz
	B	Q _B		20	30					
t _{PLH}	A	Q _A			12	20		12	20	ns
t _{PHL}					13	20		13	20	
t _{PLH}	A	Q _C of '390 Q _D of '393			37	60		40	60	ns
t _{PHL}					39	60		40	60	
t _{PLH}	B	Q _B			13	21				ns
t _{PHL}					14	21				
t _{PLH}	B	Q _C			24	39				ns
t _{PHL}					26	39				
t _{PLH}	B	Q _D			13	21				ns
t _{PHL}					14	21				
t _{PHI}	Clear	Any			24	39		24	39	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

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PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $PRR = 1 \text{ MHz}$, duty cycle = 50%, $Z_{out} \approx 50 \text{ ohms}$.

FIGURE 1

SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Clear input voltage	7 V
Any A or B clock input voltage	5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393	–55°C to 125°C
SN74LS390, SN74LS393	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		–400			–400			μ A
Low-level output current, I_{OL}		4			8			mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		12.5	0		12.5	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	40			40			
	Clear high	20			20			
Clear inactive-state setup time, t_{su}		25↓			25↓			ns
Operating free-air temperature, T_A		–55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				–1.5			–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$	$I_{OL} = 4 \text{ mA}^\S$	0.25	0.4		0.25	0.4		V
			$I_{OL} = 8 \text{ mA}^\S$				0.35	0.5		
I_I	Input current at maximum input voltage	Clear Input A Input B $V_{CC} = \text{MAX}$	$V_I = 7 \text{ V}$		0.1			0.1		mA
			$V_I = 5.5 \text{ V}$		0.2			0.2		
					0.4			0.4		
I_{IH}	High-level input current	Clear Input A Input B $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			0.02			0.02		mA
					0.1			0.1		
					0.2			0.2		
I_{IL}	Low-level input current	Clear Input A Input B $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–0.4			–0.4		mA
					–1.6			–1.6		
					–2.4			–2.4		
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		–20		–100	–20		–100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS390	15		26	15		26	mA
			'LS393	15		26	15		26	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ The Q_A outputs of the 'LS390 are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

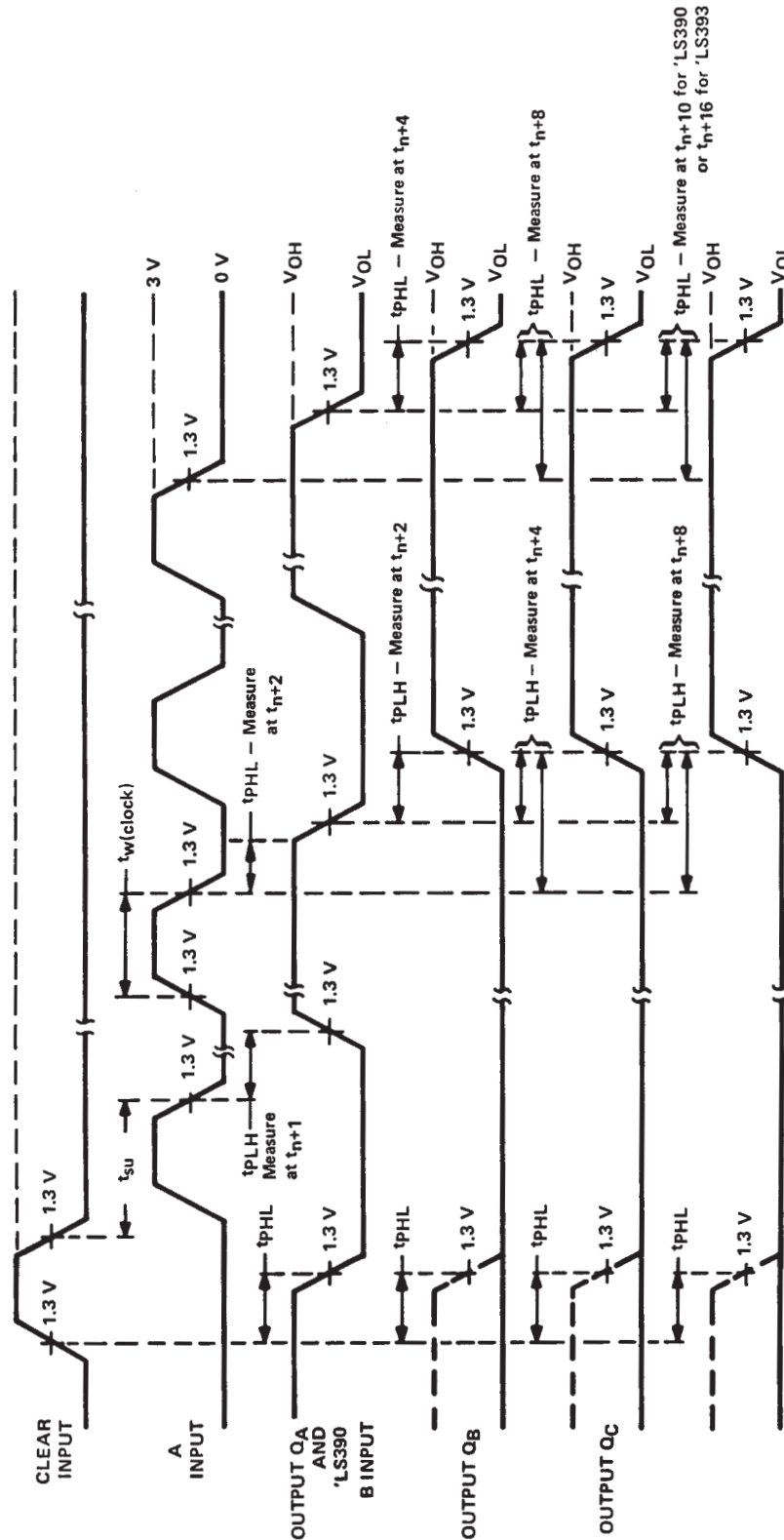
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}	A	Q _A	C _L = 15 pF, R _L = 2 kΩ, See Note 4 and Figure 2	25	35		25	35		MHz
	B	Q _B		12.5	20					
t _{PLH}	A	Q _A			12	20		12	20	ns
t _{PHL}					13	20		13	20	
t _{PLH}	A	Q _C of 'LS390 Q _D of 'LS393			37	60		40	60	ns
t _{PHL}					39	60		40	60	
t _{PLH}	B	Q _B			13	21				ns
t _{PHL}					14	21				
t _{PLH}	B	Q _C			24	39				ns
t _{PHL}					26	39				
t _{PLH}	B	Q _D			13	21				ns
t _{PHL}					14	21				
t _{PHL}	Clear	Any			24	39		24	39	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE A: Input pulses are supplied by a generator having the following characteristics $t_f \leq 15$ ns, $t_r \leq 6$ ns, PRR = 1 MHz, duty cycle = 50 %, $Z_{out} \approx 50$ ohms.

FIGURE 2

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
7802601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702SCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702SCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/32702SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74390N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74390N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74393N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
no Sb/Br)								
SN74LS390DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS390N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS390NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS390NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS393DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS393N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS393N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS393NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54393J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ54393W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54393W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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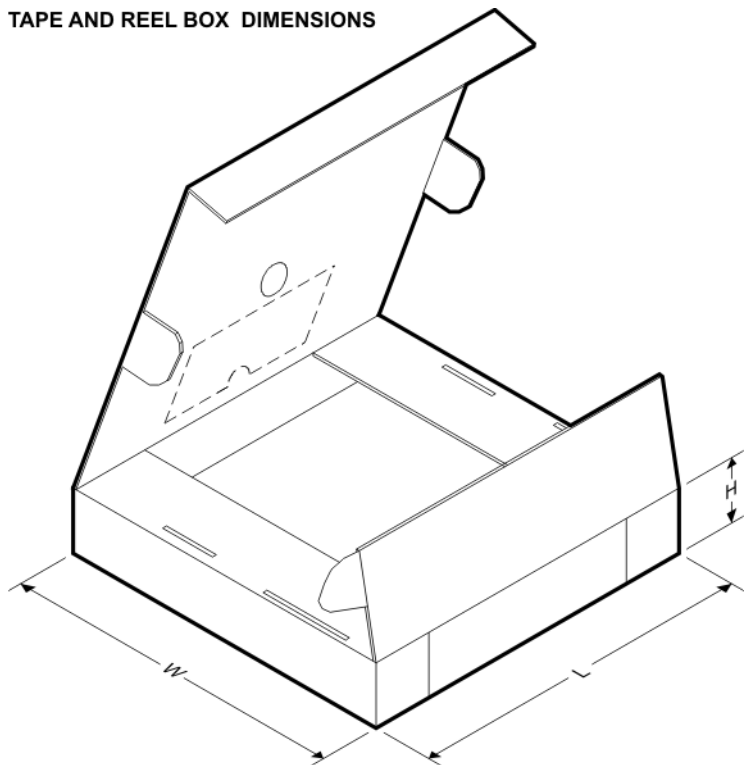
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS390NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS393DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS393NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS390DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS390NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LS393DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS393NSR	SO	NS	14	2000	346.0	346.0	33.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

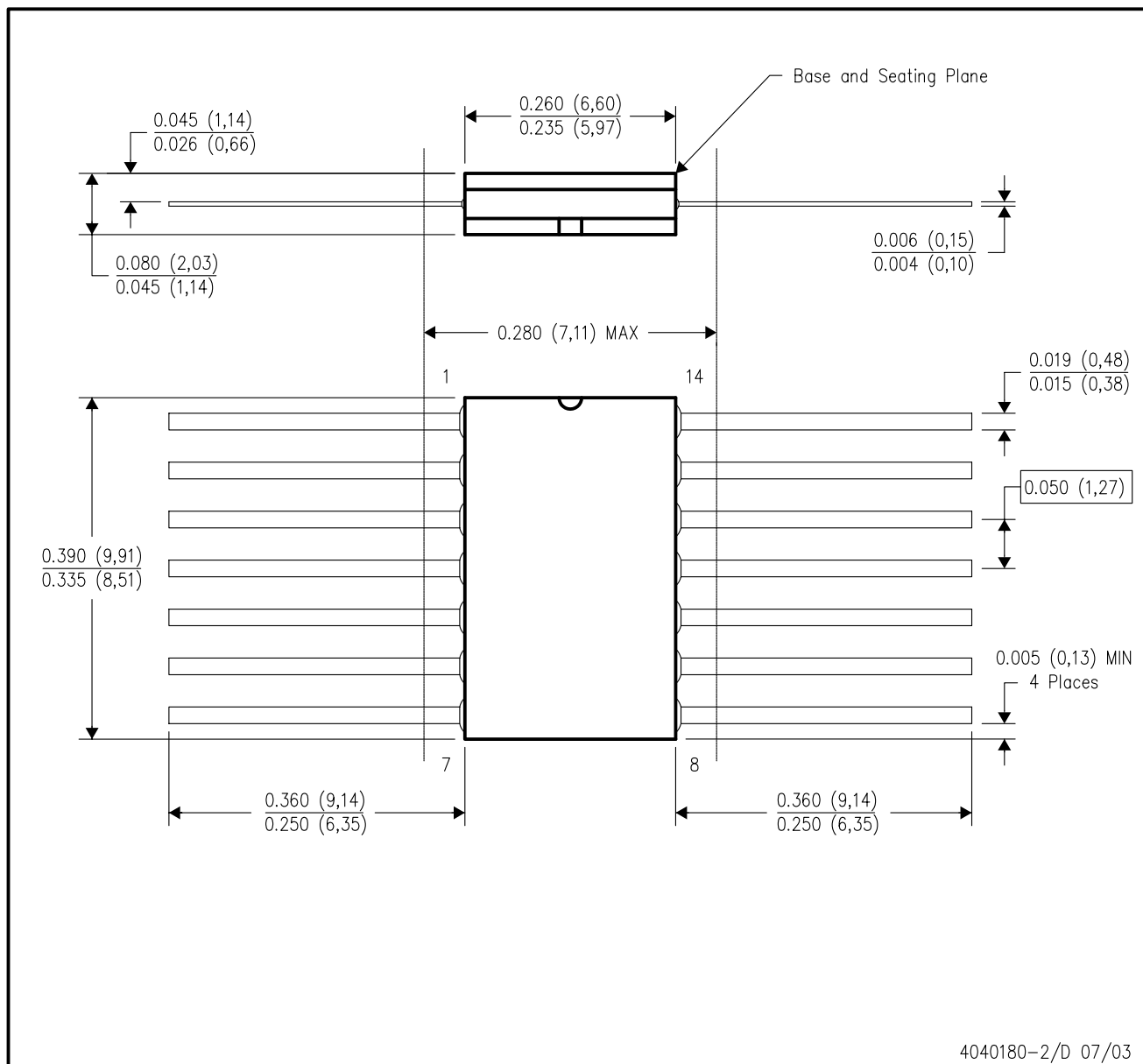


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

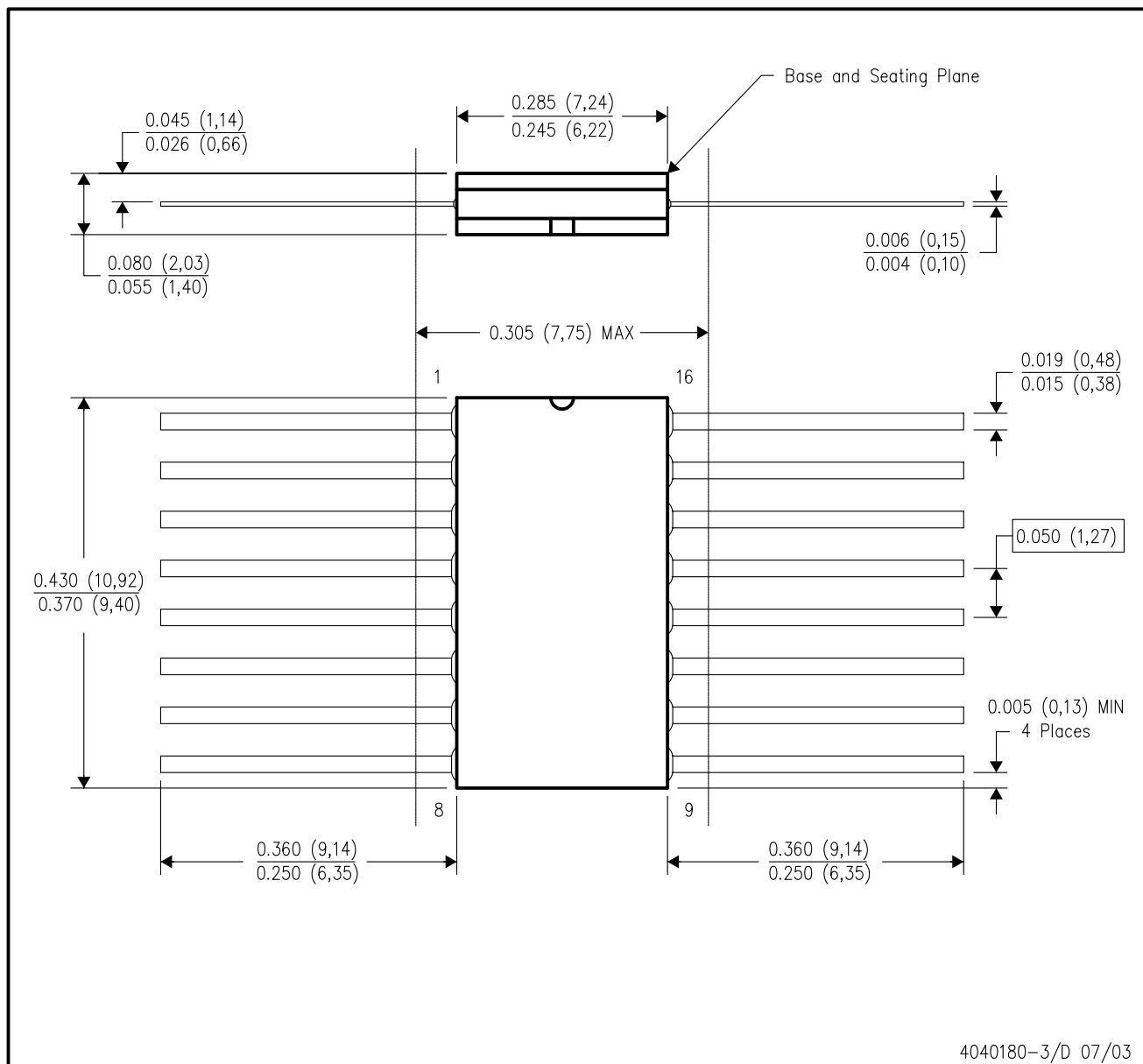
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

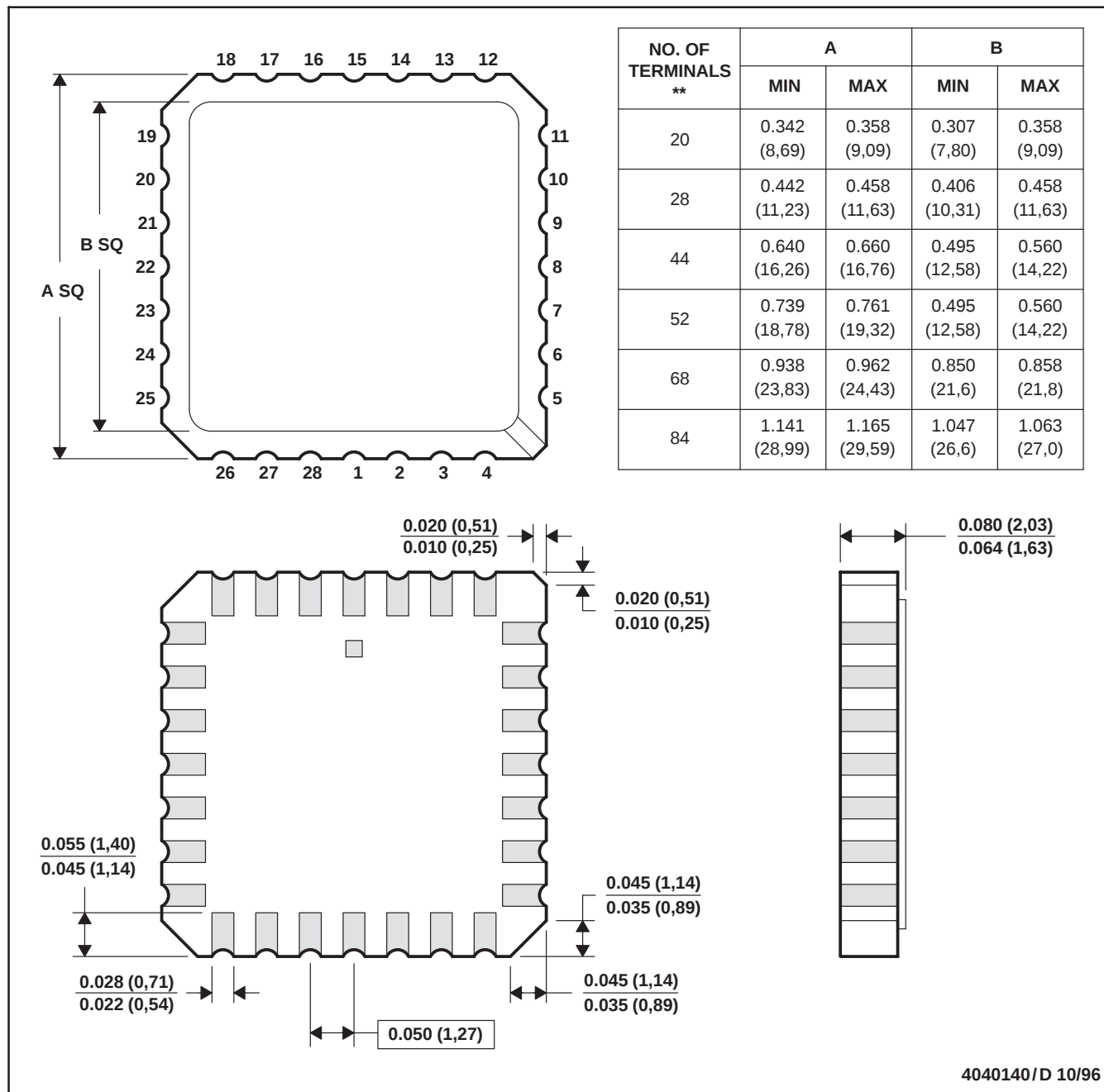


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



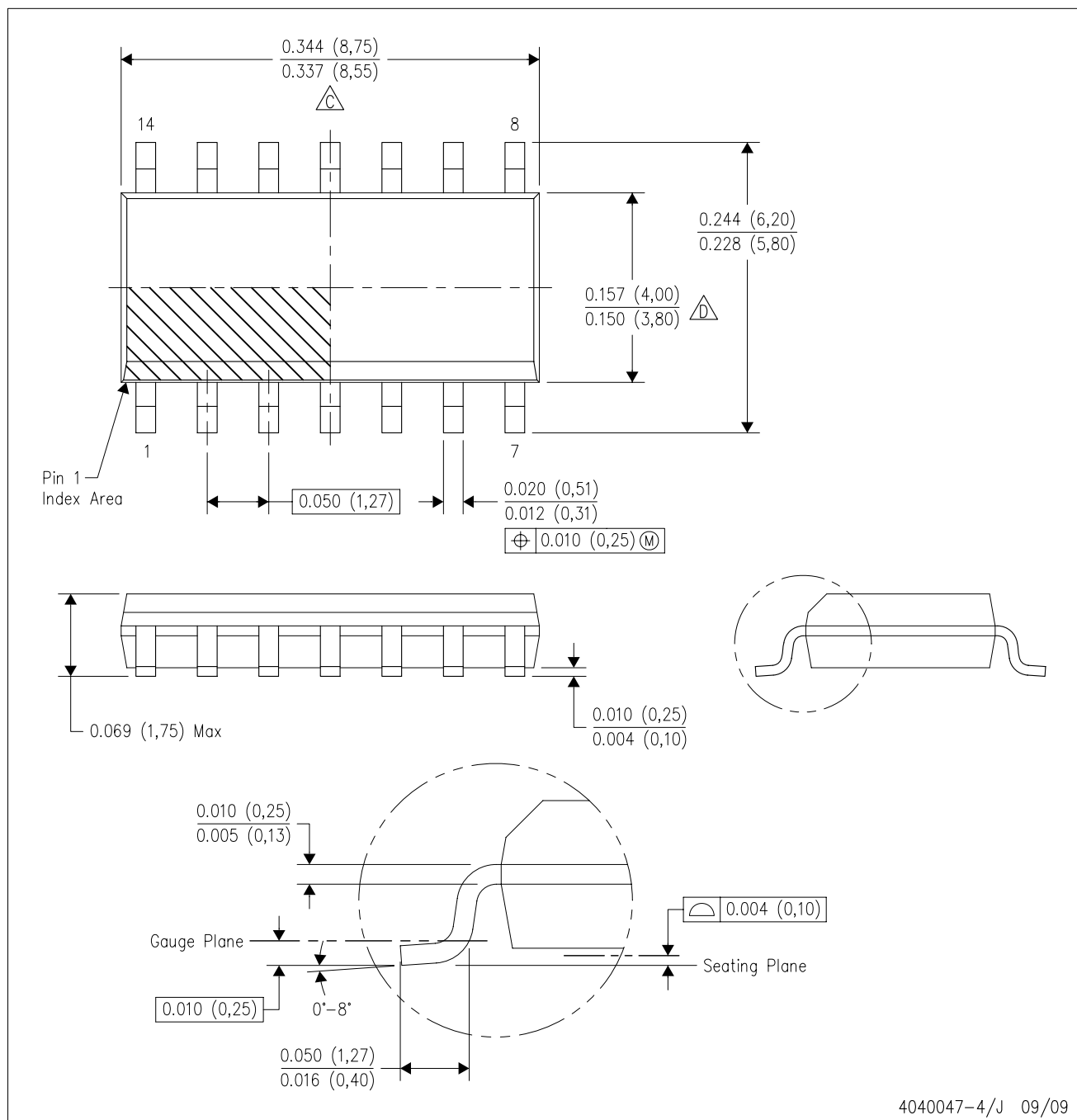
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

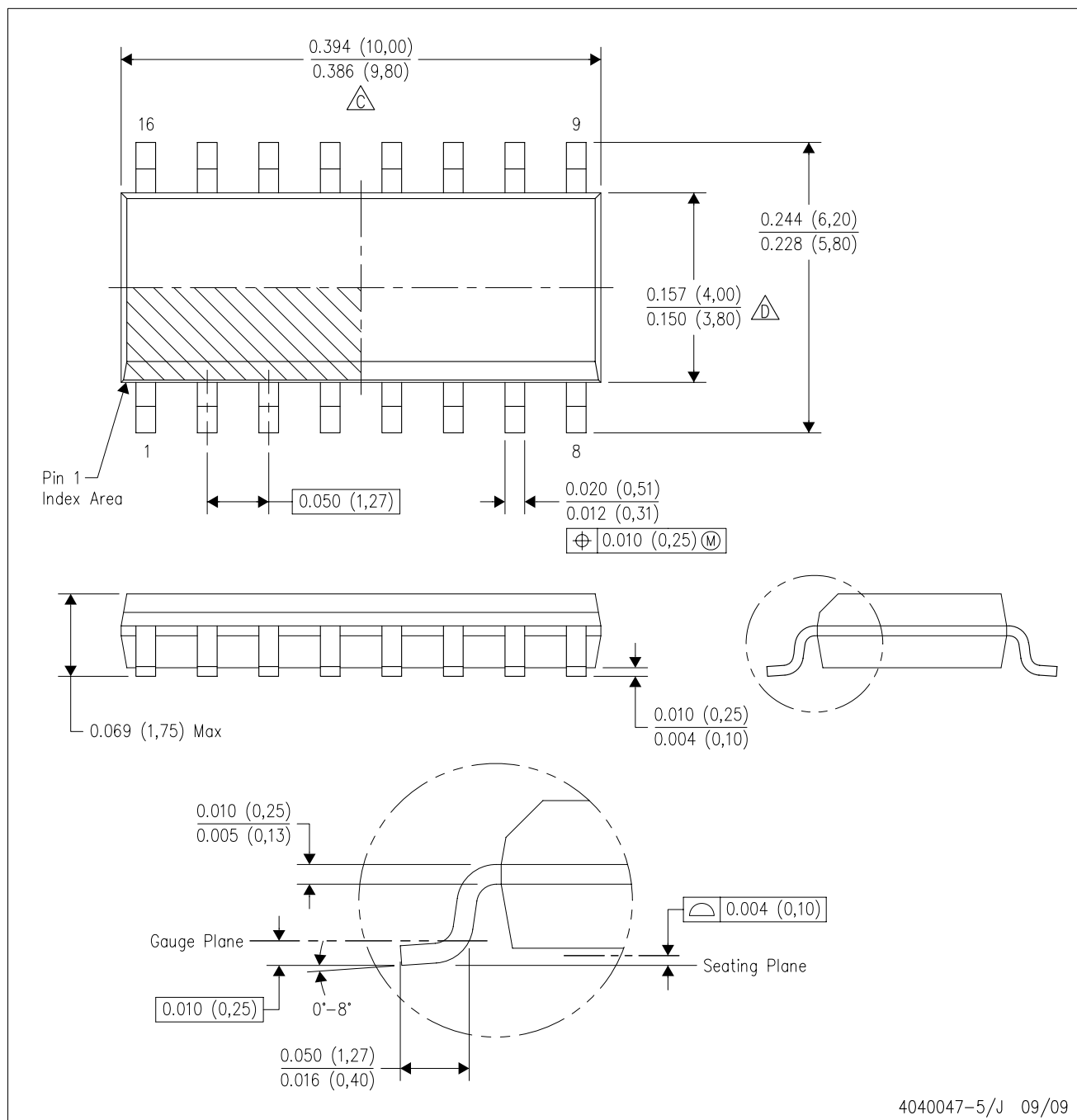


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

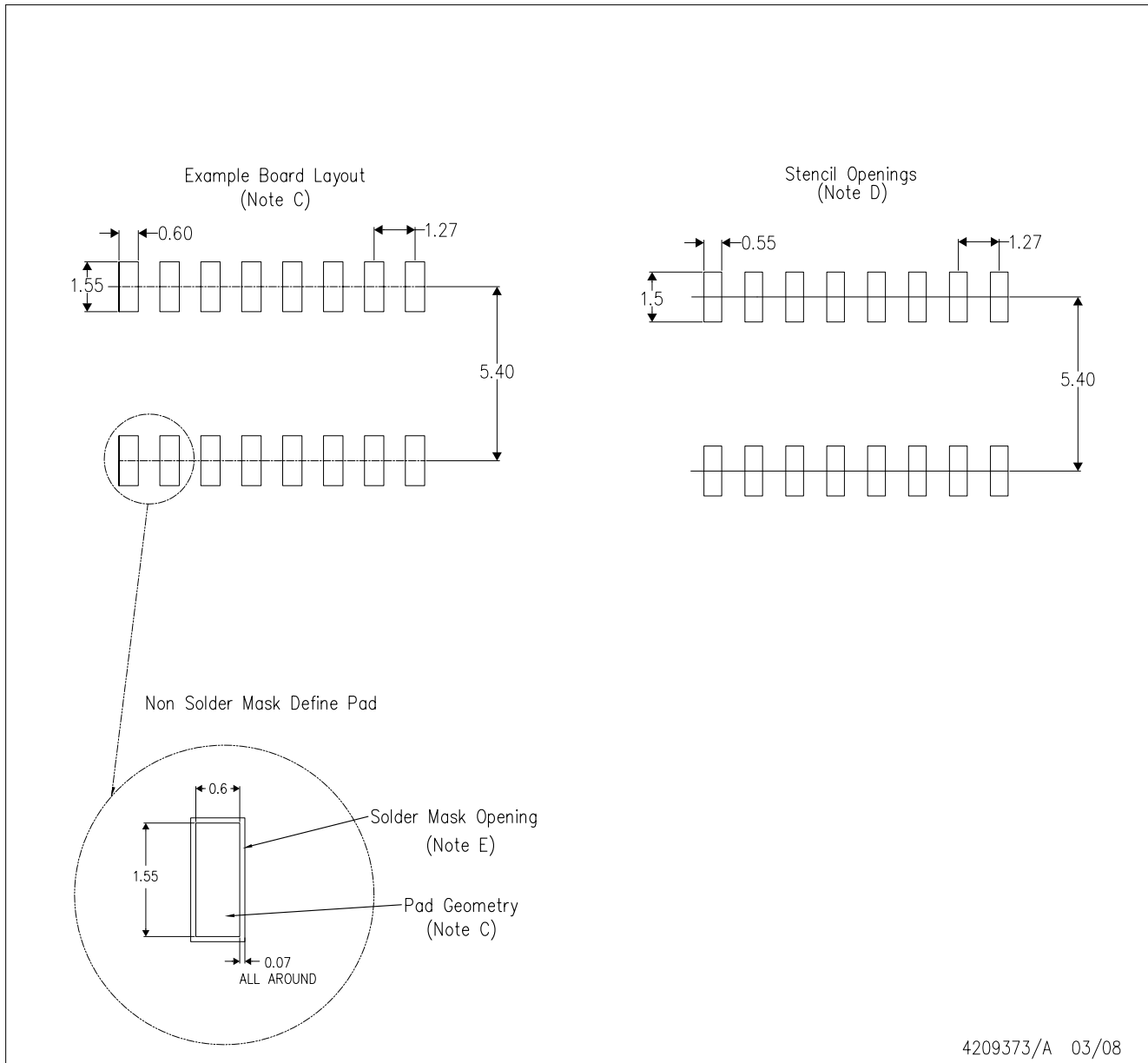
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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