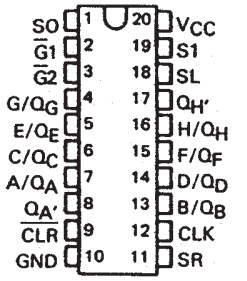
SDLS156 – MARCH 1974 – REVISED MARCH 1988

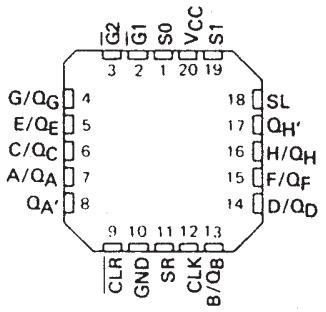
- **Multiplexed Inputs/Outputs Provide Improved Bit Density**
- **Four Modes of Operations:**
  Hold (Store) Shift Left
  Shift Right Load Data
- **Operates with Outputs Enabled or at High Z**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear**
- **Applications:**
  Stacked or Push-Down Registers
  Buffer Storage, and Accumulator Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS299, SN54S299 . . . FK PACKAGE
(TOP VIEW)



description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

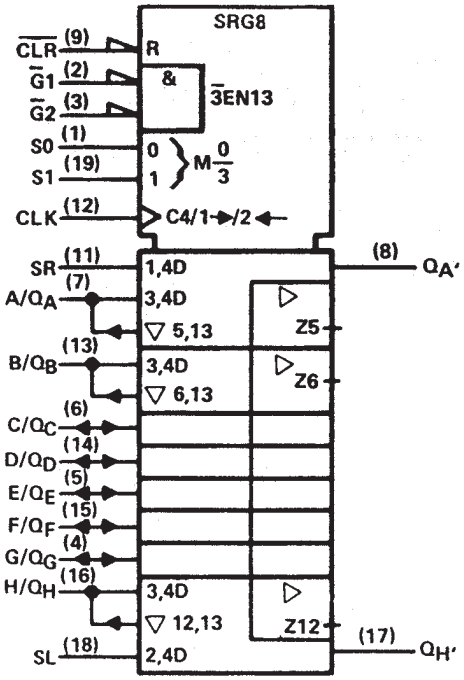
FUNCTION TABLE

MODE	INPUTS							INPUTS/OUTPUTS								OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR									
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

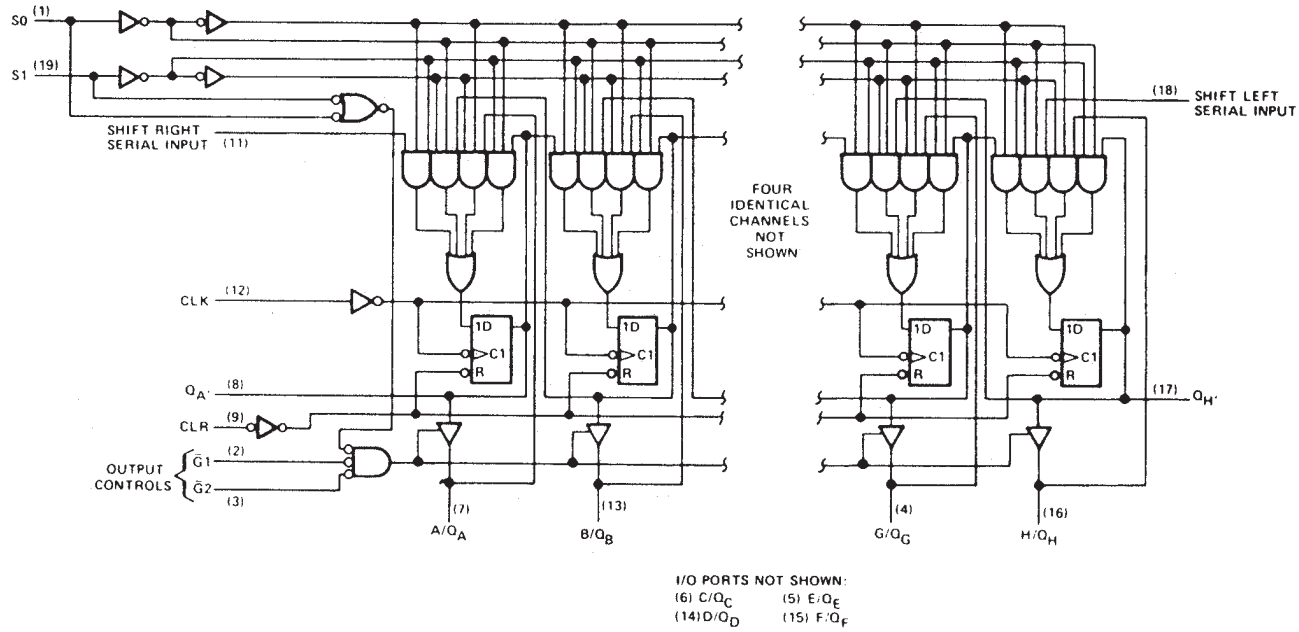
a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.2		V
		$Q_{A'}$ or $Q_{H'}$		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−250	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX, V_I = 2.7 V			100	μA
		Any other				50	
I_{IL}	Low-level input current	CLK or $\overline{CLR}$	V_{CC} = MAX, V_I = 0.5 V			−2	mA
		S0, S1				−500	μA
		Any other				−250	μA
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX	−40		−100	mA
		$Q_{A'}$ or $Q_{H'}$		−20		−100	
I_{CC}	Supply current		V_{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	50	70		MHz
t_{PLH}	CLK	$Q_{A'}$ or $Q_{H'}$	R_L = 1 kΩ, C_L = 15 pF		12	20	ns
t_{PHL}					13	20	
t_{PHL}	$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$			14	21	ns
t_{PLH}	CLK	Q_A thru Q_H	R_L = 280 Ω, C_L = 45 pF		15	21	ns
t_{PHL}					15	21	
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H			16	24	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			10	18	ns
t_{PZL}					12	18	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	R_L = 280 Ω, C_L = 5 pF		7	12	ns
t_{PLZ}					7	12	

¶ f_{max} = maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.
Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
78024012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
7802401RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
7802401RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
7802401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
7802401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS299J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54S299J	LIFEBUY	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54S299J	LIFEBUY	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74LS299DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DWE4	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DWE4	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DWRE4	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299DWRE4	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74S299N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S299N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS299J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS299W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC