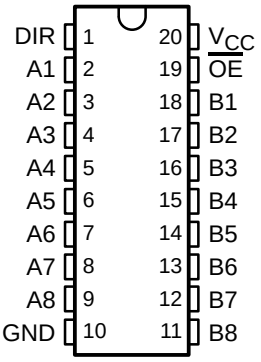
- **3-State Outputs Drive Bus Lines Directly**
- **PNP Inputs Reduce dc Loading on Bus Lines**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Typical Propagation Delay Times Port to Port, 8 ns**

| TYPE | $I_{OL}$ (SINK CURRENT) | $I_{OH}$ (SOURCE CURRENT) |
|---|---|---|
| SN54LS245 | 12 mA | –12 mA |
| SN74LS245 | 24 mA | –15 mA |

**SN54LS245 . . . J OR W PACKAGE**
**SN74LS245 . . . DB, DW, N, OR NS PACKAGE**
**(TOP VIEW)**

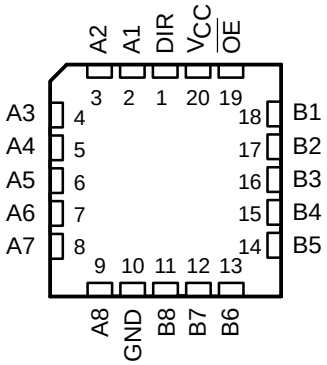



## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can disable the device so that the buses are effectively isolated.

**SN54LS245 . . . FK PACKAGE**
**(TOP VIEW)**




**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP – N | Tube | SN74LS245N | SN74LS245N |
| | SOIC – DW | Tube | SN74LS245DW | LS245 |
| | | Tape and reel | SN74LS245DWR | |
| | SOP – NS | Tape and reel | SN74LS245NSR | 74LS245 |
| | SSOP – DB | Tape and reel | SN74LS245DBR | LS245 |
| –55°C to 125°C | CDIP – J | Tube | SN54LS245J | SN54LS245J |
| | | Tube | SNJ54LS245J | SNJ54LS245J |
| | CFP – W | Tube | SNJ54LS245W | SNJ54LS245W |
| | LCCC – FK | Tube | SN54LS245FK | SN54LS245FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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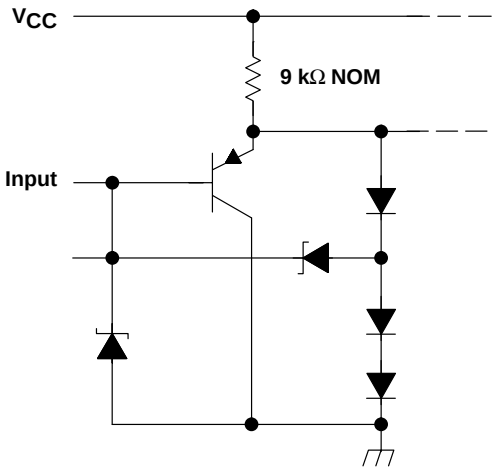
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**FUNCTION TABLE**

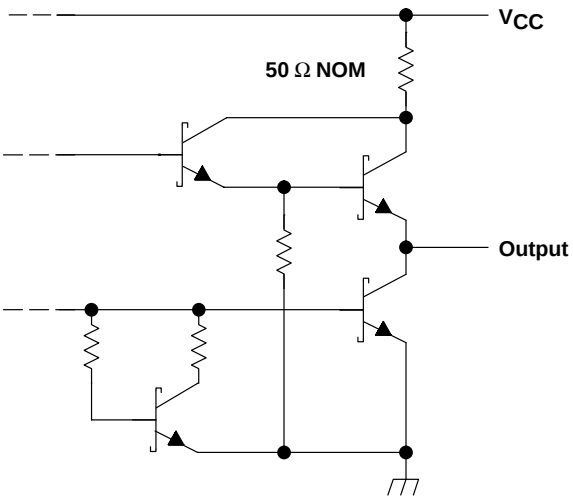
| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## schematics of inputs and outputs

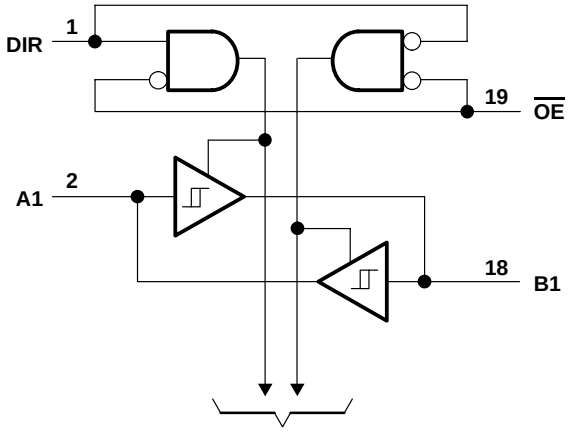
**EQUIVALENT OF EACH INPUT**




**TYPICAL OF ALL OUTPUTS**




## logic diagram (positive logic)




To Seven Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ (see Note 1) . . . . . 7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

| | | SN54LS245 | | | SN74LS245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | | | –12 | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

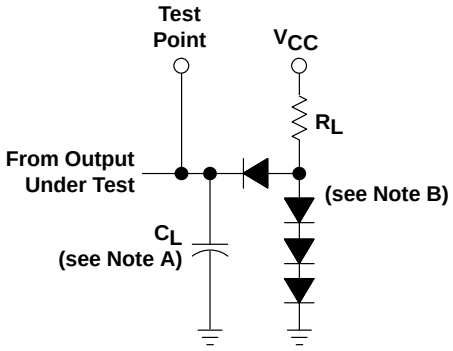
| PARAMETER | | | TEST CONDITIONS† | | SN54LS245 | | | SN74LS245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = –18 mA | | | –1.5 | | | –1.5 | V |
| | Hysteresis ($V_{T+} – V_{T–}$) | A or B | $V_{CC}$ = MIN | | 0.2 | 0.4 | | 0.2 | 0.4 | | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL(max)}$ | $I_{OH}$ = –3 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | $I_{OH}$ = MAX | 2 | | | 2 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL(max)}$ | $I_{OL}$ = 12 mA | | | 0.4 | | | 0.4 | V |
| | | | | $I_{OL}$ = 24 mA | | | | | | 0.5 | |
| $I_{OZH}$ | Off-state output current, high-level voltage applied | | $V_{CC}$ = MAX, $\overline{OE}$ at 2 V | $V_O$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | | $V_{CC}$ = MAX, $\overline{OE}$ at 2 V | $V_O$ = 0.4 V | | | –200 | | | –200 | µA |
| $I_I$ | Input current at maximum input voltage | A or B | $V_{CC}$ = MAX | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| | | DIR or $\overline{OE}$ | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, | $V_{IH}$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = MAX, | $V_{IL}$ = 0.4 V | | | –0.2 | | | –0.2 | mA |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | –40 | | –225 | 40 | | –225 | mA |
| $I_{CC}$ | Supply current | Total, outputs high | $V_{CC}$ = MAX | Outputs open | | 48 | 70 | | 48 | 70 | mA |
| | | Total, outputs low | | | | 62 | 90 | | 62 | 90 | |
| | | Outputs at high Z | | | | 64 | 95 | | 64 | 95 | |

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

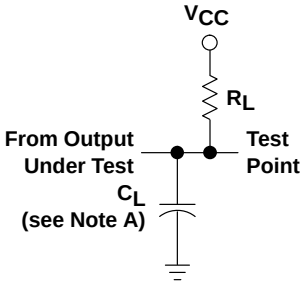
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 45 pF, | $R_L$ = 667 Ω | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 8 | 12 | |
| $t_{PZL}$ | Output enable time to low level | $C_L$ = 45 pF, | $R_L$ = 667 Ω | | 27 | 40 | ns |
| $t_{PZH}$ | Output enable time to high level | | | | 25 | 40 | |
| $t_{PLZ}$ | Output disable time from low level | $C_L$ = 5 pF, | $R_L$ = 667 Ω | | 15 | 25 | ns |
| $t_{PHZ}$ | Output disable time from high level | | | | 15 | 28 | |

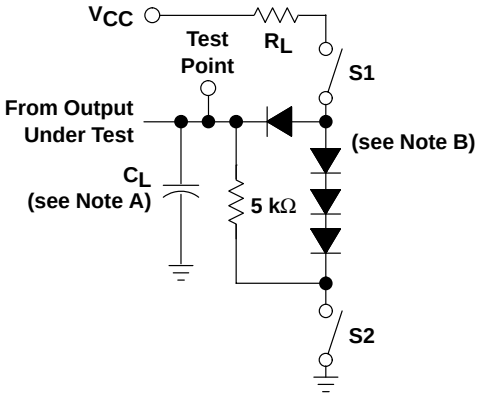
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54LS/74LS DEVICES



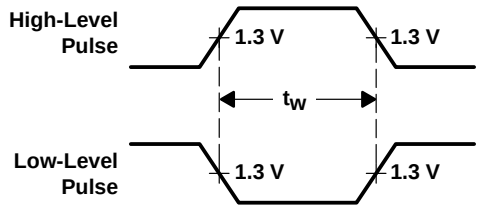

LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



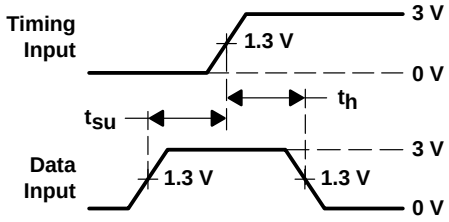

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



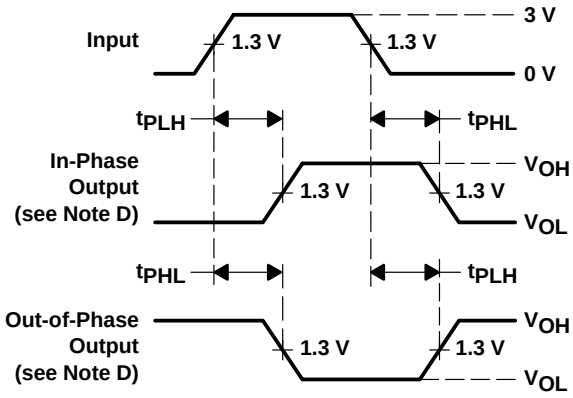

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



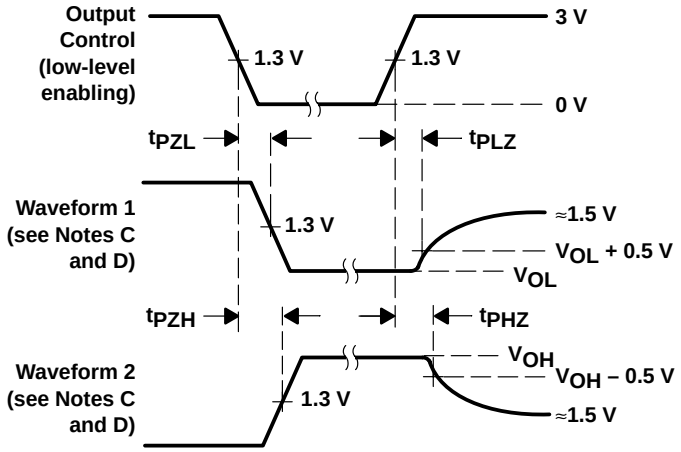

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for $t_{PLH}$, $t_{PHL}$, $t_{PHZ}$, and $t_{PLZ}$; S1 is open and S2 is closed for $t_{PZH}$; S1 is closed and S2 is open for $t_{PZL}$.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8002101VSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8002101VS A SNV54LS245W | Samples |
| 80021012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 80021012A SNJ54LS 245FK | Samples |
| 8002101SA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8002101SA SNJ54LS245W | Samples |
| JM38510/32803B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32803B2A | Samples |
| JM38510/32803BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BRA | Samples |
| JM38510/32803BSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BSA | Samples |
| M38510/32803B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32803B2A | Samples |
| M38510/32803BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BRA | Samples |
| M38510/32803BSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 32803BSA | Samples |
| SN54LS245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS245J | Samples |
| SN74LS245DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS245 | Samples |
| SN74LS245J | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS245N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS245N | Samples |
| SN74LS245N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS245NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS245N | Samples |
| SN74LS245NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS245 | Samples |
| SN74LS245NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS245 | Samples |
| SNJ54LS245FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 80021012A SNJ54LS 245FK | Samples |
| SNJ54LS245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS245J | Samples |
| SNJ54LS245W | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8002101SA SNJ54LS245W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS245, SN54LS245-SP, SN74LS245 :**

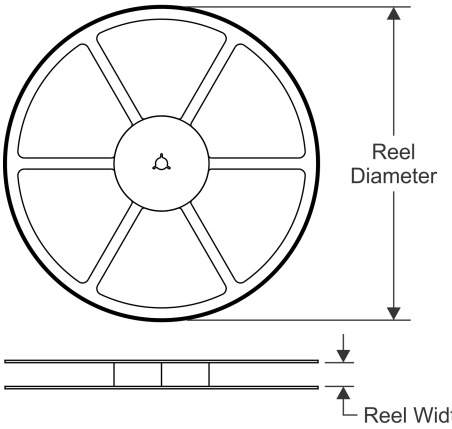
- Catalog: SN74LS245, SN54LS245
- Military: SN54LS245
- Space: SN54LS245-SP

NOTE: Qualified Version Definitions:

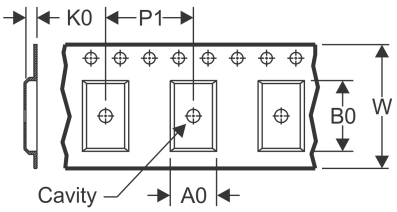
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

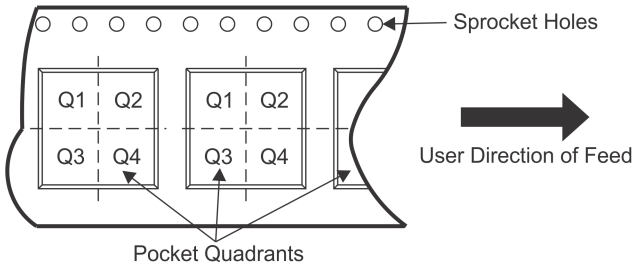



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

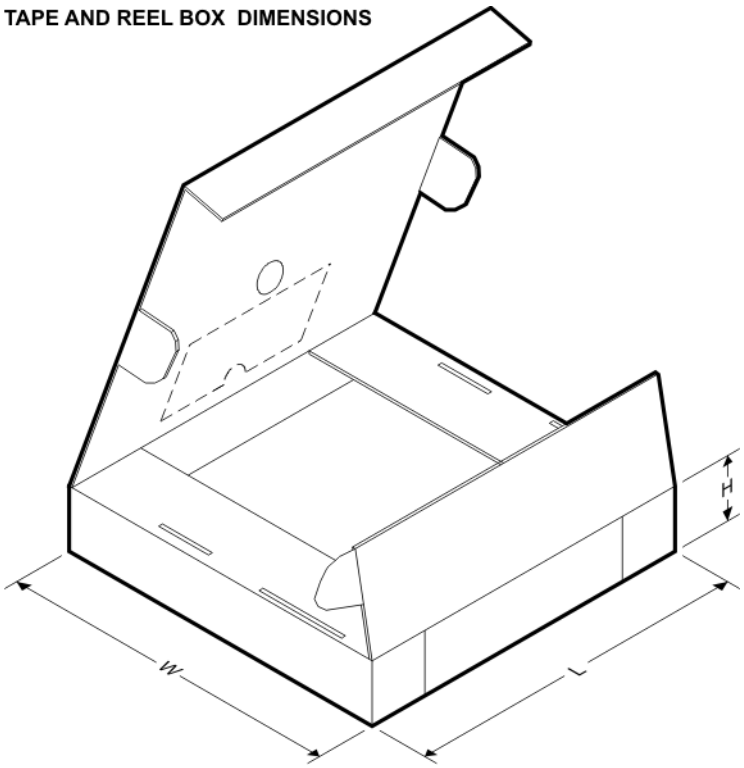
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS245NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



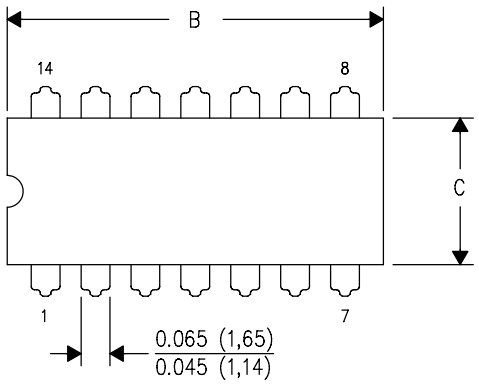

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS245DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LS245DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS245NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

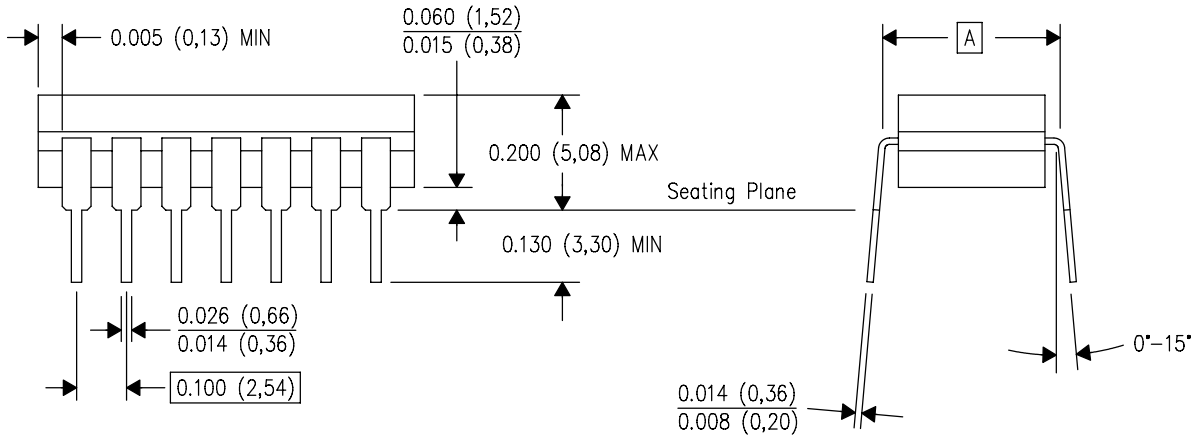
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



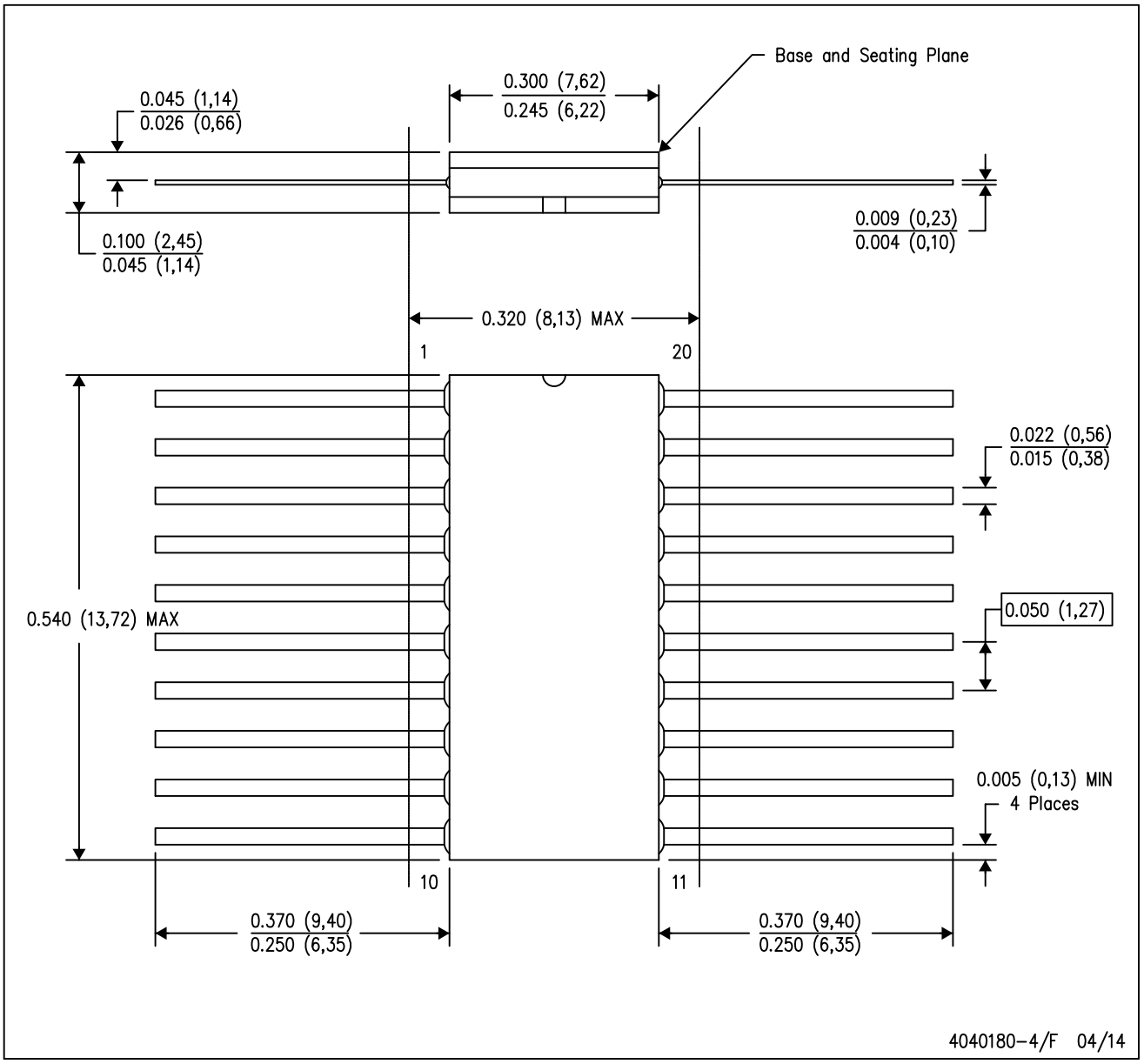

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

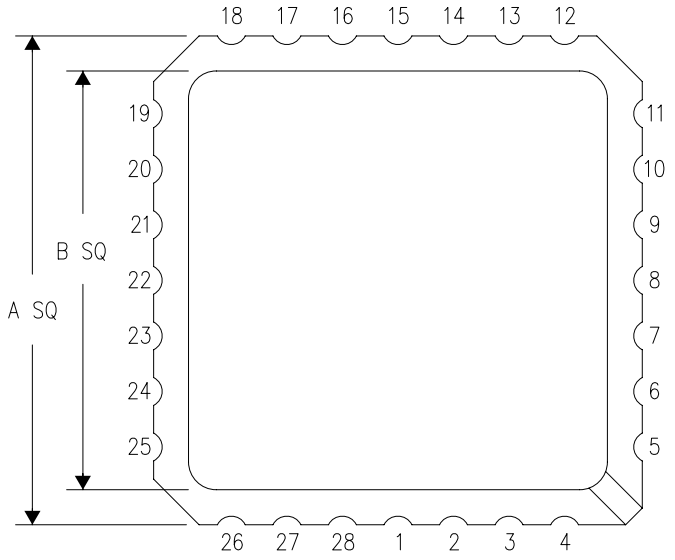
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



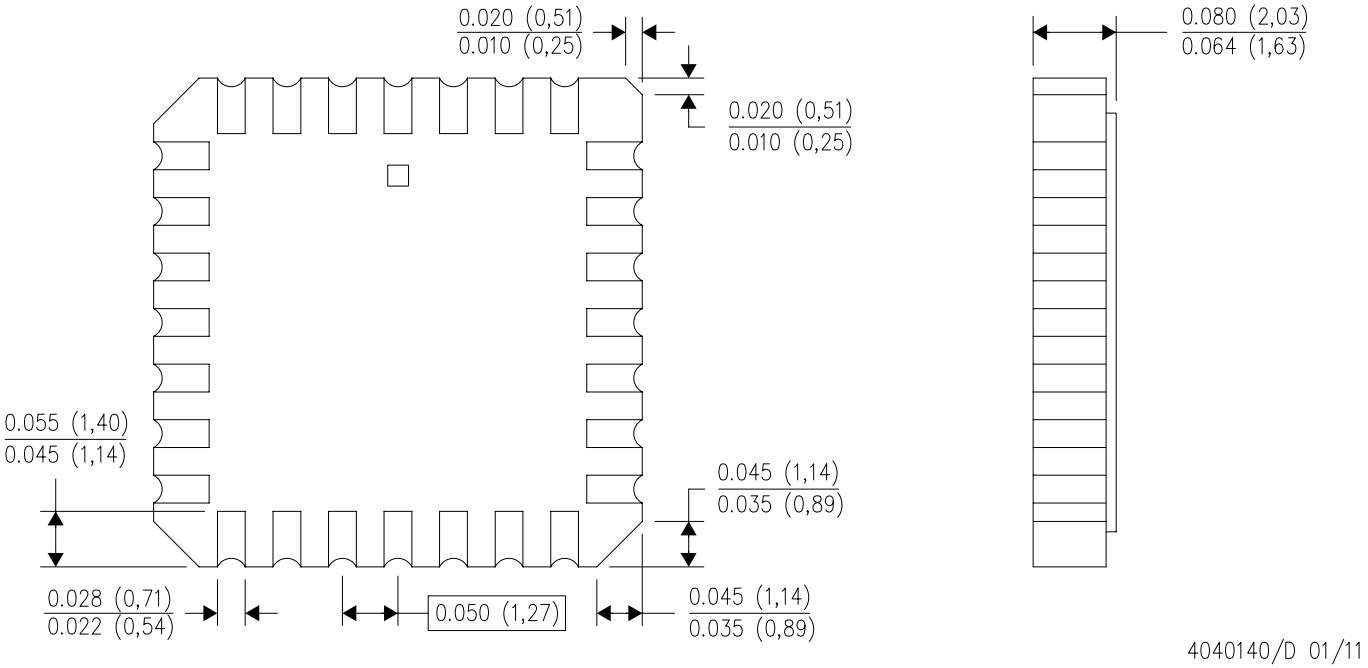

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



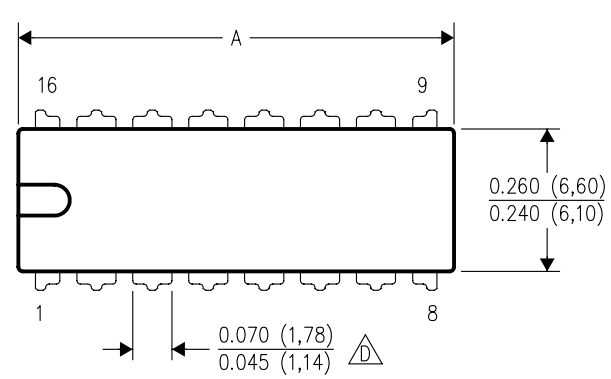

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

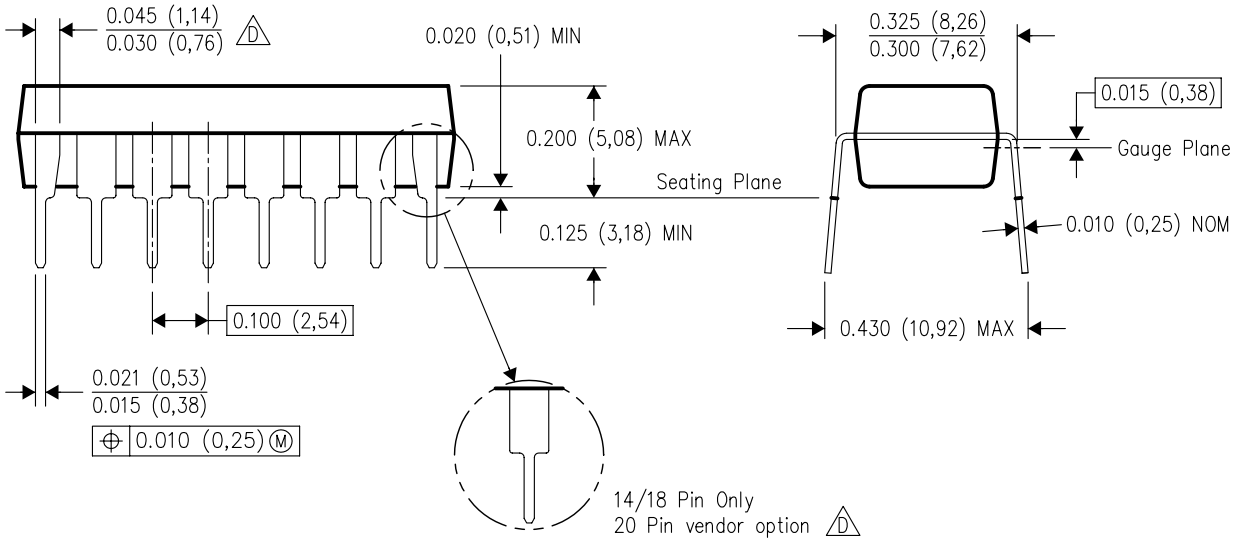
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



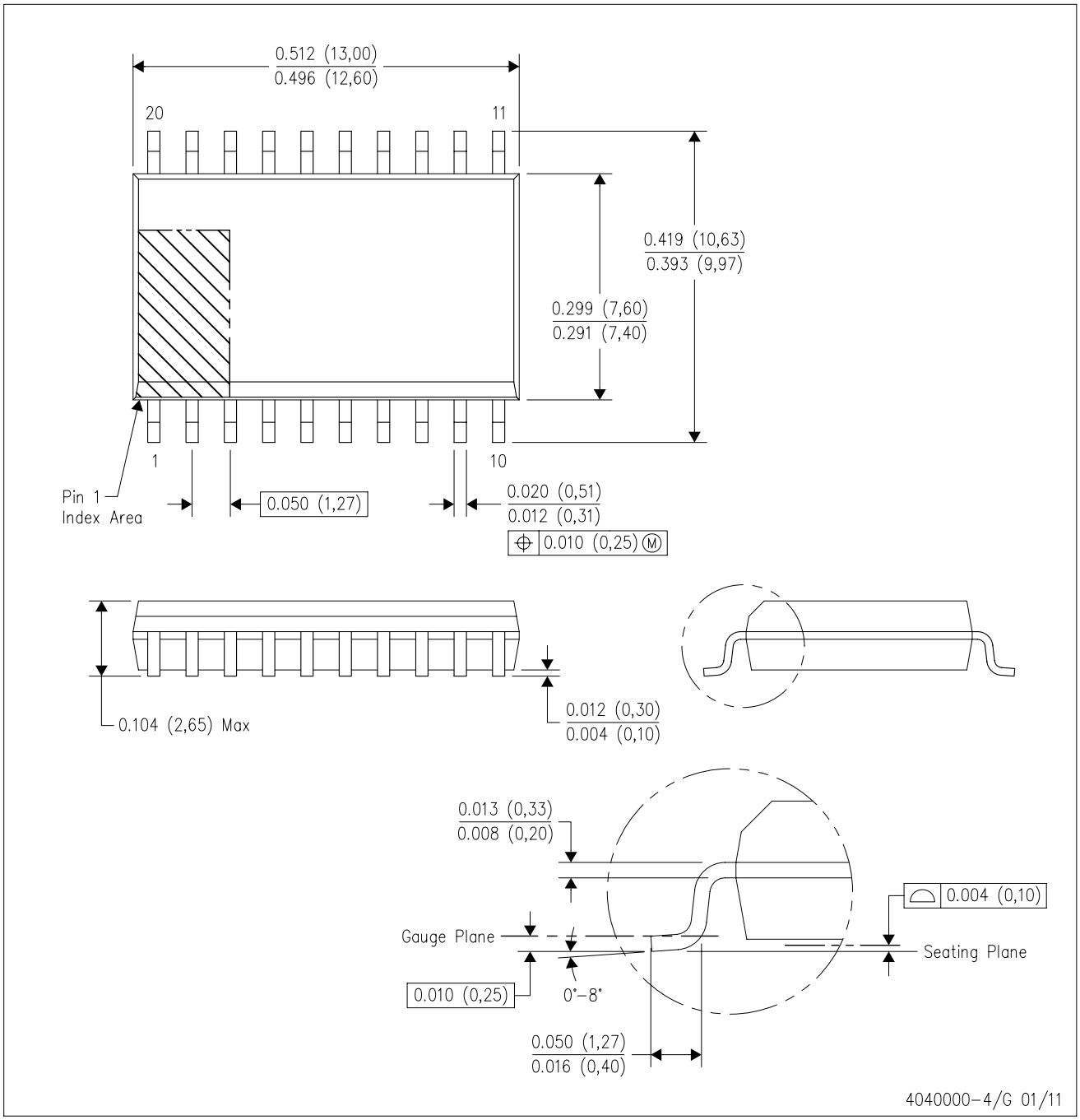

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

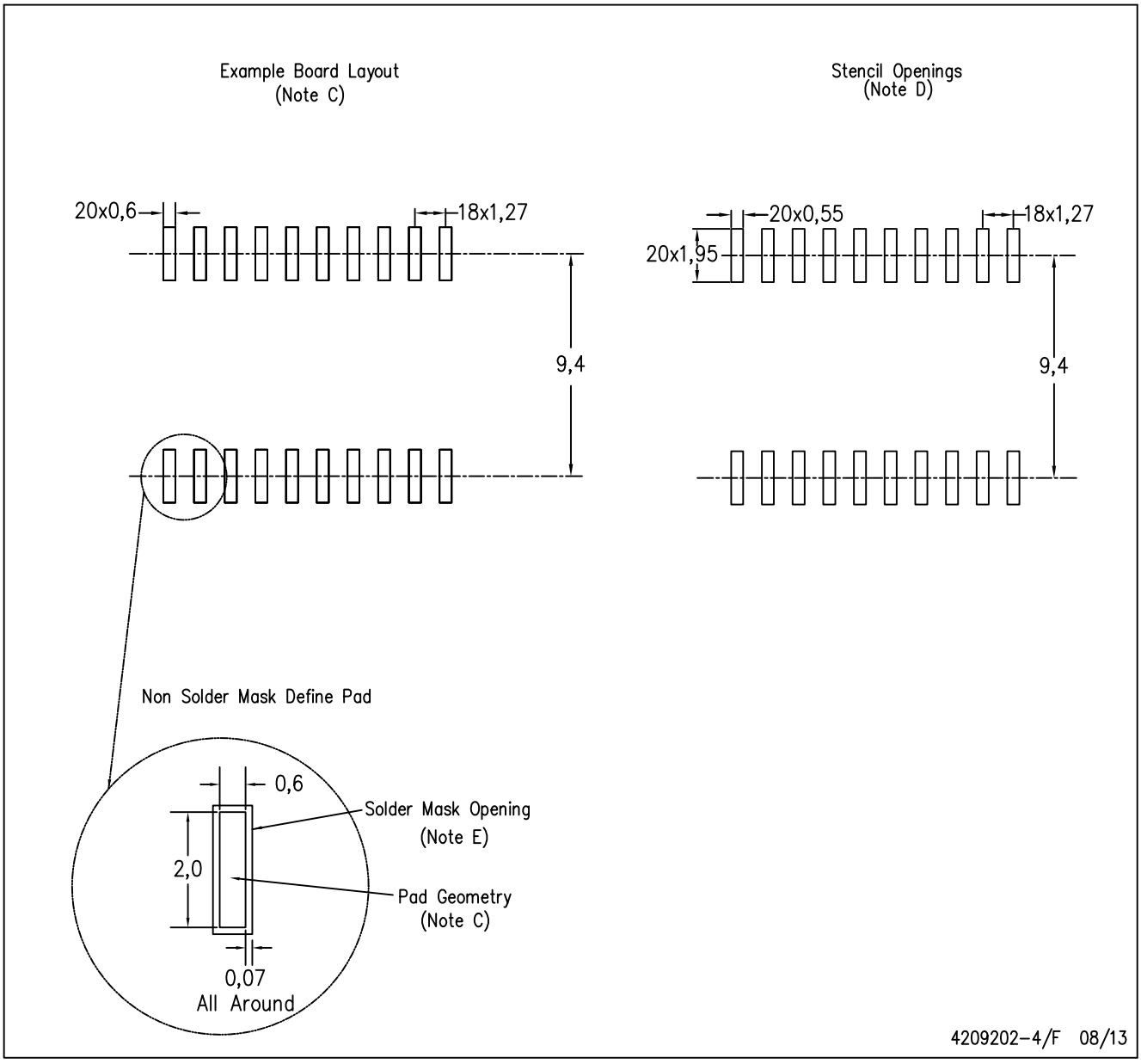
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE

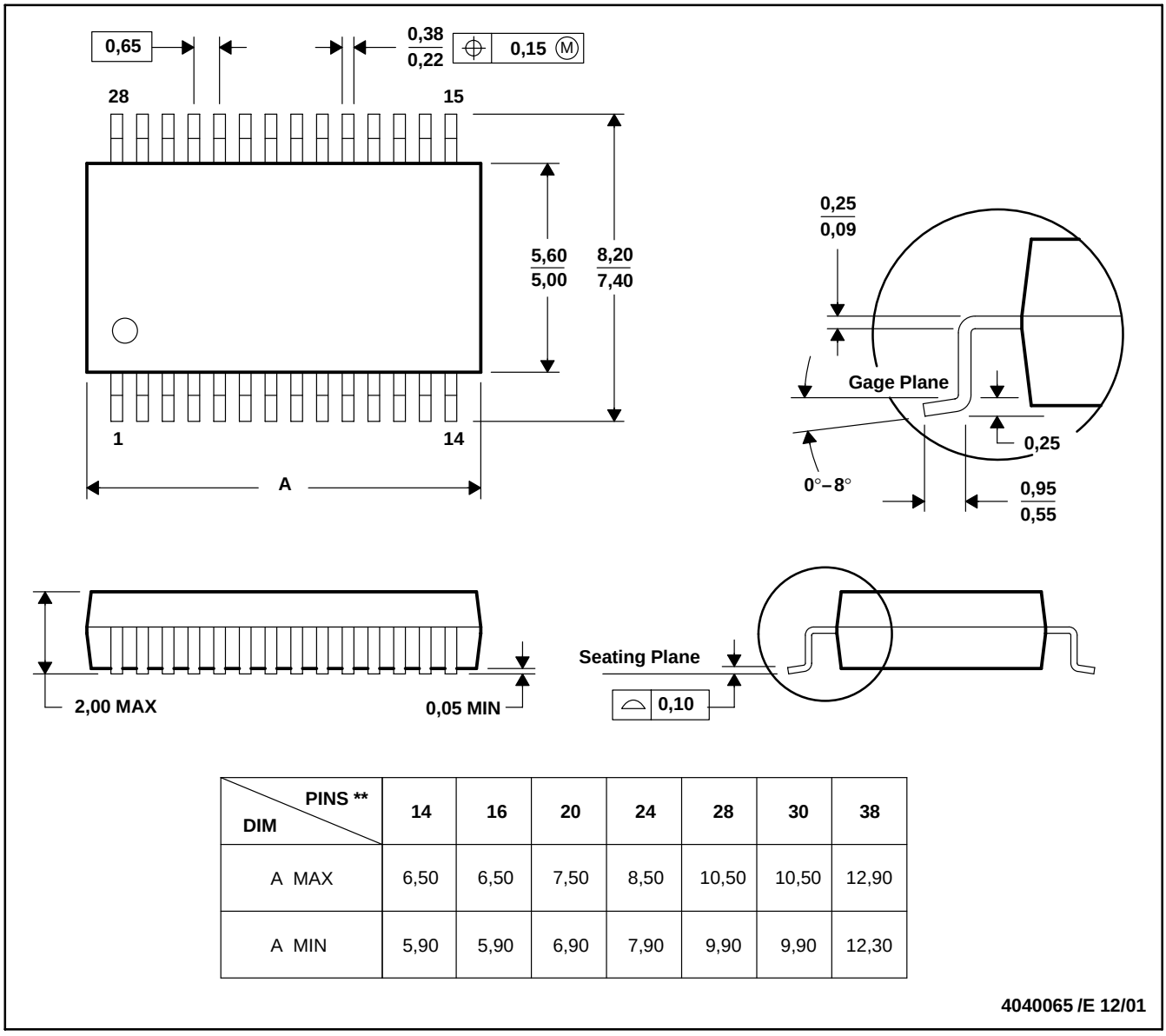



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

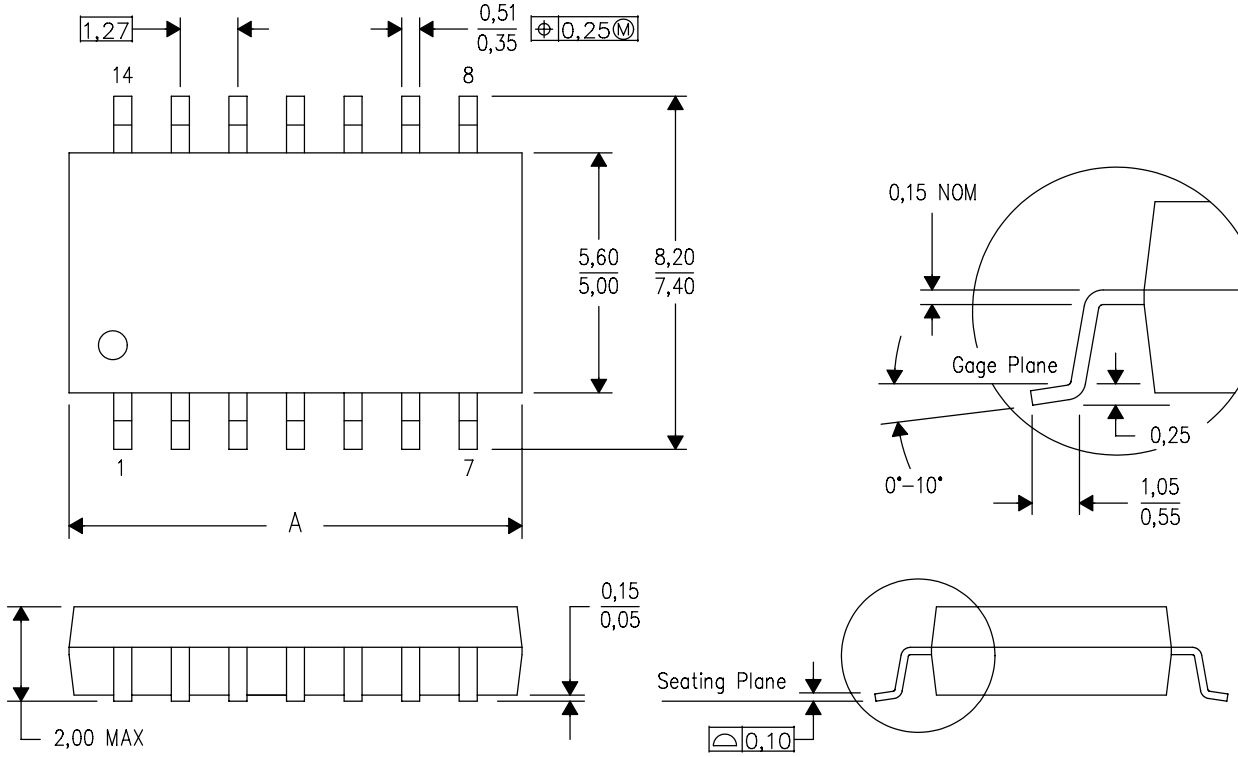
**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

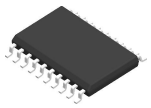
**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

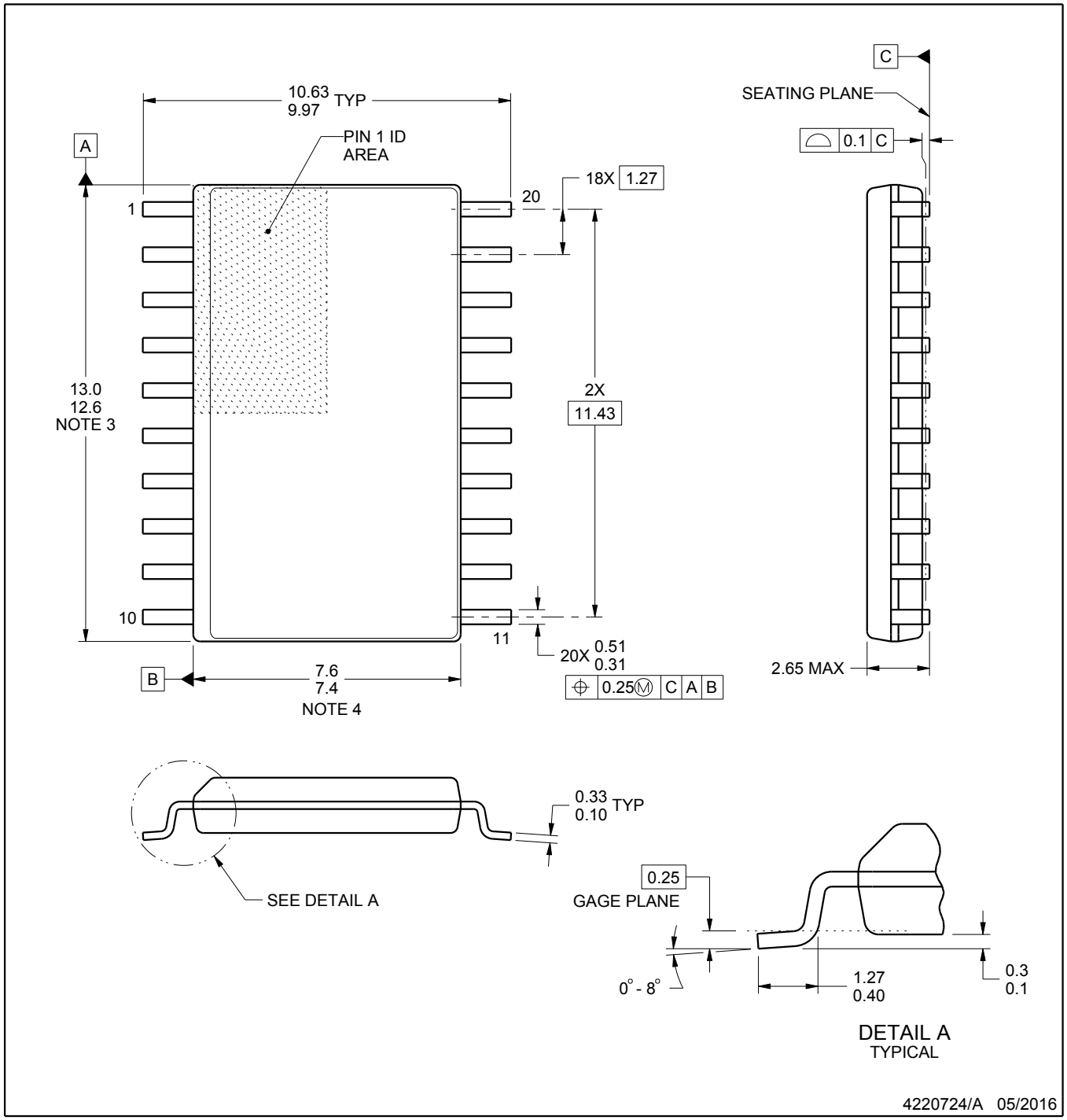


# PACKAGE OUTLINE

## DW0020A

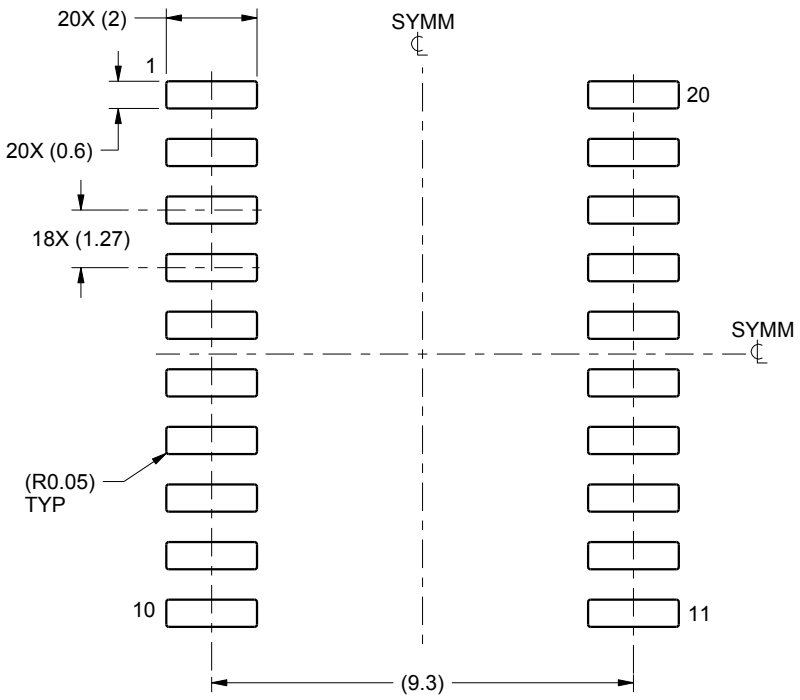
## SOIC - 2.65 mm max height

SOIC

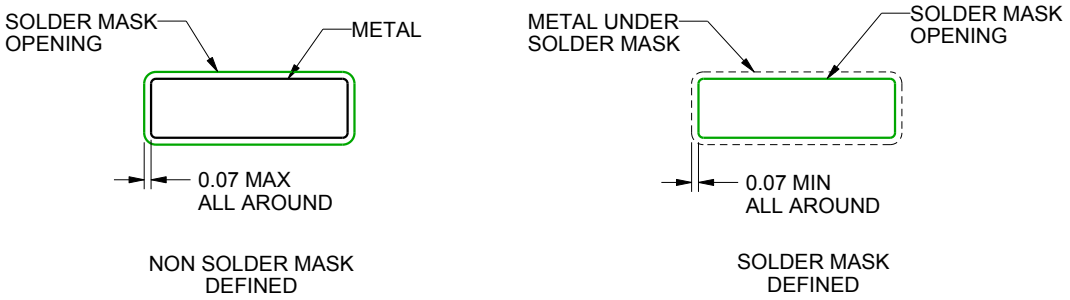



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

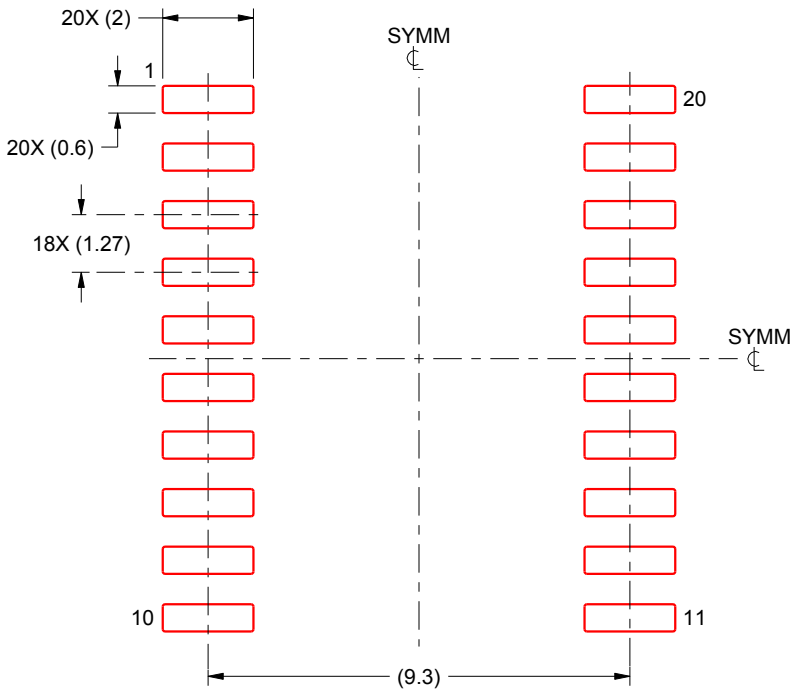



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



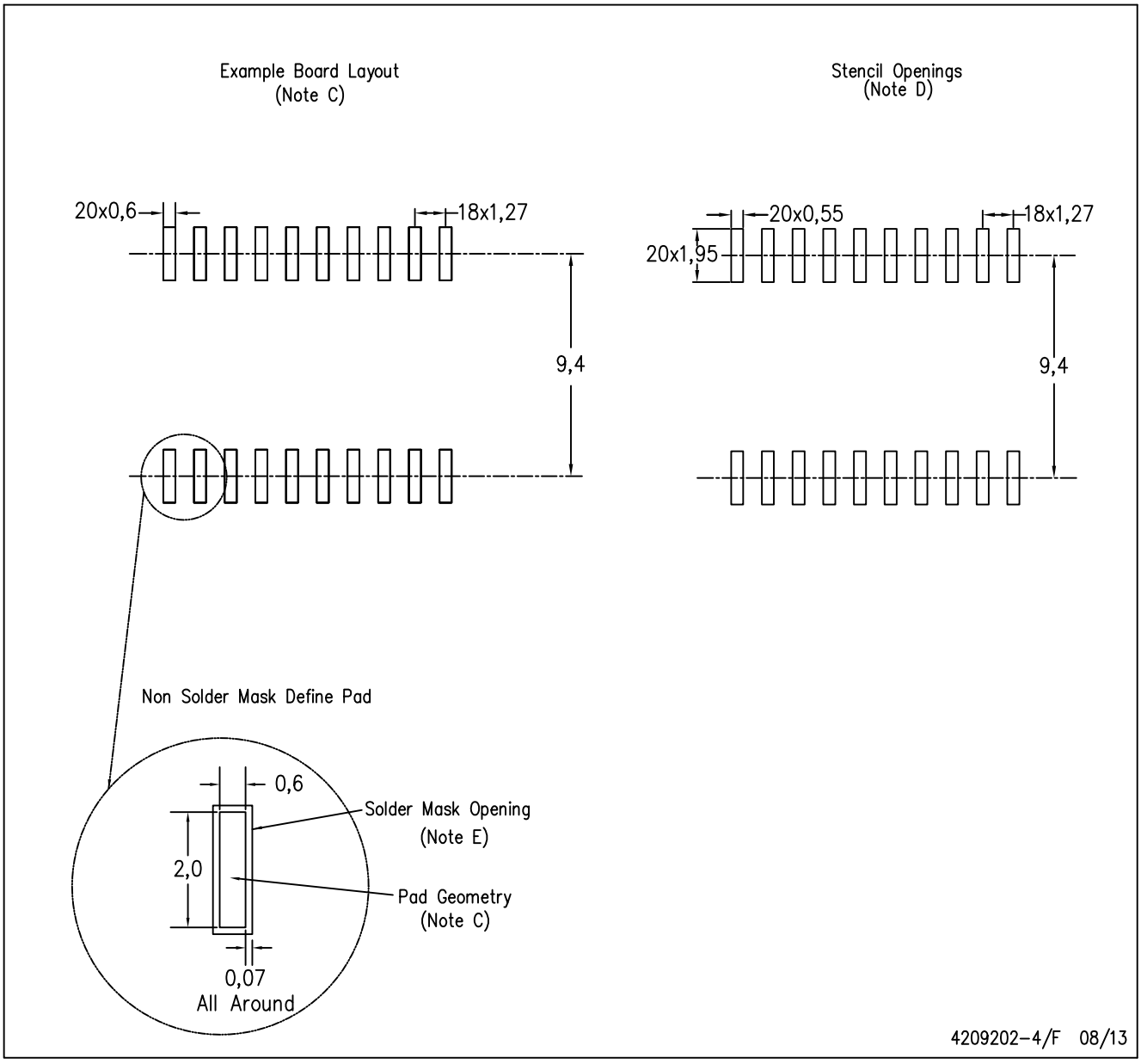

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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