

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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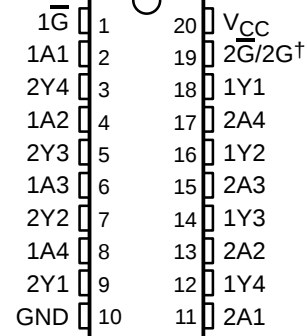
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control ($\overline{G}$) inputs, and complementary output-control (G and $\overline{G}$) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω .

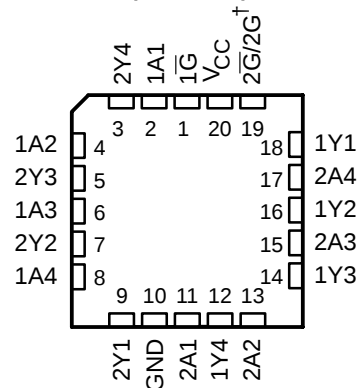
SN54LS', SN54S' . . . J OR W PACKAGE
SN74LS240, SN74LS244 . . . DB, DW, N, OR NS PACKAGE
SN74LS241 . . . DW, N, OR NS PACKAGE
SN74S' . . . DW OR N PACKAGE

(TOP VIEW)



† 2G for 'LS241 and 'S241 or $\overline{2G}$ for all other drivers.

SN54LS', SN54S' . . . FK PACKAGE
(TOP VIEW)



† 2G for 'LS241 and 'S241 or $\overline{2G}$ for all other drivers.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS240N	SN74LS240N
			SN74LS241N	SN74LS241N
			SN74LS244N	SN74LS244N
			SN74S240N	SN74S240N
			SN74S241N	SN74S241N
			SN74S244N	SN74S244N
	SOIC – DW	Tube	SN74LS240DW	LS240
		Tape and reel	SN74LS240DWR	
		Tube	SN74LS241DW	LS241
		Tape and reel	SN74LS241DWR	
		Tube	SN74LS244DW	LS244
		Tape and reel	SN74LS244DWR	
		Tube	SN74S240DW	S240
		Tape and reel	SN74S240DWR	
		Tube	SN74S241DW	S241
		Tape and reel	SN74S241DWR	
		Tube	SN74S244DW	S244
		Tape and reel	SN74S244DWR	
	SOP – NS	Tube	SN74LS240NSR	74LS240
			SN74LS241NSR	74LS241
			SN74LS244NSR	74LS244
	SSOP – DB	Tape and reel	SN74LS240DBR	LS240
			SN74LS244DBR	LS244

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
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ORDERING INFORMATION (CONTINUED)

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – J	Tube	SN54LS240J	SN54LS240J
			SNJ54LS240J	SNJ54LS240J
			SN54LS241J	SN54LS241J
			SNJ54LS241J	SNJ54LS241J
			SN54LS244J	SN54LS244J
			SNJ54LS244J	SNJ54LS244J
			SN54S240J	SN54S240J
			SNJ54S240J	SNJ54S240J
			SN54S241J	SN54S241J
			SNJ54S241J	SNJ54S241J
			SN54S244J	SN54S244J
			SNJ54S244J	SNJ54S244J
	CFP – W	Tube	SNJ54LS240W	SNJ54LS240W
			SNJ54LS241W	SNJ54LS241W
			SNJ54LS244W	SNJ54LS244W
			SNJ54S240W	SNJ54S240W
			SNJ54S241W	SNJ54S241W
			SNJ54S244W	SNJ54S244W
	LCCC – FK	Tube	SNJ54LS240FK	SNJ54LS240FK
			SNJ54LS241FK	SNJ54LS241FK
			SNJ54LS244FK	SNJ54LS244FK
			SNJ54S240FK	SNJ54S240FK
			SNJ54S241FK	SNJ54S241FK
			SNJ54S244FK	SNJ54S244FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

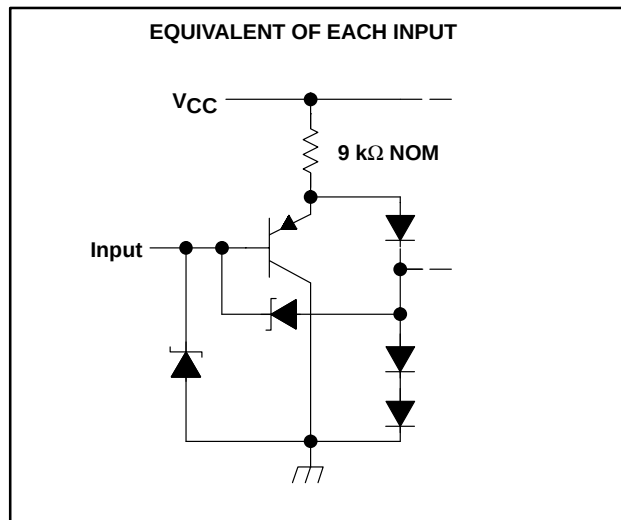


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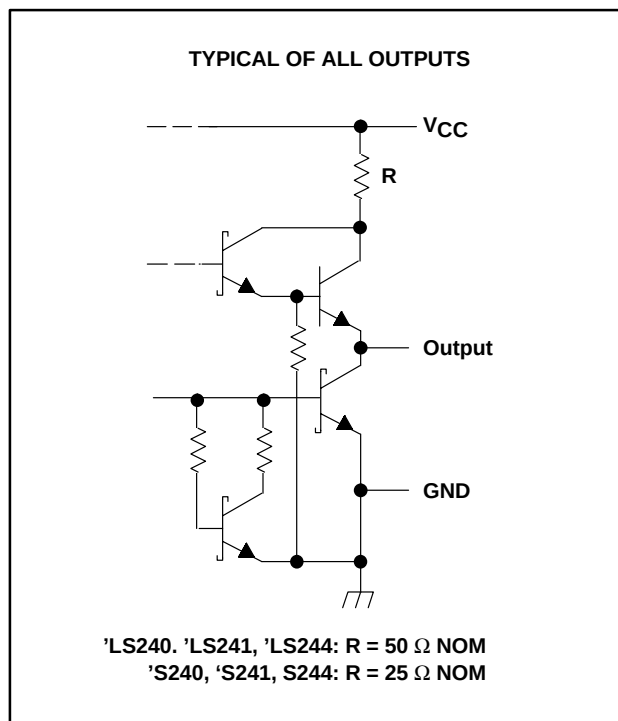
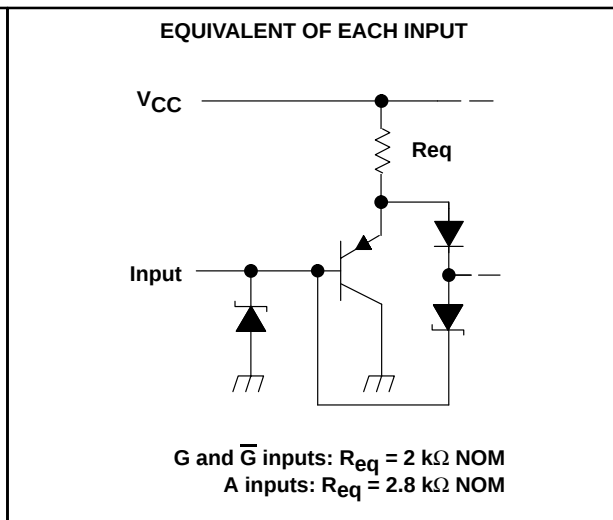
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schematics of inputs and outputs

'LS240, 'LS241, 'LS244



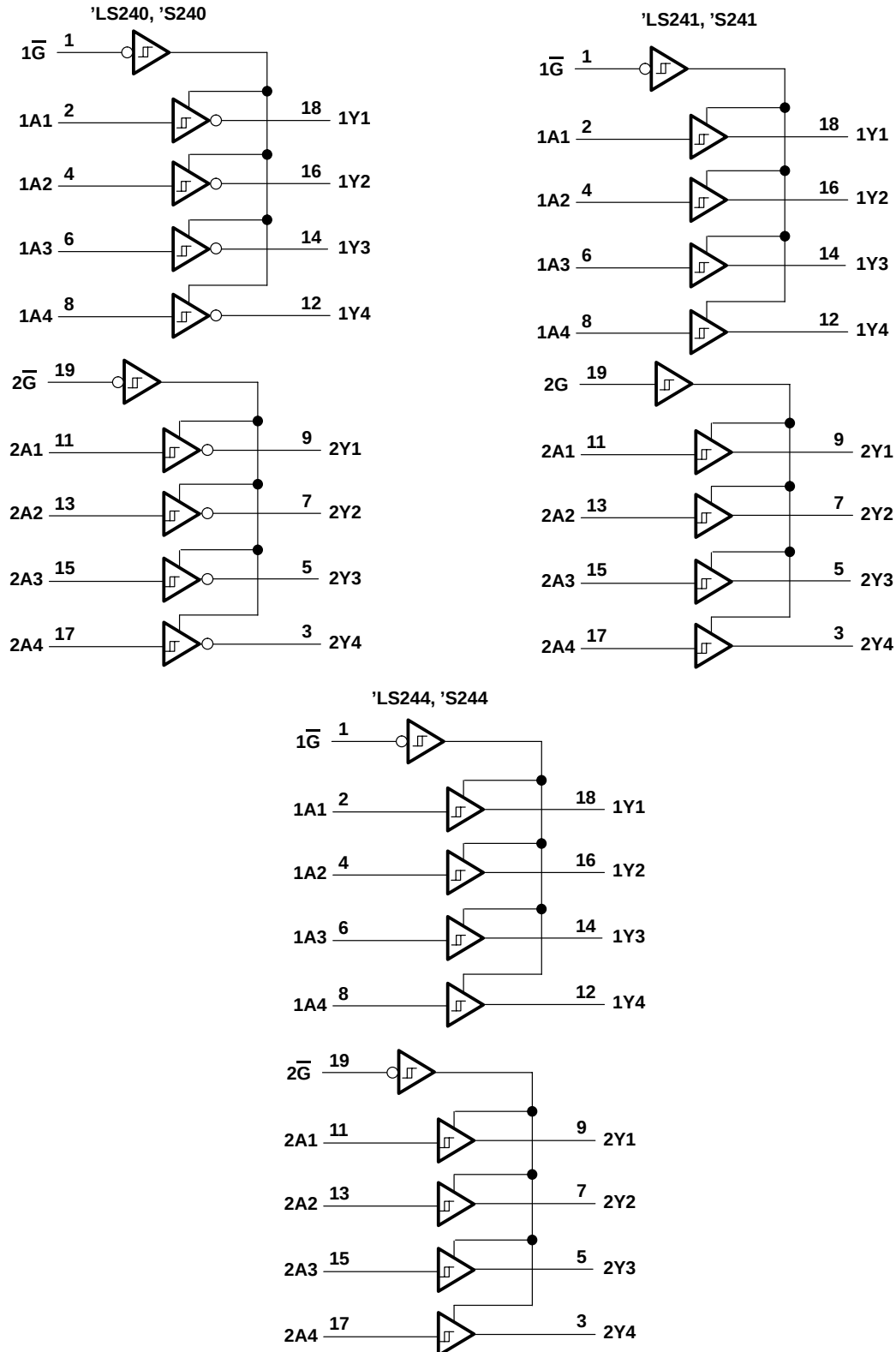
'S240, 'S241, 'S244



SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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logic diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages.



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SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : 'LS	7 V
'S	5.5 V
Off-state output voltage	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			–12			–15	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	–55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.



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SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN54LS'			SN74LS'			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = \text{MIN},$ $I_I = -18 \text{ mA}$					-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$			0.2	0.4		0.2	0.4		V
V_{OH}	$V_{CC} = \text{MIN},$ $I_{OH} = -3 \text{ mA}$	$V_{IH} = 2 \text{ V},$	$V_{IL} = \text{MAX},$	2.4	3.4		2.4	3.4		V
	$V_{CC} = \text{MIN},$ $I_{OH} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$V_{IL} = 0.5 \text{ V},$	2			2			
V_{OL}	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$I_{OL} = 12 \text{ mA}$			0.4			0.4	V
			$I_{OL} = 24 \text{ mA}$						0.5	
I_{OZH}	$V_{CC} = \text{MAX},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = \text{MAX},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = \text{MAX},$	$V_I = 7 \text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX},$	$V_I = 2.7 \text{ V}$				20			20	μA
I_{IL}	$V_{CC} = \text{MAX},$	$V_{IL} = 0.4 \text{ V}$				-0.2			-0.2	mA
$I_{OS}^{\S}$	$V_{CC} = \text{MAX},$			-40		-225	-40		-225	mA
I_{CC}	$V_{CC} = \text{MAX},$ Output open	Outputs high	All			17			17	mA
		Outputs low	'LS240			26			26	
			'LS241, 'LS244			27			27	
		Outputs disabled	'LS240			29			29	
			'LS241, 'LS244			32			32	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 667 \Omega,$	$C_L = 45 \text{ pF}$		9	14		12	18	ns
t_{PHL}				12	18		12	18	
t_{PZL}	$R_L = 667 \Omega,$	$C_L = 45 \text{ pF}$		20	30		20	30	ns
t_{PZH}				15	23		15	23	
t_{PLZ}	$R_L = 667 \Omega,$	$C_L = 5 \text{ pF}$		10	20		10	20	ns
t_{PHZ}				15	25		15	25	

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recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
	External resistance between any input and V_{CC} or ground			40			40	k Ω
T_A	Operating free-air temperature (see Note 3)	–55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = −18 mA			−1.2			−1.2			V
Hysteresis (V _{T+} − V _{T−})	V _{CC} = MIN			0.2	0.4		0.2	0.4		V
V _{OH}	V _{CC} = MIN I _{OH} = −1 mA	V _{IH} = 2 V,	V _{IL} = 0.8 V,				2.7			V
	V _{CC} = MIN, I _{OH} = −3 mA	V _{IH} = 2 V,	V _{IL} = 0.8 V,	2.4	3.4		2.4	3.4		
	V _{CC} = MIN, I _{OH} = MAX	V _{IH} = 2 V,	V _{IL} = 0.5 V,	2			2			
V _{OL}	V _{CC} = MIN, I _{OL} = MAX	V _{IH} = 2 V,	V _{IL} = 0.8 V,	0.55			0.55			V
I _{OZH}	V _{CC} = MAX, V _{IL} = 0.8 V	V _{IH} = 2 V,	V _O = 2.4 V	50			50			μA
I _{OZL}	V _{CC} = MAX, V _{IL} = 0.8 V	V _{IH} = 2 V,	V _O = 0.5 V	−50			−50			μA
I _I	V _{CC} = MAX,	V _I = 5.5 V		1			1			mA
I _{IH}	V _{CC} = MAX,	V _I = 2.7 V		50			50			μA
I _{IL}	V _{CC} = MAX,	V _I = 0.5 V	Any A	−400			−400			μA
			Any G	−2			−2			mA
I _{OS} §	V _{CC} = MAX			−50	−225		−50	−225		mA
I _{CC}	V _{CC} = MAX, Output open	Outputs high	'S240	80	123		80	135		mA
			'S241, 'S244	95	147		95	160		
		Outputs low	'S240	100	145		100	150		
			'S241, 'S244	120	170		120	180		
		Outputs disabled	'S240	100	145		100	150		
			'S241, 'S244	120	170		120	180		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.



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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

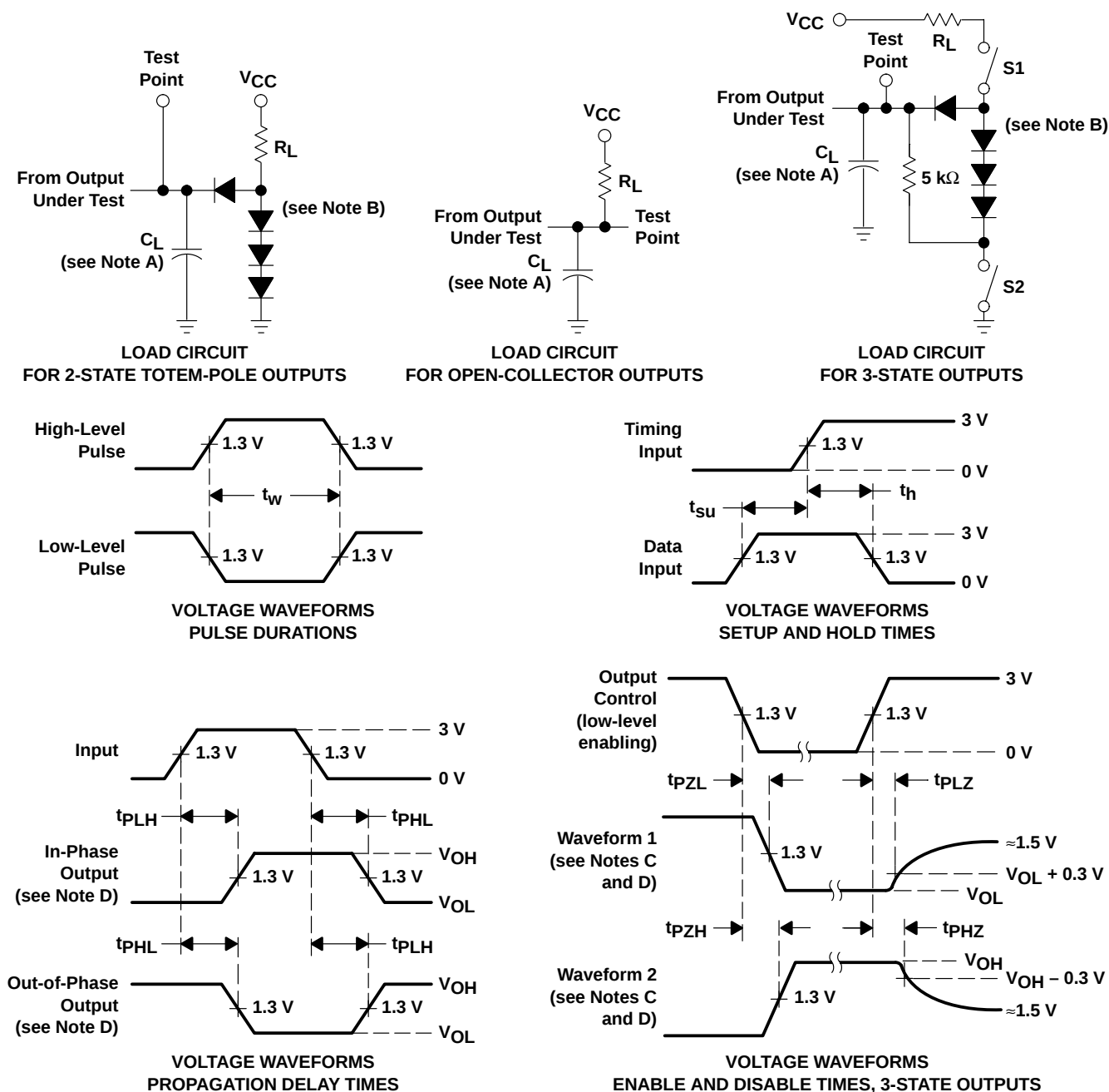
PARAMETER	TEST CONDITIONS	'S240			'S241, 'S244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 90\ \Omega$, $C_L = 50\text{ pF}$		4.5	7		6	9	ns
t_{PHL}			4.5	7		6	9	
t_{PZL}	$R_L = 90\ \Omega$, $C_L = 50\text{ pF}$		10	15		10	15	ns
t_{PZH}			6.5	10		8	12	
t_{PLZ}	$R_L = 90\ \Omega$, $C_L = 5\text{ pF}$		10	15		10	15	ns
t_{PHZ}			6	9		6	9	



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PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES



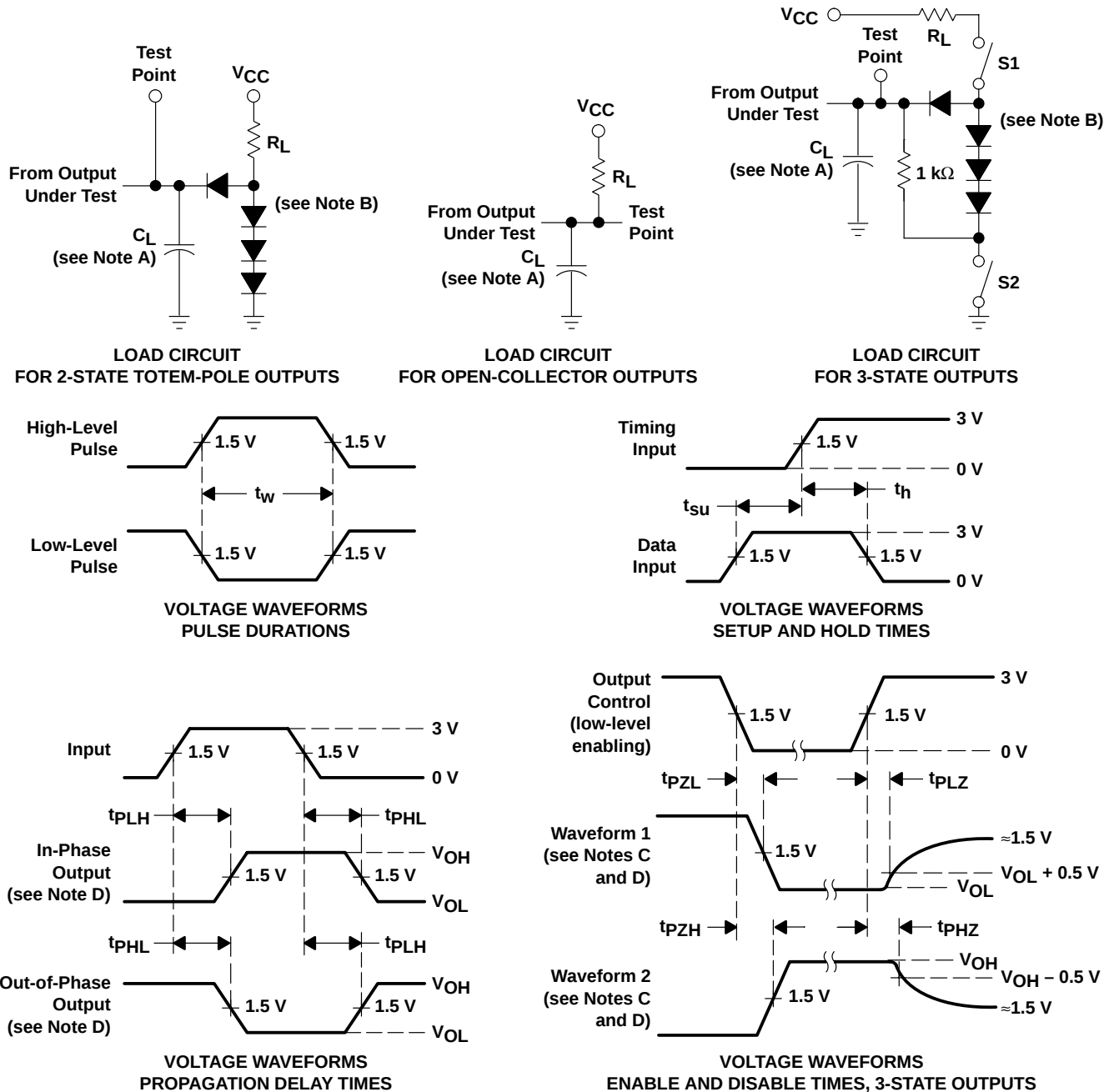
- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION SERIES 54S/74S DEVICES

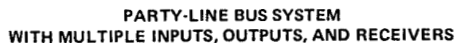


- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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APPLICATION INFORMATION



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