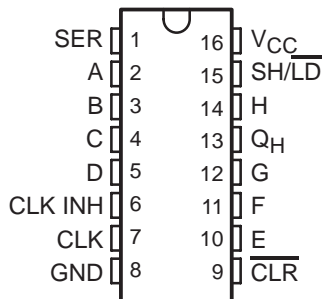


# SN54LV166A, SN74LV166A 8-BIT PARALLEL-LOAD SHIFT REGISTERS

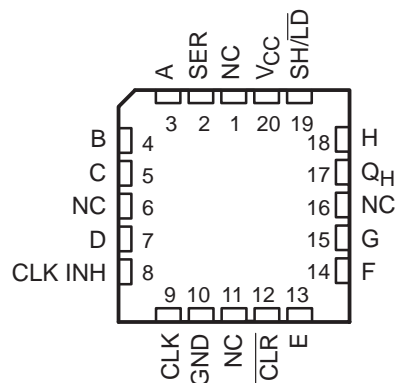
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 10.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down-Mode Operation
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54LV166A . . . J OR W PACKAGE  
SN74LV166A . . . D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV166A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'LV166A devices are 8-bit parallel-load shift registers, designed for 2-V to 5.5-V  $V_{CC}$  operation.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 40	SN74LV166AD	LV166A
		Reel of 2500	SN74LV166ADR	
	SOP – NS	Reel of 2000	SN74LV166ANSR	74LV166A
	SSOP – DB	Reel of 2000	SN74LV166ADBR	LV166A
	TSSOP – PW	Tube of 90	SN74LV166APW	LV166A
		Reel of 2000	SN74LV166APWR	
Reel of 250		SN74LV166APWT		
TVSOP – DGV	Reel of 2000	SN74LV166ADGVR	LV166A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV166AJ	SNJ54LV166AJ
	CFP – W	Tube of 150	SNJ54LV166AW	SNJ54LV166AW
	LCCC – FK	Tube of 55	SNJ54LV166AFK	SNJ54LV166AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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# SN54LV166A, SN74LV166A

## 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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### description/ordering information (continued)

The 'LV166A parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ( $\overline{\text{CLR}}$ ) input. The parallel-in or serial-in modes are established by the shift/load ( $\text{SH}/\overline{\text{LD}}$ ) input. When high,  $\text{SH}/\overline{\text{LD}}$  enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high.  $\overline{\text{CLR}}$  overrides all other inputs, including CLK, and resets all flip-flops to zero.

These devices are fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

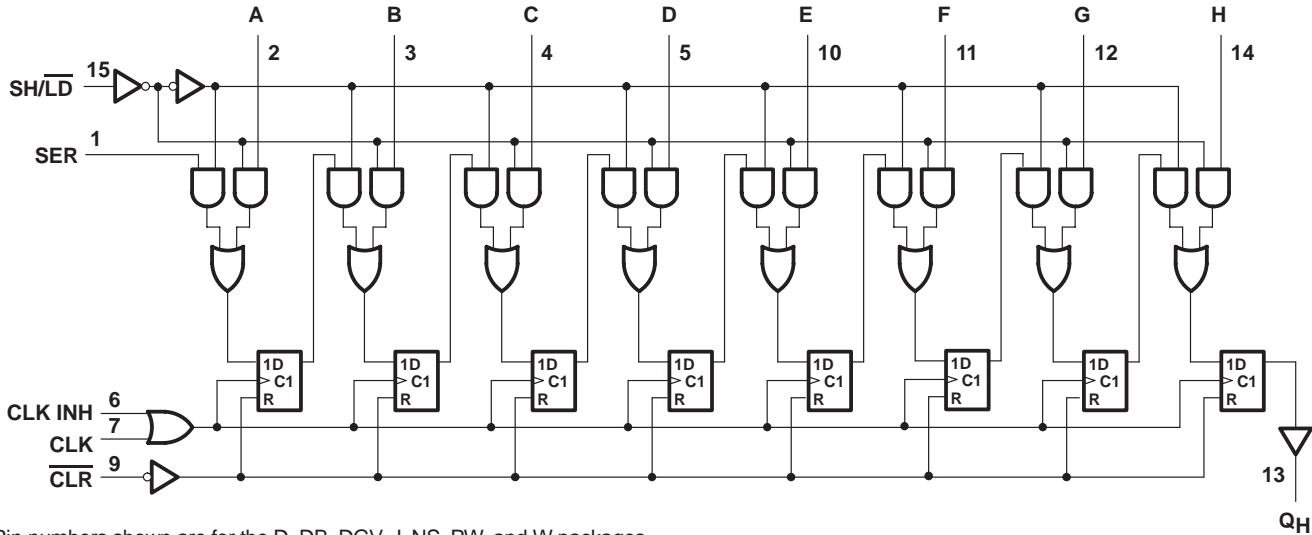
FUNCTION TABLE

INPUTS						OUTPUTS		
						INTERNAL		Q <sub>H</sub>
$\overline{\text{CLR}}$	$\text{SH}/\overline{\text{LD}}$	CLK INH	CLK	SER	PARALLEL A . . . H	Q <sub>A</sub>	Q <sub>B</sub>	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>

# SN54LV166A, SN74LV166A 8-BIT PARALLEL-LOAD SHIFT REGISTERS

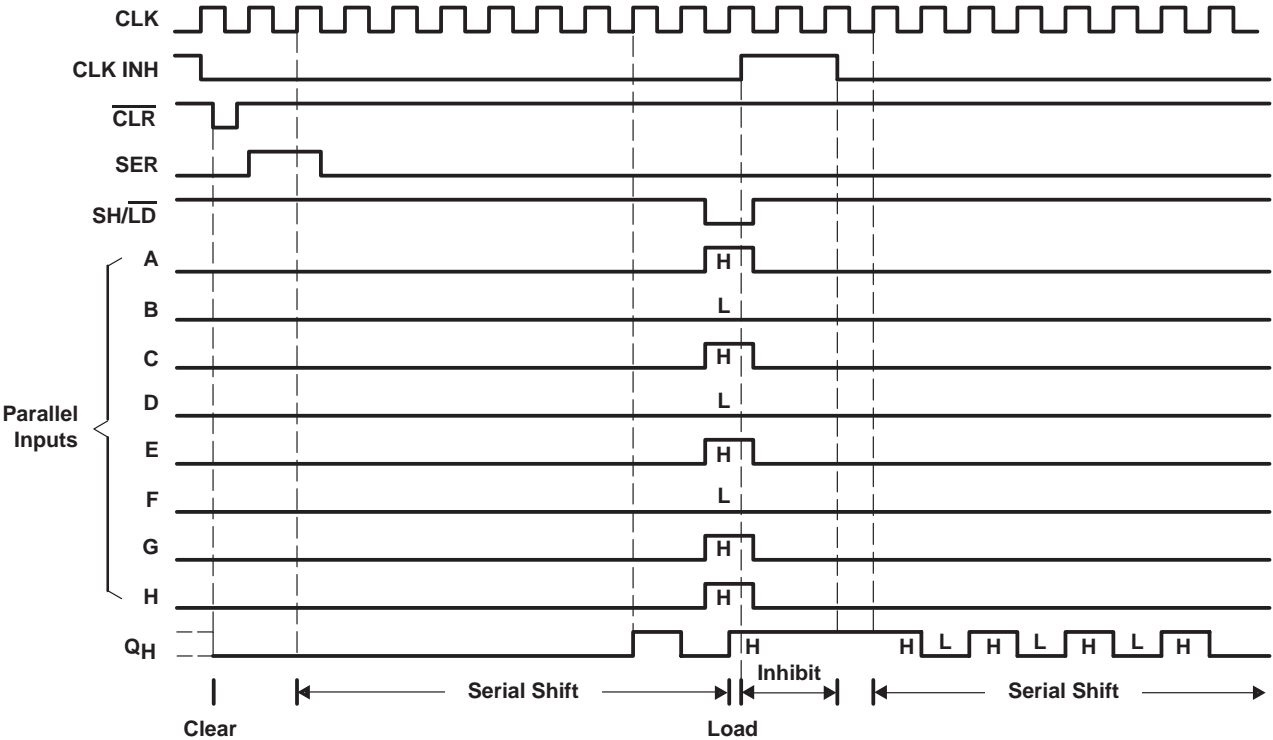
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## logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

## typical clear, shift, load, inhibit, and shift sequence



# SN54LV166A, SN74LV166A

## 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range applied in high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any output in the power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	73°C/W
DB package .....	82°C/W
DGV package .....	120°C/W
NS package .....	64°C/W
PW package .....	108°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



# SN54LV166A, SN74LV166A 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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## recommended operating conditions (see Note 4)

		SN54LV166A		SN74LV166A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	0.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	-50	-50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	-2	-2		mA
		V <sub>CC</sub> = 3 V to 3.6 V	-6	-6		
		V <sub>CC</sub> = 4.5 V to 5.5 V	-12	-12		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	2		mA
		V <sub>CC</sub> = 3 V to 3.6 V	6	6		
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	12		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	200		ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	100		
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	20		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV166A			SN74LV166A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4			0.4	
	I <sub>OL</sub> = 6 mA	3 V			0.44			0.44	
	I <sub>OL</sub> = 12 mA	4.5 V			0.55			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20			20	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5			5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.6			1.6		pF

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# SN54LV166A, SN74LV166A 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV166A		SN74LV166A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	8	9	9	9	ns	
		CLK high or low	8.5	9	9	9		
$t_{su}$	Setup time	CLK INH before CLK $\uparrow$	7	7	7	7	ns	
		Data before CLK $\uparrow$	6.5	8.5	8.5	8.5		
		SH/ $\overline{\text{LD}}$ before CLK $\uparrow$	7	8.5	8.5	8.5		
		SER before CLK $\uparrow$	8.5	9.5	9.5	9.5		
$t_h$	Hold time	$\overline{\text{CLR}}$ $\uparrow$ inactive before CLK $\uparrow$	6	7	7	7	ns	
		Data after CLK $\uparrow$	-0.5	0	0	0		

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV166A		SN74LV166A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	6	7	7	7	ns	
		CLK high or low	6	7	7	7		
$t_{su}$	Setup time	CLK INH before CLK $\uparrow$	5	5	5	5	ns	
		Data before CLK $\uparrow$	5	6	6	6		
		SH/ $\overline{\text{LD}}$ before CLK $\uparrow$	5	6	6	6		
		SER before CLK $\uparrow$	5	6	6	6		
$t_h$	Hold time	$\overline{\text{CLR}}$ $\uparrow$ inactive before CLK $\uparrow$	4	4	4	4	ns	
		Data after CLK $\uparrow$	0	0	0	0		

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV166A		SN74LV166A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	5	5	5	5	ns	
		CLK high or low	4	4	4	4		
$t_{su}$	Setup time	CLK INH before CLK $\uparrow$	3.5	3.5	3.5	3.5	ns	
		Data before CLK $\uparrow$	4.5	4.5	4.5	4.5		
		SH/ $\overline{\text{LD}}$ before CLK $\uparrow$	4	4	4	4		
		SER before CLK $\uparrow$	4	4	4	4		
$t_h$	Hold time	$\overline{\text{CLR}}$ $\uparrow$ inactive before CLK $\uparrow$	3.5	3.5	3.5	3.5	ns	
		Data after CLK $\uparrow$	1	1	1	1		

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# SN54LV166A, SN74LV166A 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV166A		SN74LV166A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	50*	105*		45*		45		MHz
			$C_L = 50\text{ pF}$	40	80		35		35		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	$Q_H$	$C_L = 15\text{ pF}$		8.8*	16*	1*	18*	1	18	ns
$t_{\text{pd}}$	CLK				9.2*	19.8*	1*	22*	1	22	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	$Q_H$	$C_L = 50\text{ pF}$		11.3	19.5	1	22	1	22	ns
$t_{\text{pd}}$	CLK				11.8	23.3	1	26	1	26	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV166A		SN74LV166A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	65*	150*		55*		55		MHz
			$C_L = 50\text{ pF}$	60	120		50		50		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	$Q_H$	$C_L = 15\text{ pF}$		6.3*	12.5*	1*	15*	1	15	ns
$t_{\text{pd}}$	CLK				6.6*	15.4*	1*	18*	1	18	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	$Q_H$	$C_L = 50\text{ pF}$		7.9	16.3	1	18.5	1	18.5	ns
$t_{\text{pd}}$	CLK				8.3	18.9	1	21.5	1	21.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV166A		SN74LV166A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	110*	205*		90*		90		MHz
			$C_L = 50\text{ pF}$	95	160		85		85		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	$Q_H$	$C_L = 15\text{ pF}$		4.6*	8.6*	1*	10*	1	10	ns
$t_{\text{pd}}$	CLK				4.8*	9.9*	1*	11.5*	1	11.5	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	$Q_H$	$C_L = 50\text{ pF}$		5.7	10.6	1	12	1	12	ns
$t_{\text{pd}}$	CLK				6.1	11.9	1	13.5	1	13.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	39.1	pF
		5 V	44.5	

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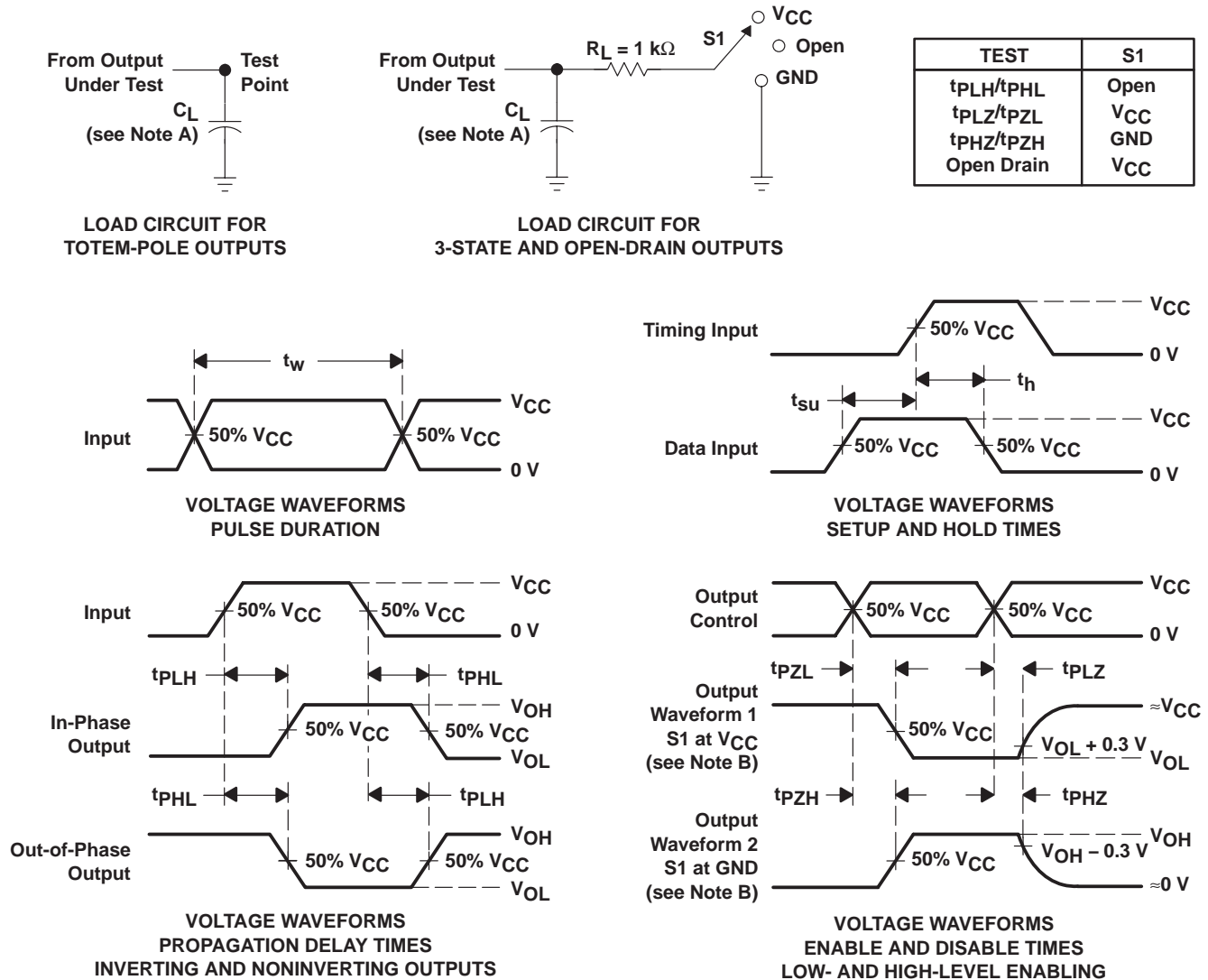


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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV166AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV166APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV166ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV166ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV166ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV166ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV166APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV166ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV166ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV166ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV166ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV166APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

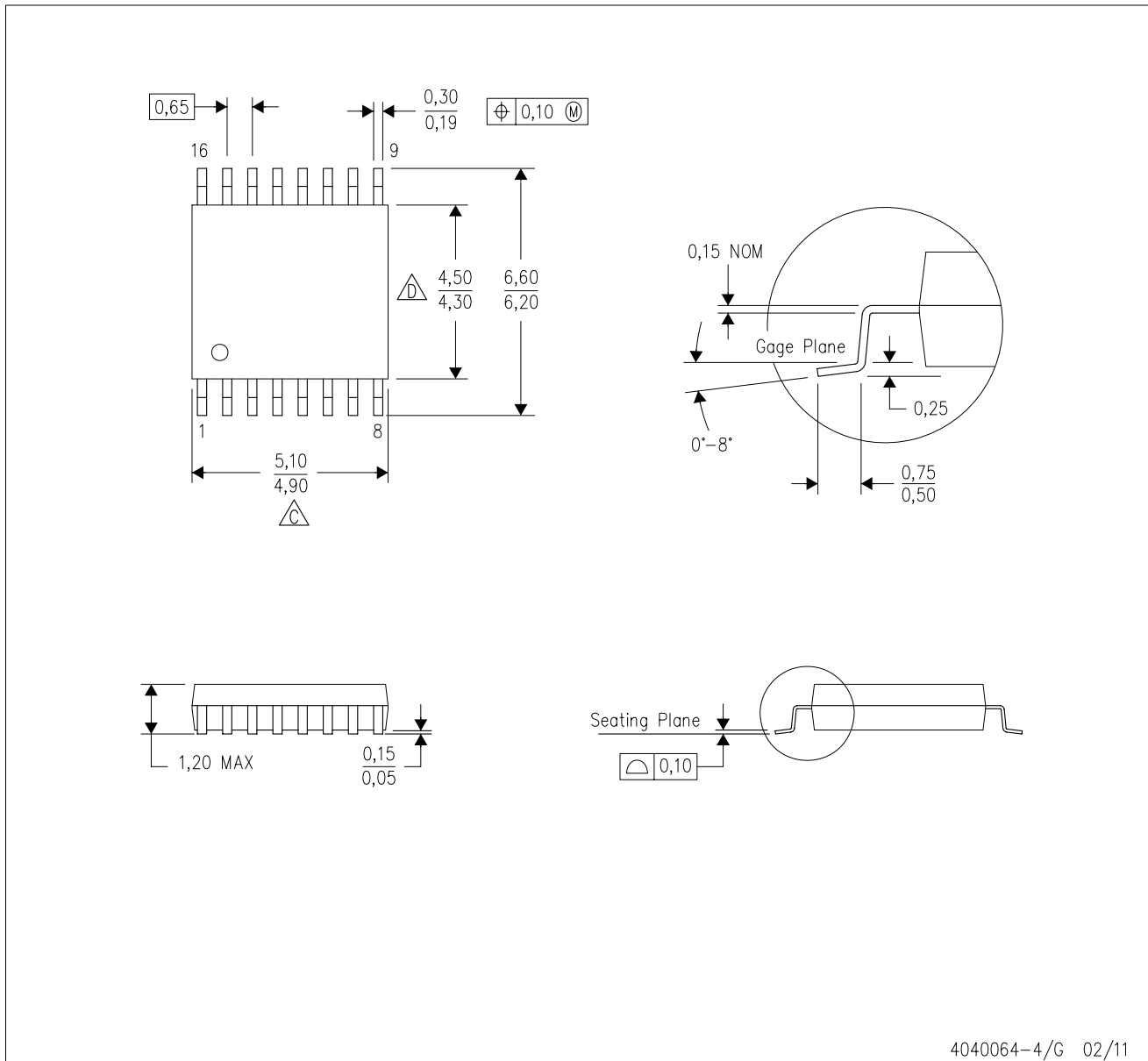


4040047-6/M 06/11



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

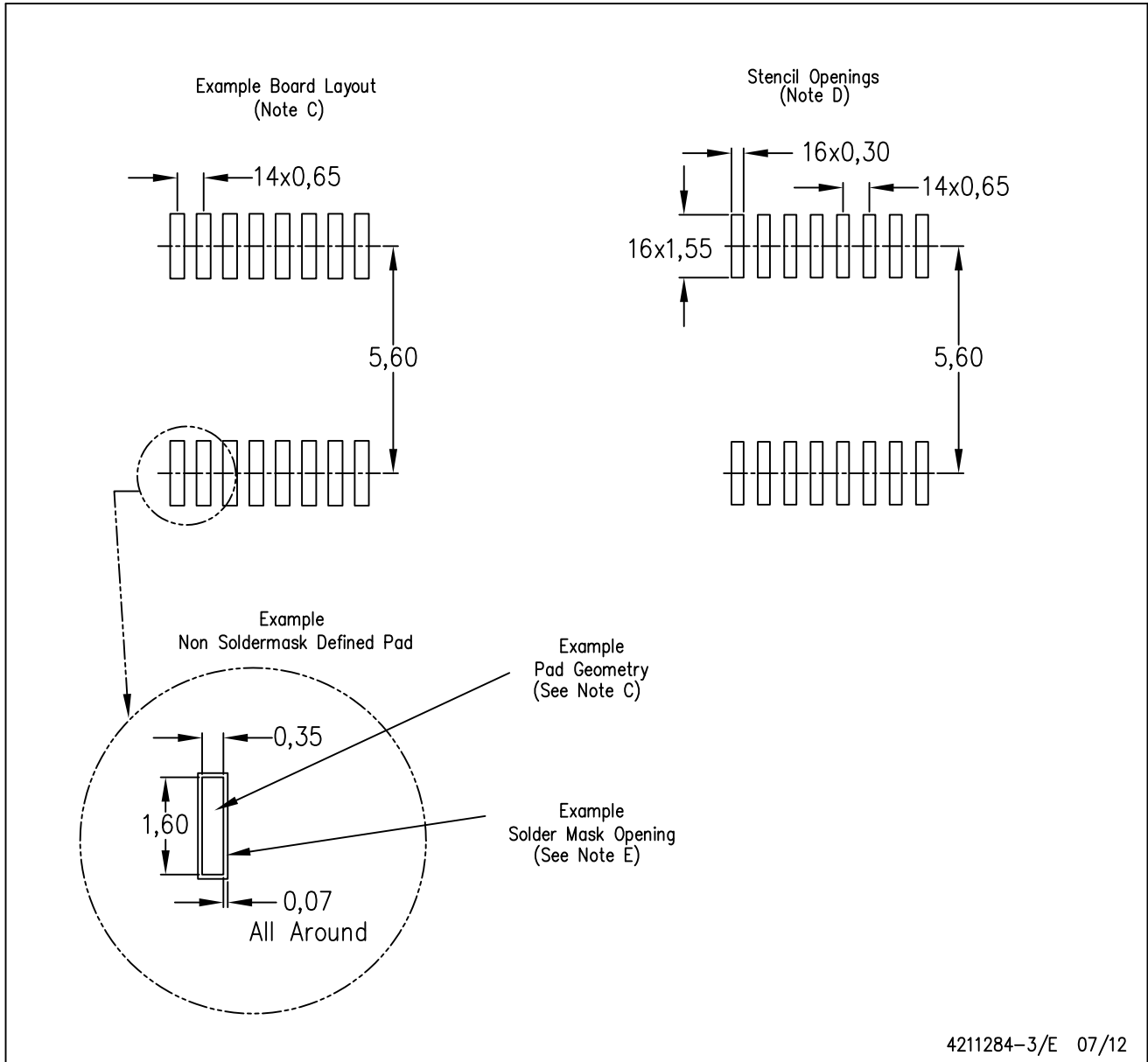


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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