

SN74HSTL16918 9-BIT TO 18-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

SCES096C – APRIL 1997 – REVISED JANUARY 1999

- Member of the Texas Instruments Widebus™ Family
- Inputs Meet JEDEC HSTL Std JESD 8-6 and Outputs Meet Level III Specifications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Thin Shrink Small-Outline Package

description

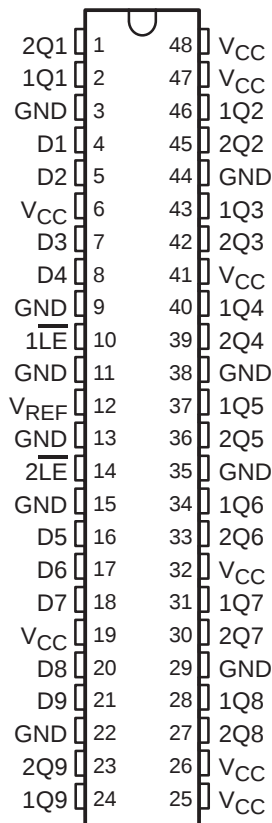
This 9-bit to 18-bit D-type latch is designed for 3.15-V to 3.45-V V_{CC} operation. The D inputs accept HSTL levels and the Q outputs provide LVTTL levels.

The SN74HSTL16918 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable ($\overline{LE}$) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While $\overline{LE}$ is low, the Q outputs of the corresponding nine latches follow the D inputs. When $\overline{LE}$ is taken high, the Q outputs are latched at the levels set up at the D inputs.

The SN74HSTL16918 is characterized for operation from 0°C to 70°C.

DGG PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{LE}$	D	Q
L	H	H
L	L	L
H	X	$Q_0^\dagger$

[†] Output level before the indicated steady-state input conditions were established



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

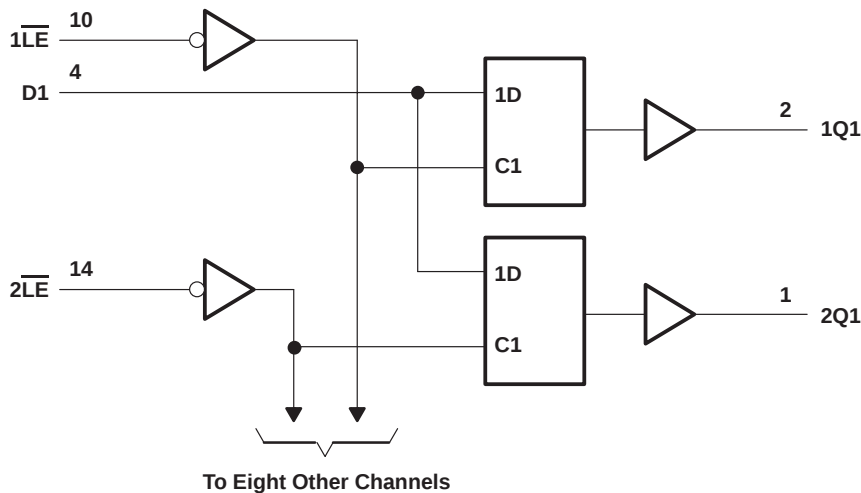
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	89°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.15		3.45	V
V_{REF}	Reference voltage	0.68	0.75	0.9	V
V_I	Input voltage	0		1.5	V
V_{IH}	AC high-level input voltage	All inputs	$V_{REF}+200$ mV		V
V_{IL}	AC low-level input voltage	All inputs	$V_{REF}-200$ mV		V
V_{IH}	DC high-level input voltage	All inputs	$V_{REF}+100$ mV		V
V_{IL}	DC low-level input voltage	All inputs	$V_{REF}-100$ mV		V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 3.15\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 3.15\text{ V}$, $I_{OH} = -24\text{ mA}$	2.4			V
V_{OL}		$V_{CC} = 3.15\text{ V}$, $I_{OL} = 24\text{ mA}$			0.5	V
I_I	Control inputs	$V_{CC} = 3.45\text{ V}$	$V_I = 0\text{ or }1.5\text{ V}$		±5	μA
	Data inputs		$V_I = 0\text{ or }1.5\text{ V}$		±5	
	V_{REF}		$V_{REF} = 0.68\text{ V or }0.9\text{ V}$		90	
I_{CC}		$V_{CC} = 3.45\text{ V}$, $V_I = 0\text{ or }1.5\text{ V}$		50	100	mA
C_i	Control inputs	$V_{CC} = 0\text{ or }3.3\text{ V}$, $V_I = 0\text{ or }3.3\text{ V}$		2		pF
	Data inputs	$V_{CC} = 0\text{ or }3.3\text{ V}$, $V_I = 0\text{ or }3.3\text{ V}$		2.5		
C_o	Outputs	$V_{CC} = 0$, $V_O = 0$		4		pF

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ low		3		ns
t_{su}	Setup time, D before $\overline{LE}\uparrow$		2		ns
t_h	Hold time	D after $\overline{LE}\uparrow$	1		ns
$t_{ldr}^\ddagger$	Data race condition time	D after $\overline{LE}\downarrow$		0	ns

[‡] This is the maximum time after $\overline{LE}$ switches low that the data input can return to the latched state from the opposite state without producing a glitch on the output.

switching characteristics over recommended operating free-air temperature range, $V_{REF} = 0.75\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.9	3.4	ns
	$\overline{LE}$		1.9	4.2	

simultaneous switching characteristics over recommended operating free-air temperature range, $V_{REF} = 0.75\text{ V}$ [§]

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.9	4.4	ns
	$\overline{LE}$		1.9	5.2	

[§] All outputs switching

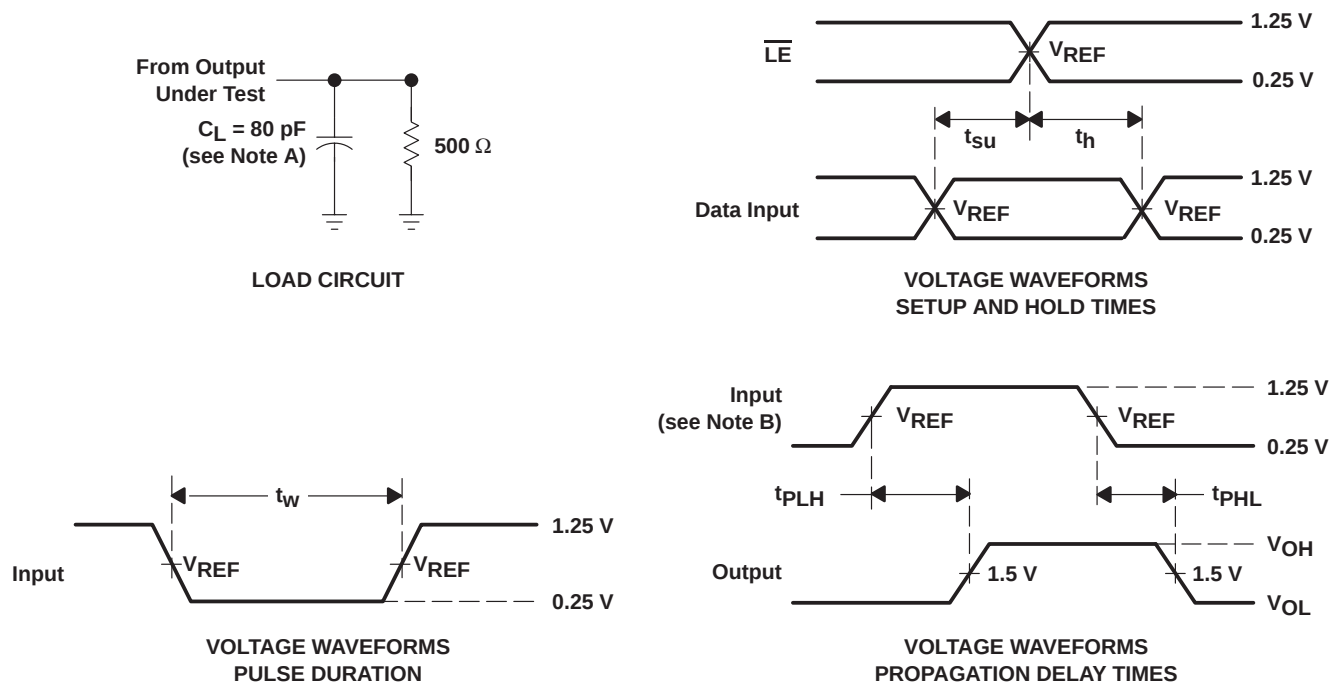


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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 1 \text{ ns}$, $t_f \leq 1 \text{ ns}$.
 C. The outputs are measured one at a time with one transition per measurement.
 D. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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