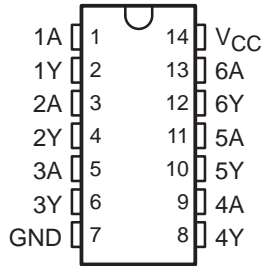


SN54HCU04, SN74HCU04 HEX INVERTERS

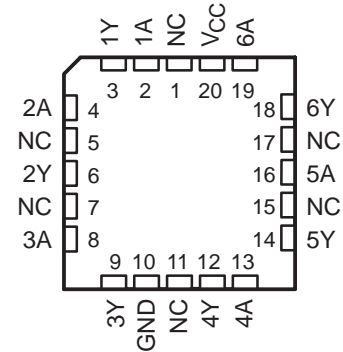
SCLS079E – MARCH 1984 – REVISED MARCH 2004

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 7$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Unbuffered Outputs

SN54HCU04 . . . J OR W PACKAGE
SN74HCU04 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCU04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HCU04 devices contain six independent inverters. They perform the Boolean function $Y = \bar{A}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HCU04N	SN74HCU04N
	SOIC – D	Tube of 50	SN74HCU04D	HCU04
		Reel of 2500	SN74HCU04DR	
		Reel of 250	SN74HCU04DT	
	SOP – NS	Reel of 2000	SN74HCU04NSR	HCU04
	SSOP – DB	Reel of 2000	SN74HCU04DBR	HU04
	TSSOP – PW	Reel of 90	SN74HCU04PW	HCU04
Reel of 2000		SN74HCU04PWR		
Reel of 250		SN74HCU04PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCU04J	SNJ54HCU04J
	CFP – W	Tube of 150	SNJ54HCU04W	SNJ54HCU04W
	LCCC – FK	Tube of 55	SNJ54HCU04FK	SNJ54HCU04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HCU04, SN74HCU04 HEX INVERTERS

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FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HCU04			SN74HCU04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.7	1.7		V	
		$V_{CC} = 4.5$ V		3.6	3.6			
		$V_{CC} = 6$ V		4.8	4.8			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5		V	
		$V_{CC} = 4.5$ V			1.35			
		$V_{CC} = 6$ V			1.8			
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54HCU04, SN74HCU04 HEX INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{CC} or GND	I _{OH} = -20 μA	2 V	1.8			1.8		1.8	V	
			4.5 V	4			4		4		
			6 V	5.5			5.5		5.5		
		I _{OH} = -4 mA	4.5 V	3.98			3.7		3.84		
		I _{OH} = -5.2 mA	6 V	5.48			5.2		5.34		
V _{OL}	V _I = V _{CC} or GND	I _{OL} = 20 μA	2 V			0.2		0.2	0.2	V	
			4.5 V			0.5		0.5	0.5		
			6 V			0.5		0.5	0.5		
		I _{OL} = 4 mA	4.5 V			0.26		0.4	0.33		
		I _{OL} = 5.2 mA	6 V			0.26		0.4	0.33		
I _I	V _I = V _{CC} or 0		6 V			±100		±1000	±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			2		40	20	μA	
C _i			2 V to 6 V		3	10		10	10	pF	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2 V		40	80		120		100	ns
			4.5 V		8	16		24		20	
			6 V		7	14		20		17	
t _f		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

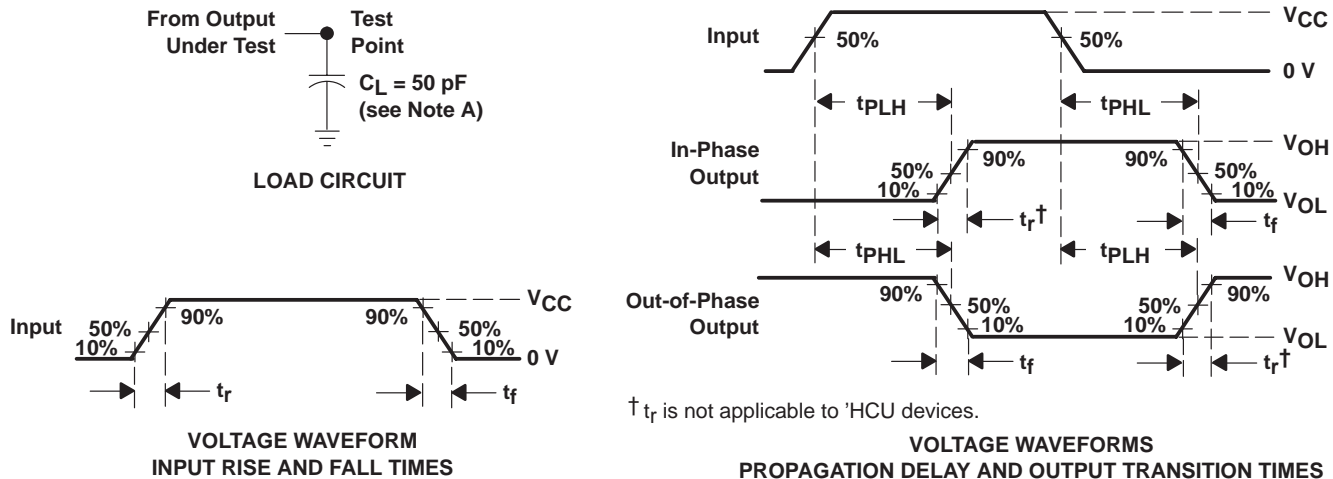
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per inverter	No load	20	pF



SN54HCU04, SN74HCU04 HEX INVERTERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time, with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



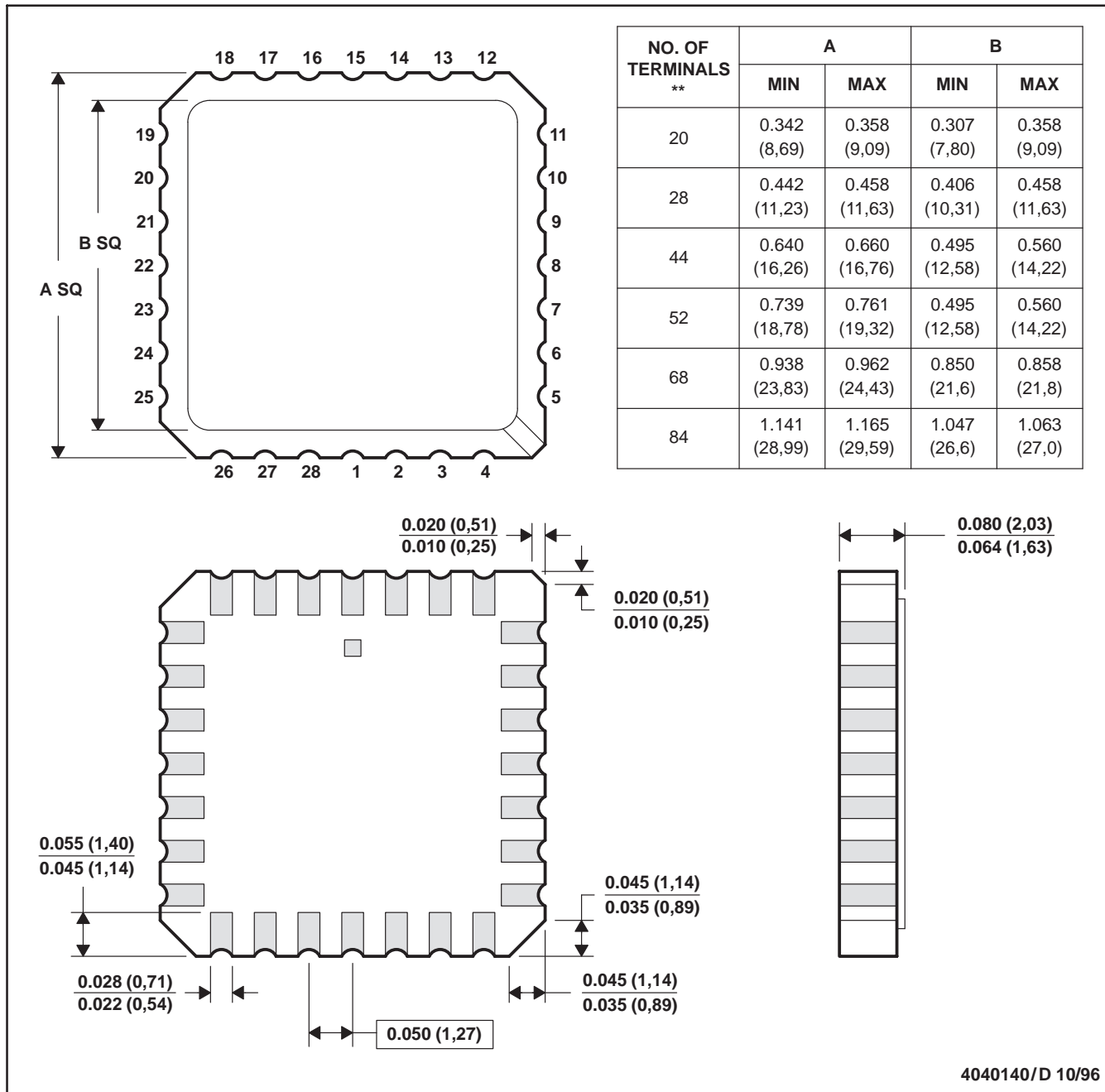
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

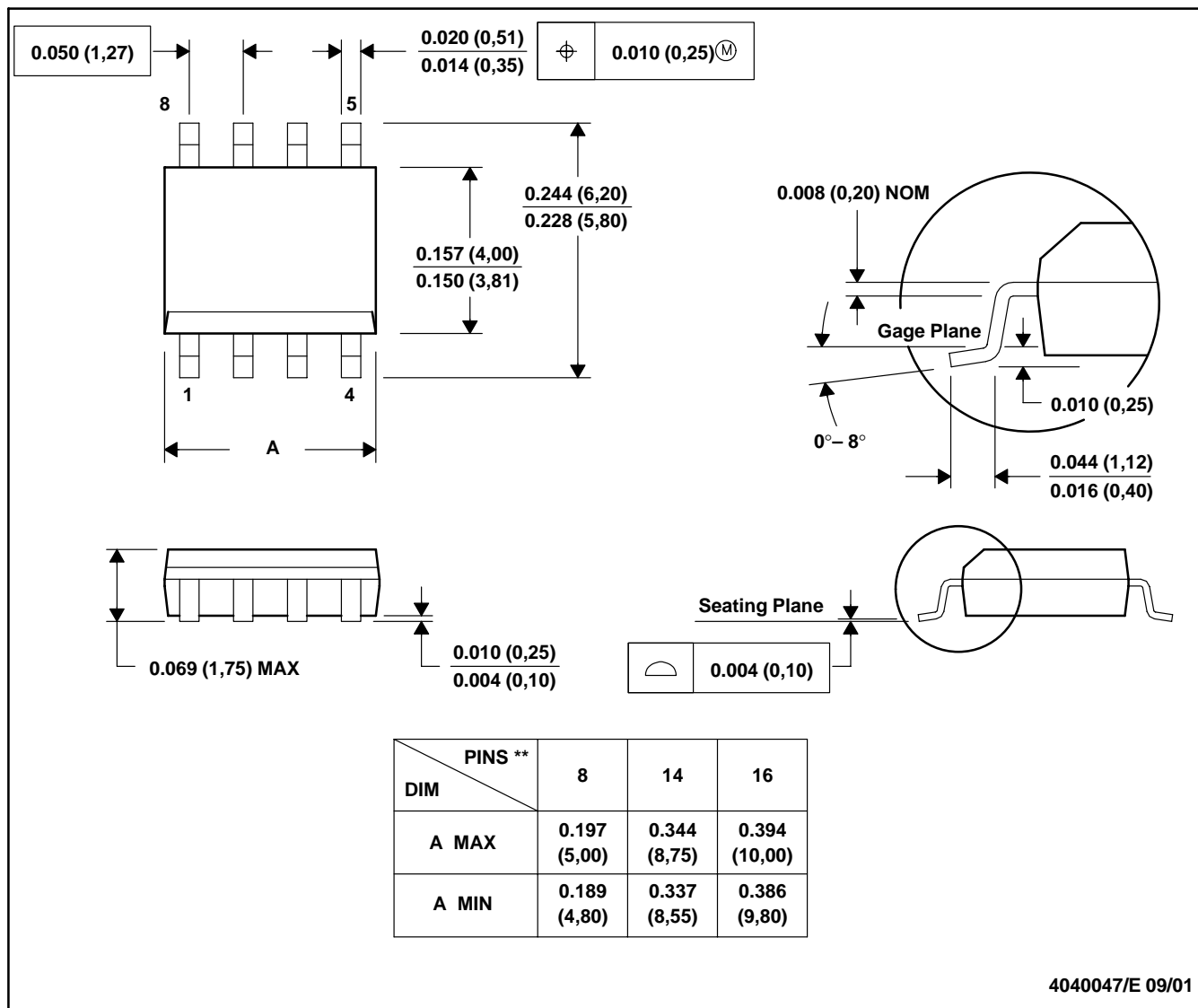


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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