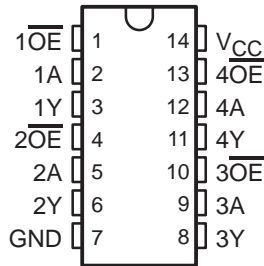


SN54HCT125, SN74HCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

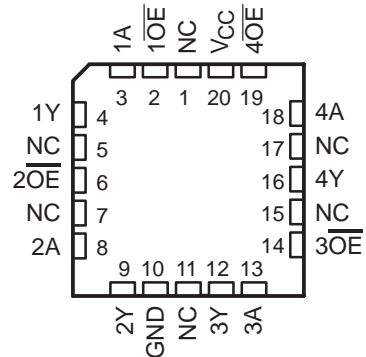
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- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current Outputs Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- High-Current 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

SN54HCT125 . . . J OR W PACKAGE
SN74HCT125 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCT125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HCT125N	SN74HCT125N
	SOIC – D	Tube of 50	SN74HCT125D	HCT125
		Reel of 2500	SN74HCT125DR	
		Reel of 250	SN74HCT125DT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT125J	SNJ54HCT125J
	CFP – W	Tube of 150	SNJ54HCT125W	SNJ54HCT125W
	LCCC – FK	Tube of 55	SNJ54HCT125FK	SNJ54HCT125FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54HCT125, SN74HCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
		I _{OH} = -6 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1	0.1	V	
		I _{OL} = 6 mA			0.17	0.26		0.4	0.33		
I _I	V _I = V _{CC} or 0		5.5 V		±0.1	±100		±1000	±1000	nA	
I _{OZ}	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}		5.5 V		±0.01	±0.5		±10	±5	μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			8		160	80	μA	
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4		3	2.9	mA	
C _i			4.5 V to 5.5 V		3	10		10*	10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	4.5 V		15	26		39		33	ns
			5.5 V		12	23		35		30	
t _{en}	\overline{OE}	Y	4.5 V		18	28		42		35	ns
			5.5 V		15	25		38		31	
t _{dis}	\overline{OE}	Y	4.5 V		15	26		39		33	ns
			5.5 V		13	23		35		30	
t _t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	4.5 V		19	36		58		46	ns
			5.5 V		16	32		48		42	
t _{en}	\overline{OE}	Y	4.5 V		25	40		60		50	ns
			5.5 V		21	35		53		43	
t _t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	35	pF

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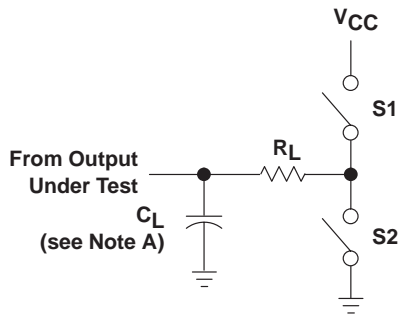


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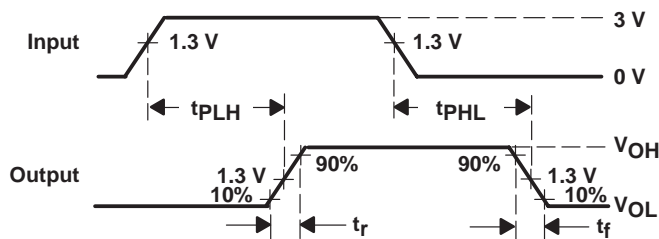
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

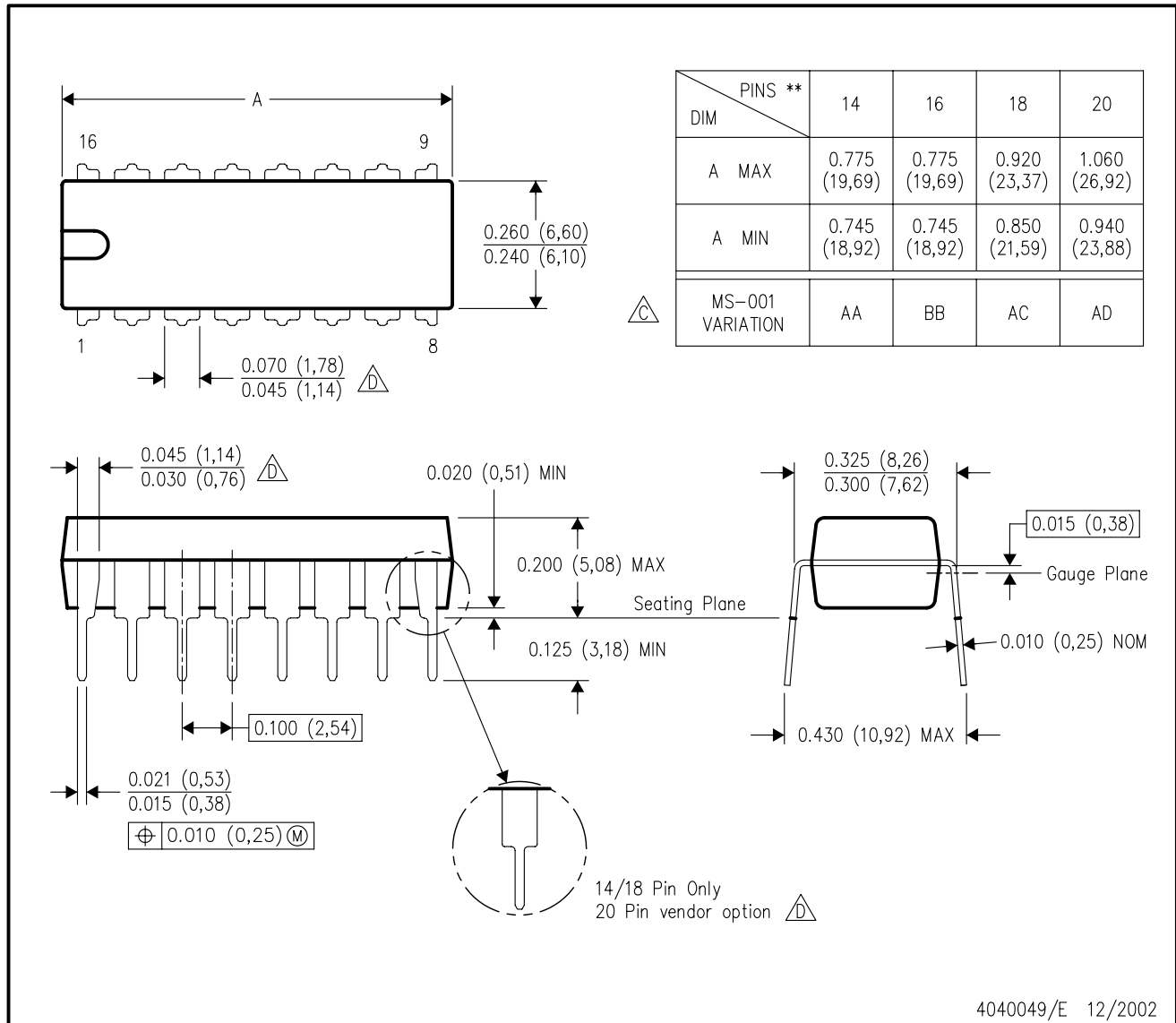
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

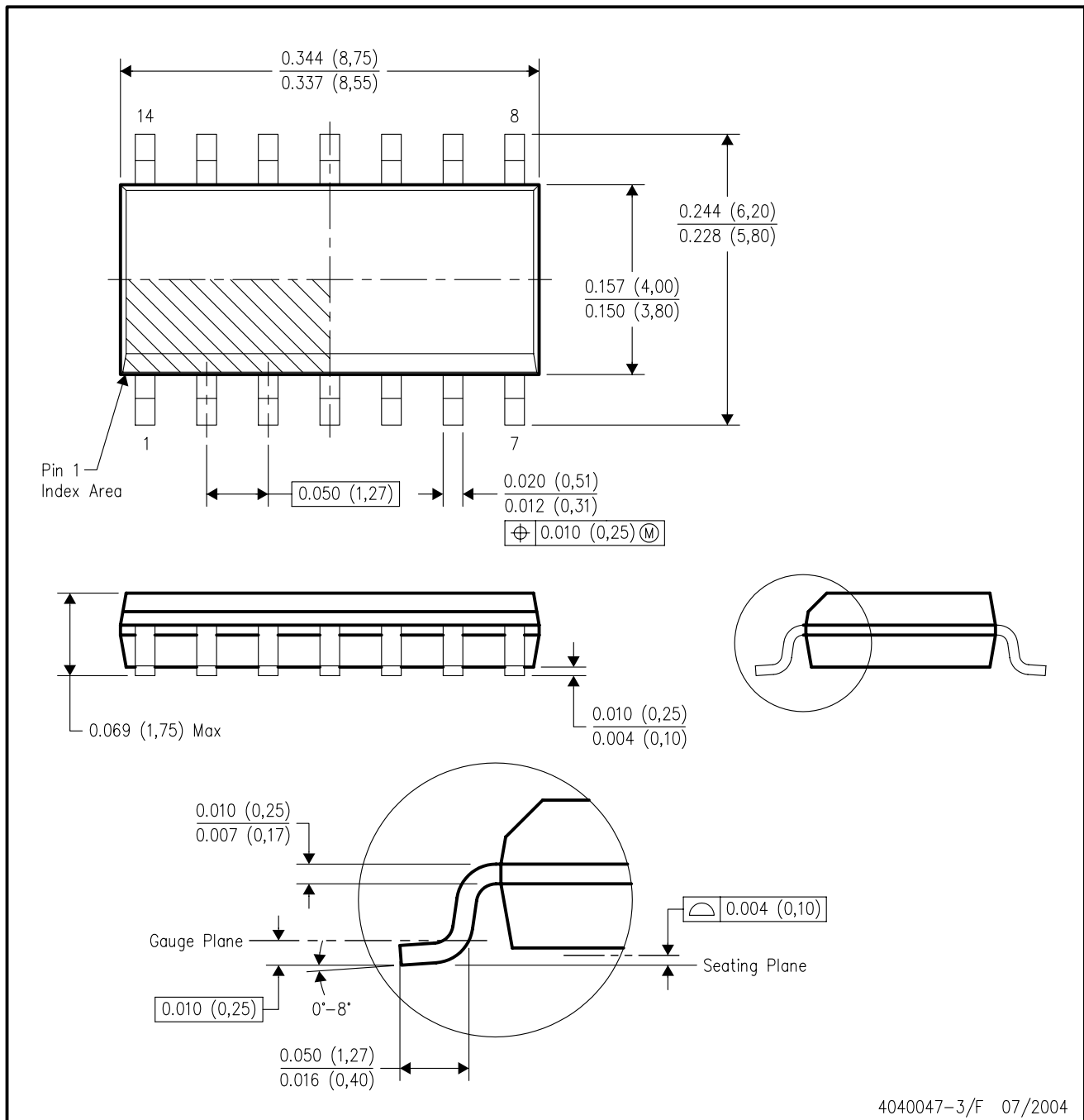


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

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