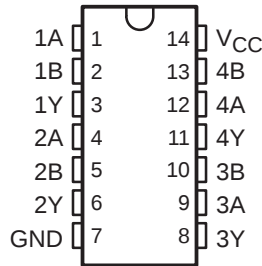


# SN54HCT00, SN74HCT00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

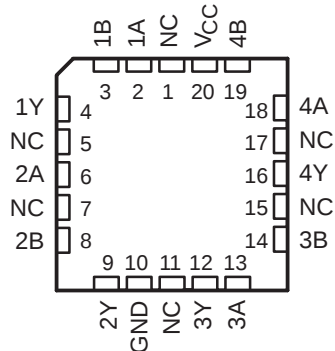
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- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 10$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible

SN54HCT00 . . . J OR W PACKAGE  
SN74HCT00 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCT00 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices contain four independent 2-input NAND gates. They perform the Boolean function  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†   |              | ORDERABLE<br>PART NUMBER | TOP-SIDE<br>MARKING |
|----------------|------------|--------------|--------------------------|---------------------|
| –40°C to 85°C  | PDIP – N   | Tube of 25   | SN74HCT00N               | SN74HCT00N          |
|                | SOIC – D   | Tube of 50   | SN74HCT00D               | HCT00               |
|                |            | Reel of 2500 | SN74HCT00DR              |                     |
|                |            | Reel of 250  | SN74HCT00DT              |                     |
|                | SOP – NS   | Reel of 2000 | SN74HCT00NSR             | HCT00               |
|                | SSOP – DB  | Reel of 2000 | SN74HCT00DBR             | HT00                |
|                | TSSOP – PW | Tube of 90   | SN74HCT00PW              | HT00                |
|                |            | Reel of 2000 | SN74HCT00PWR             |                     |
| Reel of 250    |            | SN74HCT00PWT |                          |                     |
| –55°C to 125°C | CDIP – J   | Tube of 25   | SNJ54HCT00J              | SNJ54HCT00J         |
|                | CFP – W    | Tube of 150  | SNJ54HCT00W              | SNJ54HCT00W         |
|                | LCCC – FK  | Tube of 55   | SNJ54HCT00FK             | SNJ54HCT00FK        |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
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SN54HCT00, SN74HCT00  
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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FUNCTION TABLE  
(each gate)

| INPUTS |   | OUTPUT<br>Y |
|--------|---|-------------|
| A      | B |             |
| H      | H | L           |
| L      | X | H           |
| X      | L | H           |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                             |               |
|-----------------------------------------------------------------------------|---------------|
| Supply voltage range, $V_{CC}$                                              | –0.5 V to 7 V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)  | ±20 mA        |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) | ±20 mA        |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                  | ±25 mA        |
| Continuous current through $V_{CC}$ or GND                                  | ±50 mA        |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):                      |               |
| D package                                                                   | 86°C/W        |
| DB package                                                                  | 96°C/W        |
| N package                                                                   | 80°C/W        |
| NS package                                                                  | 76°C/W        |
| PW package                                                                  | 113°C/W       |

|                                      |                |
|--------------------------------------|----------------|
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |
|--------------------------------------|----------------|

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

|                     |                                 | SN54HCT00                               |     |          | SN74HCT00 |     |          | UNIT |
|---------------------|---------------------------------|-----------------------------------------|-----|----------|-----------|-----|----------|------|
|                     |                                 | MIN                                     | NOM | MAX      | MIN       | NOM | MAX      |      |
| $V_{CC}$            | Supply voltage                  | 4.5                                     | 5   | 5.5      | 4.5       | 5   | 5.5      | V    |
| $V_{IH}$            | High-level input voltage        | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ |     |          | 2         |     |          | V    |
| $V_{IL}$            | Low-level input voltage         | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ |     |          | 0.8       |     |          | V    |
| $V_I$               | Input voltage                   | 0                                       |     | $V_{CC}$ | 0         |     | $V_{CC}$ | V    |
| $V_O$               | Output voltage                  | 0                                       |     | $V_{CC}$ | 0         |     | $V_{CC}$ | V    |
| $\Delta t/\Delta v$ | Input transition rise/fall time |                                         |     | 500      |           |     | 500      | ns   |
| $T_A$               | Operating free-air temperature  | –55                                     |     | 125      | –40       |     | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54HCT00, SN74HCT00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS                                                      |                          | V <sub>CC</sub>   | T <sub>A</sub> = 25°C |       |      | SN54HCT00 |       | SN74HCT00 |       | UNIT |
|-------------------------------|----------------------------------------------------------------------|--------------------------|-------------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
|                               |                                                                      |                          |                   | MIN                   | TYP   | MAX  | MIN       | MAX   | MIN       | MAX   |      |
| V <sub>OH</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                  | I <sub>OH</sub> = -20 µA | 4.5 V             | 4.4                   | 4.499 |      | 4.4       |       | 4.4       |       | V    |
|                               |                                                                      | I <sub>OH</sub> = -4 mA  |                   | 3.98                  | 4.3   |      | 3.7       |       | 3.84      |       |      |
| V <sub>OL</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                  | I <sub>OL</sub> = 20 µA  | 4.5 V             |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   | V    |
|                               |                                                                      | I <sub>OL</sub> = 4 mA   |                   |                       | 0.17  | 0.26 |           | 0.4   |           | 0.33  |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or 0                                |                          | 5.5 V             |                       | ±0.1  | ±100 |           | ±1000 |           | ±1000 | nA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0            |                          | 5.5 V             |                       |       | 2    |           | 40    |           | 20    | µA   |
| ΔI <sub>CC</sub> <sup>†</sup> | One input at 0.5 V or 2.4 V,<br>Other inputs at 0 or V <sub>CC</sub> |                          | 5.5 V             |                       | 1.4   | 2.4  |           | 3     |           | 2.9   | mA   |
| C <sub>i</sub>                |                                                                      |                          | 4.5 V<br>to 5.5 V |                       | 3     | 10   |           | 10    |           | 10    | pF   |

<sup>†</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT00 |     | SN74HCT00 |     | UNIT |
|-----------------|--------------|-------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
|                 |              |             |                 | MIN                   | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>pd</sub> | A or B       | Y           | 4.5 V           |                       | 11  | 20  |           | 30  |           | 25  | ns   |
|                 |              |             | 5.5 V           |                       | 10  | 18  |           | 27  |           | 22  |      |
| t <sub>t</sub>  |              | Y           | 4.5 V           |                       | 9   | 15  |           | 22  |           | 19  | ns   |
|                 |              |             | 5.5 V           |                       | 8   | 14  |           | 20  |           | 17  |      |

operating characteristics, T<sub>A</sub> = 25°C

| PARAMETER                                              | TEST CONDITIONS | TYP | UNIT |
|--------------------------------------------------------|-----------------|-----|------|
| C <sub>pd</sub> Power dissipation capacitance per gate | No load         | 20  | pF   |

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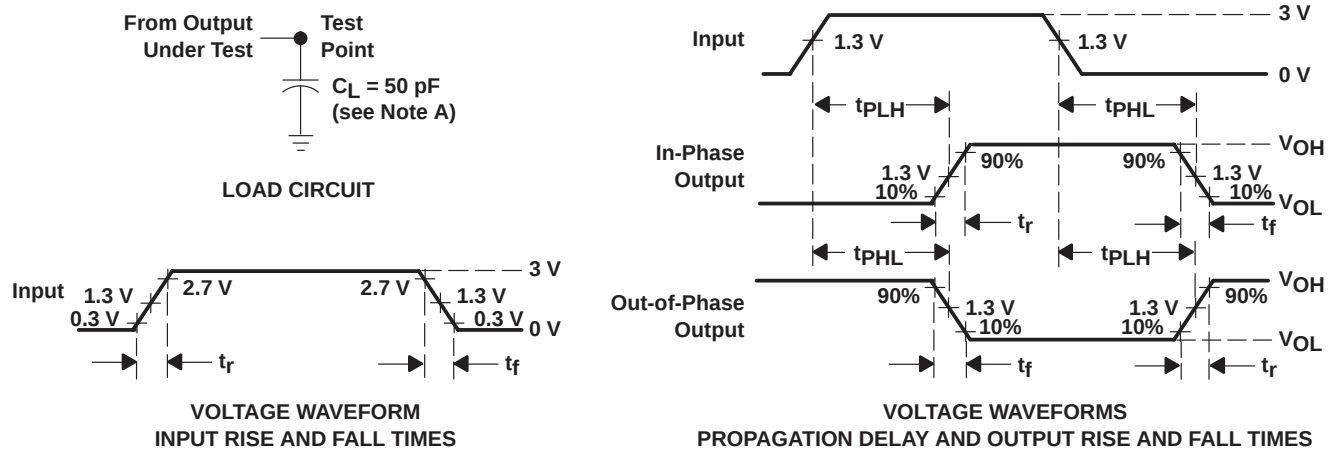


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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

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**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74HCT00D       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DBR     | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DBRE4   | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DBRG4   | ACTIVE                | SSOP         | DB              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DE4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DG4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DR      | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DRE4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DRG4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DT      | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DTE4    | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00DTG4    | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00N       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74HCT00NE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74HCT00NSR     | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00NSRE4   | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00NSRG4   | ACTIVE                | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PW      | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWE4    | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWG4    | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWLE    | OBSOLETE              | TSSOP        | PW              | 14   |             | TBD                     | Call TI          | Call TI                      |
| SN74HCT00PWR     | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWRE4   | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWRG4   | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWT     | ACTIVE                | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74HCT00PWTE4   | ACTIVE                | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HCT00PWTE4   | ACTIVE                | TSSOP        | PW              | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT00DBR | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74HCT00DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HCT00DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HCT00NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74HCT00PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 7.0     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT00DBR | SSOP         | DB              | 14   | 2000 | 346.0       | 346.0      | 33.0        |
| SN74HCT00DR  | SOIC         | D               | 14   | 2500 | 346.0       | 346.0      | 33.0        |
| SN74HCT00DR  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74HCT00NSR | SO           | NS              | 14   | 2000 | 346.0       | 346.0      | 33.0        |
| SN74HCT00PWR | TSSOP        | PW              | 14   | 2000 | 346.0       | 346.0      | 29.0        |

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

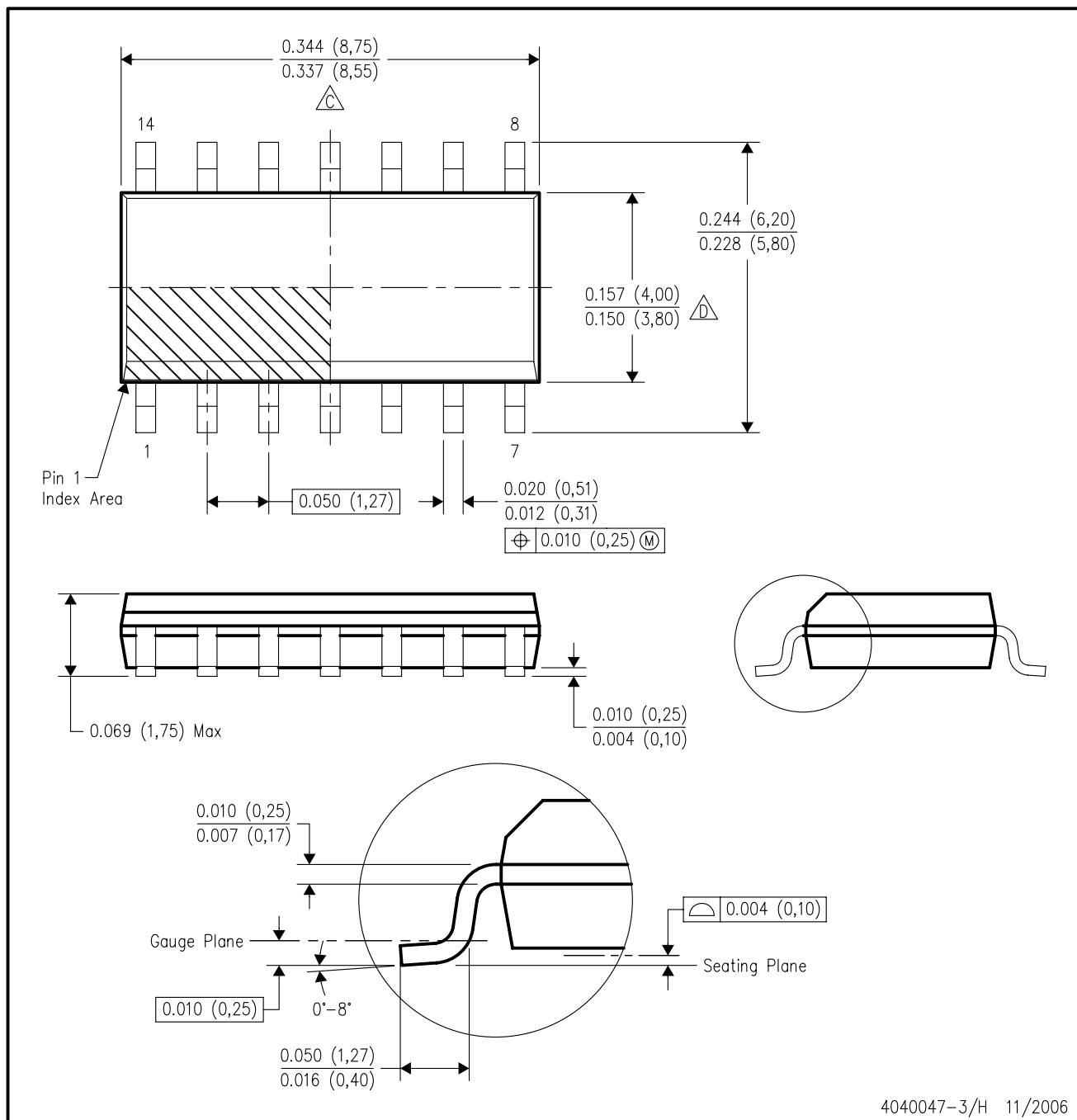
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
 Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.