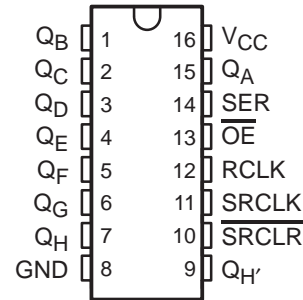


# SN54HC595, SN74HC595 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS041G – DECEMBER 1982 – REVISED FEBRUARY 2004

- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 13$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Shift Register Has Direct Clear

SN54HC595 . . . J OR W PACKAGE  
SN74HC595 . . . D, DB, DW, N, OR NS PACKAGE  
(TOP VIEW)

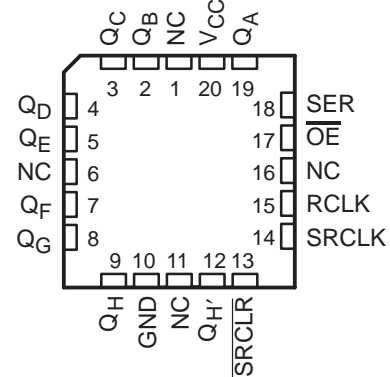


## description/ordering information

The 'HC595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ( $\overline{SRCLR}$ ) input, serial (SER) input, and serial outputs for cascading. When the output-enable ( $\overline{OE}$ ) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

SN54HC595 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC595N	SN74HC595N
	SOIC – D	Tube of 40	SN74HC595D	HC595
		Reel of 2500	SN74HC595DR	
		Reel of 250	SN74HC595DT	
	SOIC – DW	Tube of 40	SN74HC595DW	HC595
		Reel of 2000	SN74HC595DWR	
-55°C to 125°C	SOP – NS	Reel of 2000	SN74HC595NSR	HC595
	SSOP – DB	Reel of 2000	SN74HC595DBR	HC595
	CDIP – J	Tube of 25	SNJ54HC595J	SNJ54HC595J
	CFP – W	Tube of 150	SNJ54HC595W	SNJ54HC595W
	LCCC – FK	Tube of 55	SNJ54HC595FK	SNJ54HC595FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

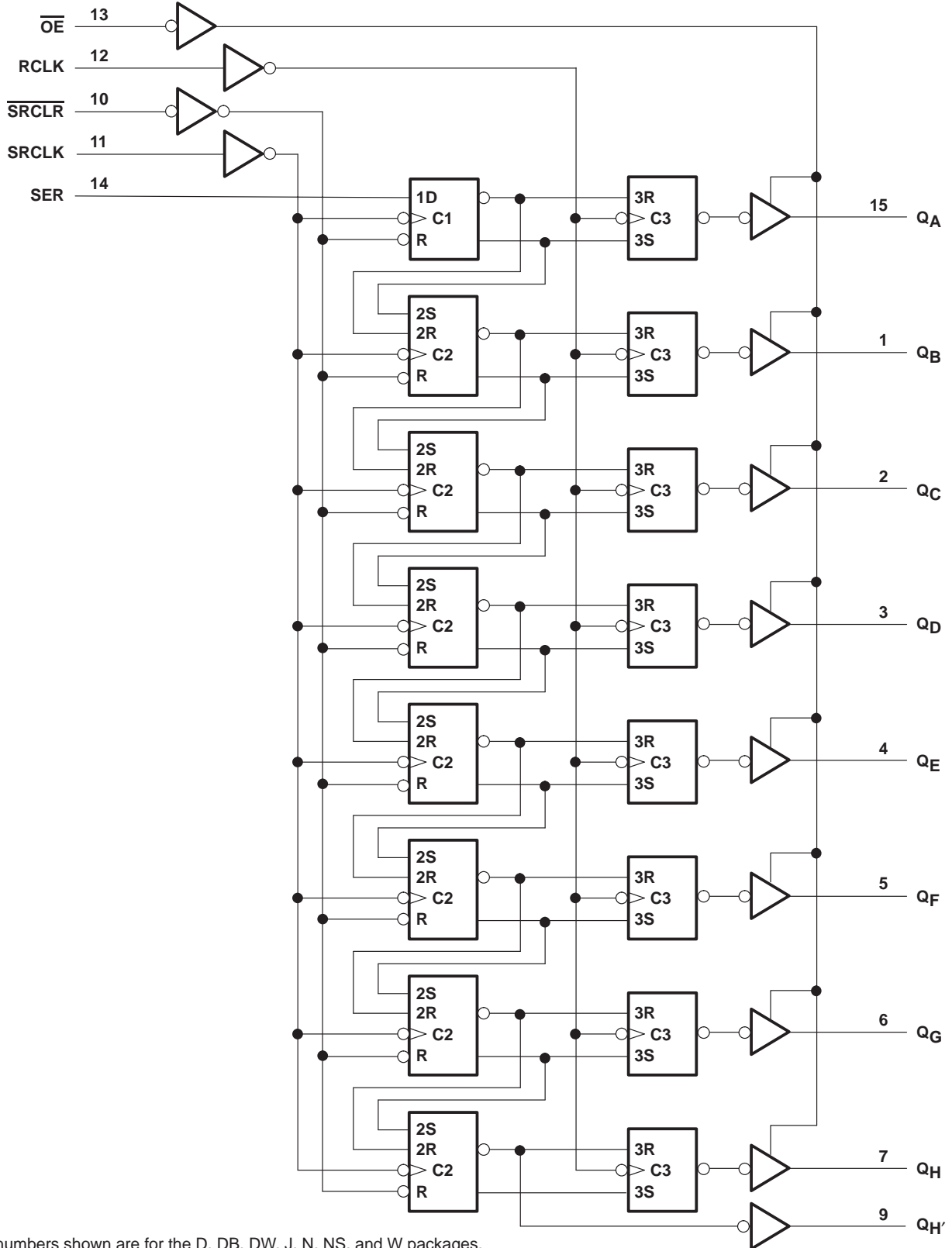
**SN54HC595, SN74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

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**FUNCTION TABLE**

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	
X	X	X	X	H	Outputs Q <sub>A</sub> –Q <sub>H</sub> are disabled.
X	X	X	X	L	Outputs Q <sub>A</sub> –Q <sub>H</sub> are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

logic diagram (positive logic)

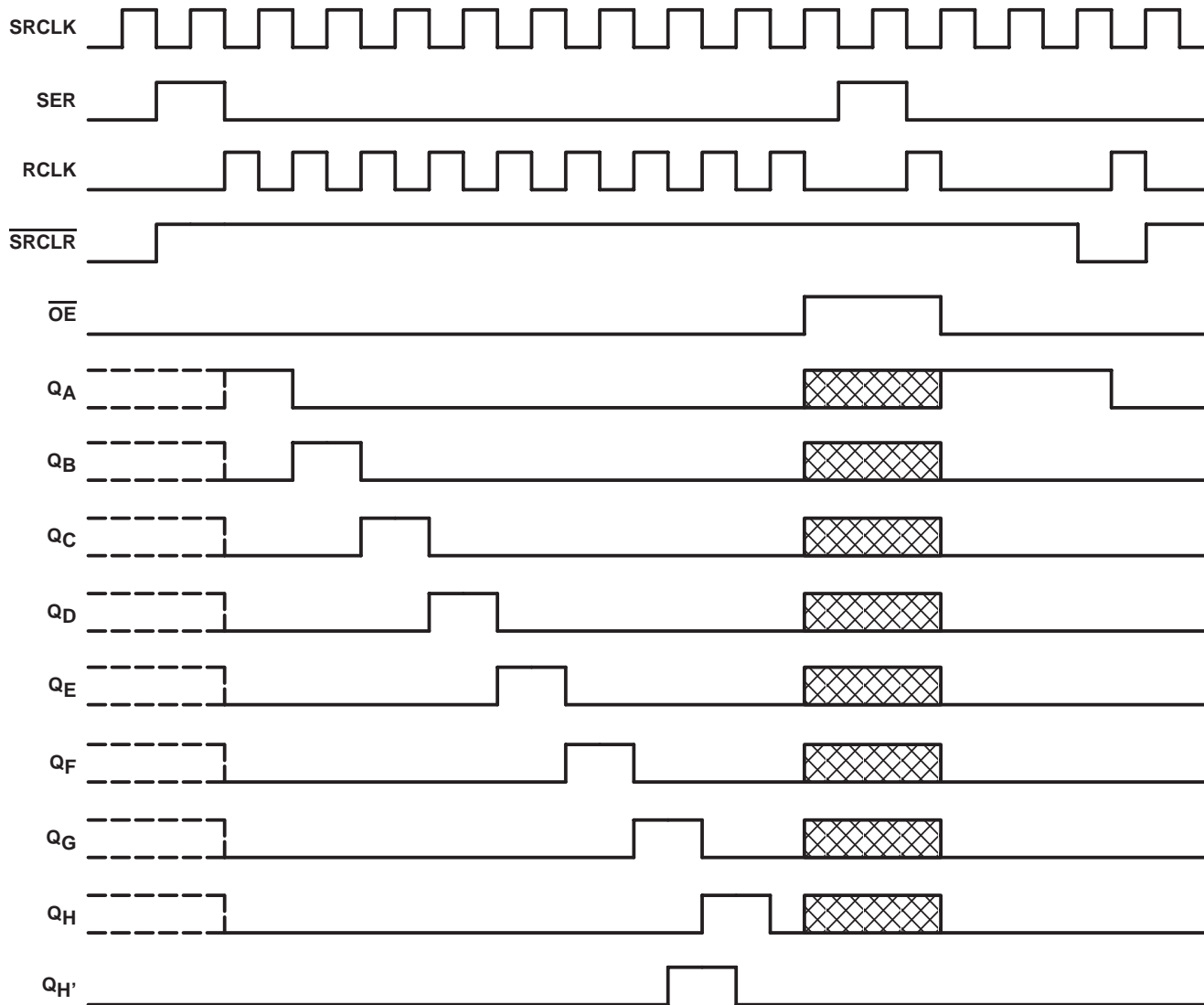



Pin numbers shown are for the D, DB, DW, J, N, NS, and W packages.

# SN54HC595, SN74HC595 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

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## timing diagram



NOTE:  implies that the output is in 3-State mode.

**SN54HC595, SN74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±35 mA
Continuous current through $V_{CC}$ or GND .....	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	73°C/W
DB package .....	82°C/W
DW package .....	57°C/W
N package .....	67°C/W
NS package .....	64°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		SN54HC595			SN74HC595			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V			$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V			$V_{CC} = 6$ V		1.8	
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$ ‡	Input transition rise/fall time	$V_{CC} = 2$ V			$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V			$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V			$V_{CC} = 6$ V		400	
$T_A$	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from  $V_{IL,max} = 0.5$  V to  $V_{IH,min} = 1.5$  V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_f = 1000$  ns and  $V_{CC} = 2$  V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



**SN54HC595, SN74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		4.5 V	Q <sub>H</sub> ', I <sub>OH</sub> = -4 mA	3.98	4.3		3.7		3.84		
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -6 mA	3.98	4.3		3.7		3.84		
		6 V	Q <sub>H</sub> ', I <sub>OH</sub> = -5.2 mA	5.48	5.8		5.2		5.34		
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -7.8 mA	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		V	
			4.5 V		0.001	0.1		0.1			
			6 V		0.001	0.1		0.1			
		4.5 V	Q <sub>H</sub> ', I <sub>OL</sub> = 4 mA		0.17	0.26		0.4			0.33
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 6 mA		0.17	0.26		0.4			0.33
		6 V	Q <sub>H</sub> ', I <sub>OL</sub> = 5.2 mA		0.15	0.26		0.4			0.33
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 7.8 mA		0.15	0.26		0.4			0.33
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000	nA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, Q <sub>A</sub> -Q <sub>H</sub>	6 V		±0.01	±0.5		±10		±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8		160		80	μA	
C <sub>i</sub>		2 V to 6 V			3	10		10		10	pF



**SN54HC595, SN74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**  
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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC595		SN74HC595		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	6		4.2		5		MHz
		4.5 V	31		21		25		
		6 V	36		25		29		
t <sub>w</sub>	SRCLK or RCLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	$\overline{\text{SRCLR}}$ low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t <sub>su</sub>	SER before SRCLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	SRCLK↑ before RCLK↑†	2 V	75		113		94		
		4.5 V	15		23		19		
		6 V	13		19		16		
	$\overline{\text{SRCLR}}$ low before RCLK↑	2 V	50		75		65		
		4.5 V	10		15		13		
		6 V	9		13		11		
	$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2 V	50		75		60		
		4.5 V	10		15		12		
		6 V	9		13		11		
t <sub>h</sub>	Hold time, SER after SRCLK↑	2 V	0		0		0		ns
		4.5 V	0		0		0		
		6 V	0		0		0		

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

**SN54HC595, SN74HC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	26		4.2		5	MHz	
			4.5 V	31	38		21		25		
			6 V	36	42		25		29		
t <sub>pd</sub>	SRCLK	Q <sub>H'</sub>	2 V		50	160		240		200	ns
			4.5 V		17	32		48		40	
			6 V		14	27		41		34	
	RCLK	Q <sub>A</sub> -Q <sub>H</sub>	2 V		50	150		225		187	
			4.5 V		17	30		45		37	
			6 V		14	26		38		32	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H'</sub>	2 V		51	175		261		219	ns
			4.5 V		18	35		52		44	
			6 V		15	30		44		37	
t <sub>en</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> -Q <sub>H</sub>	2 V		40	150		225		187	ns
			4.5 V		15	30		45		37	
			6 V		13	26		38		32	
t <sub>dis</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> -Q <sub>H</sub>	2 V		42	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		20	34		51		43	
t <sub>t</sub>		Q <sub>A</sub> -Q <sub>H</sub>	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	
		Q <sub>H'</sub>	2 V		28	75		110		95	
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)

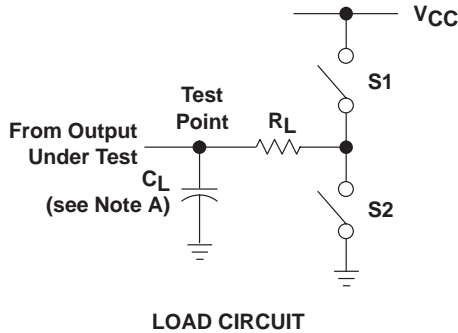
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC595		SN74HC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	RCLK	Q <sub>A</sub> -Q <sub>H</sub>	2 V		60	200		300		250	ns
			4.5 V		22	40		60		50	
			6 V		19	34		51		43	
t <sub>en</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> -Q <sub>H</sub>	2 V		70	200		298		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t <sub>t</sub>		Q <sub>A</sub> -Q <sub>H</sub>	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T<sub>A</sub> = 25°C

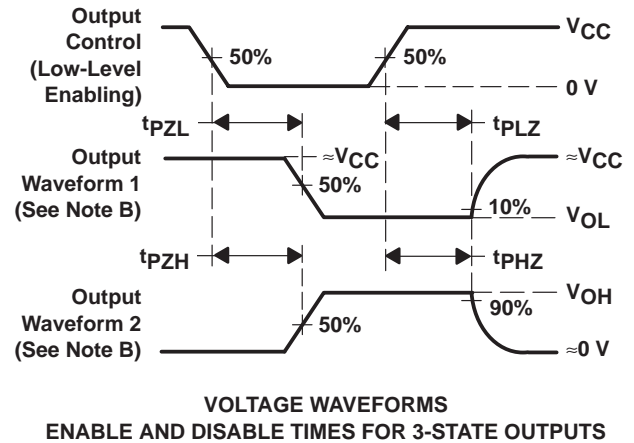
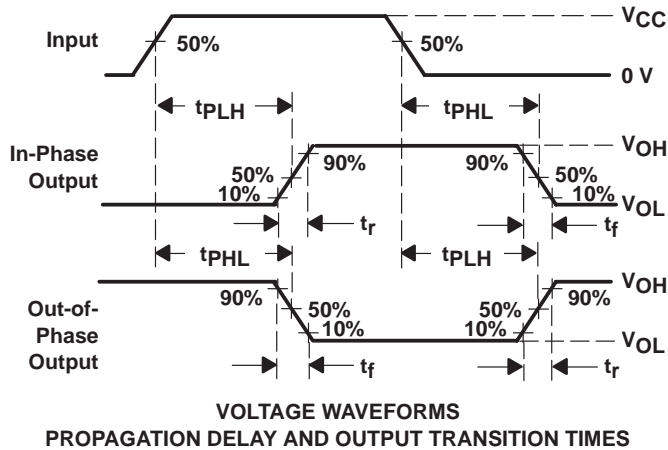
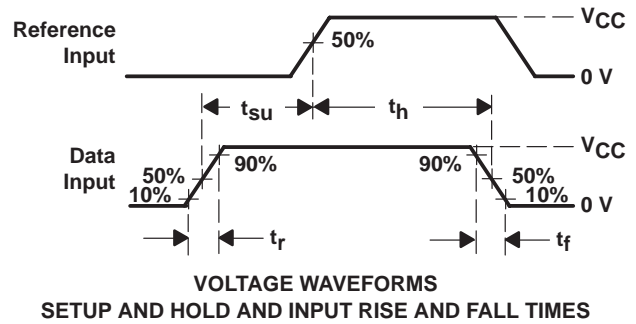
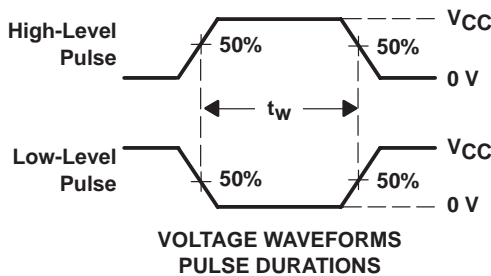
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	400	pF



PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.  
 E. The outputs are measured one at a time, with one input transition per measurement.  
 F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

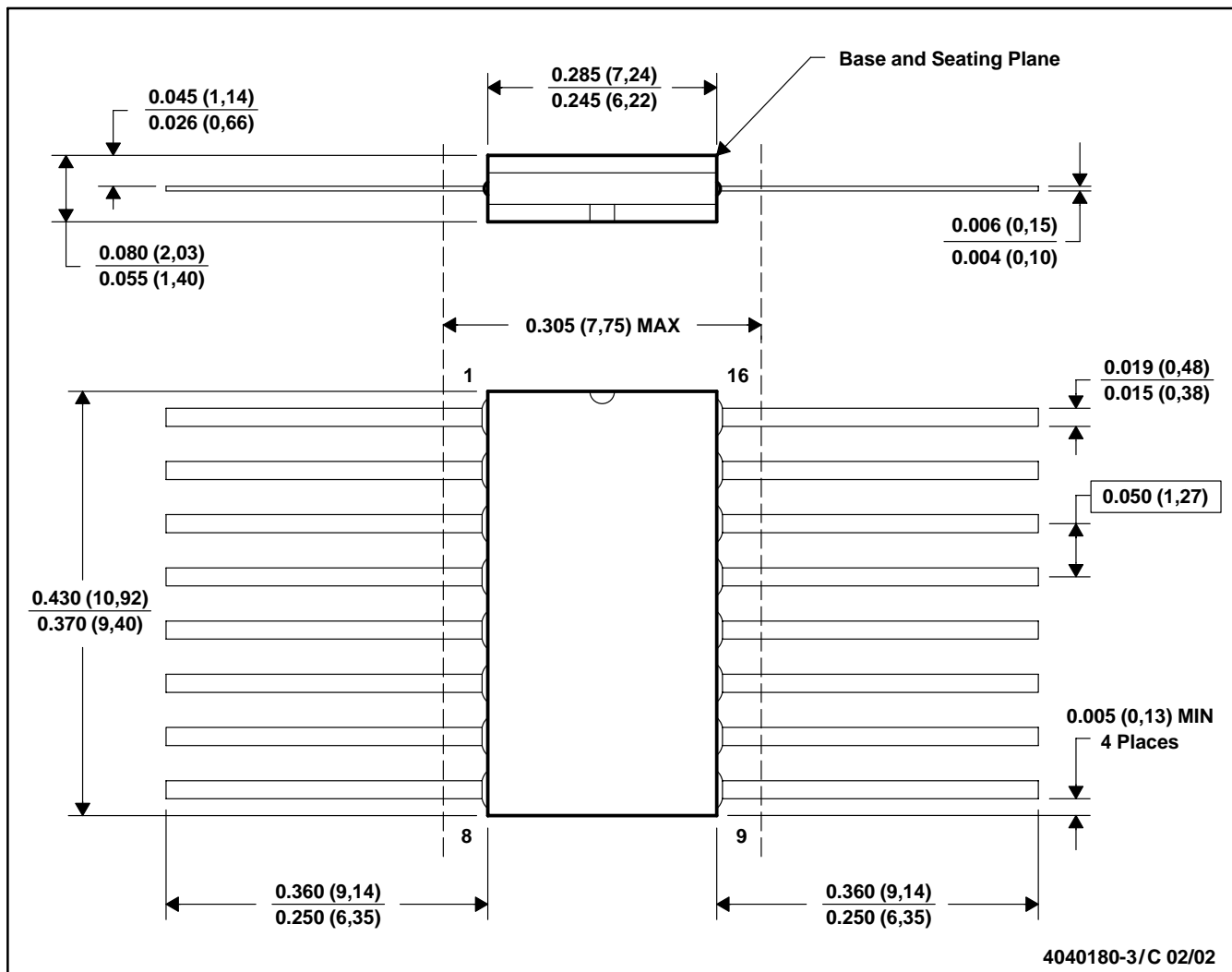


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835 GDFP-1F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

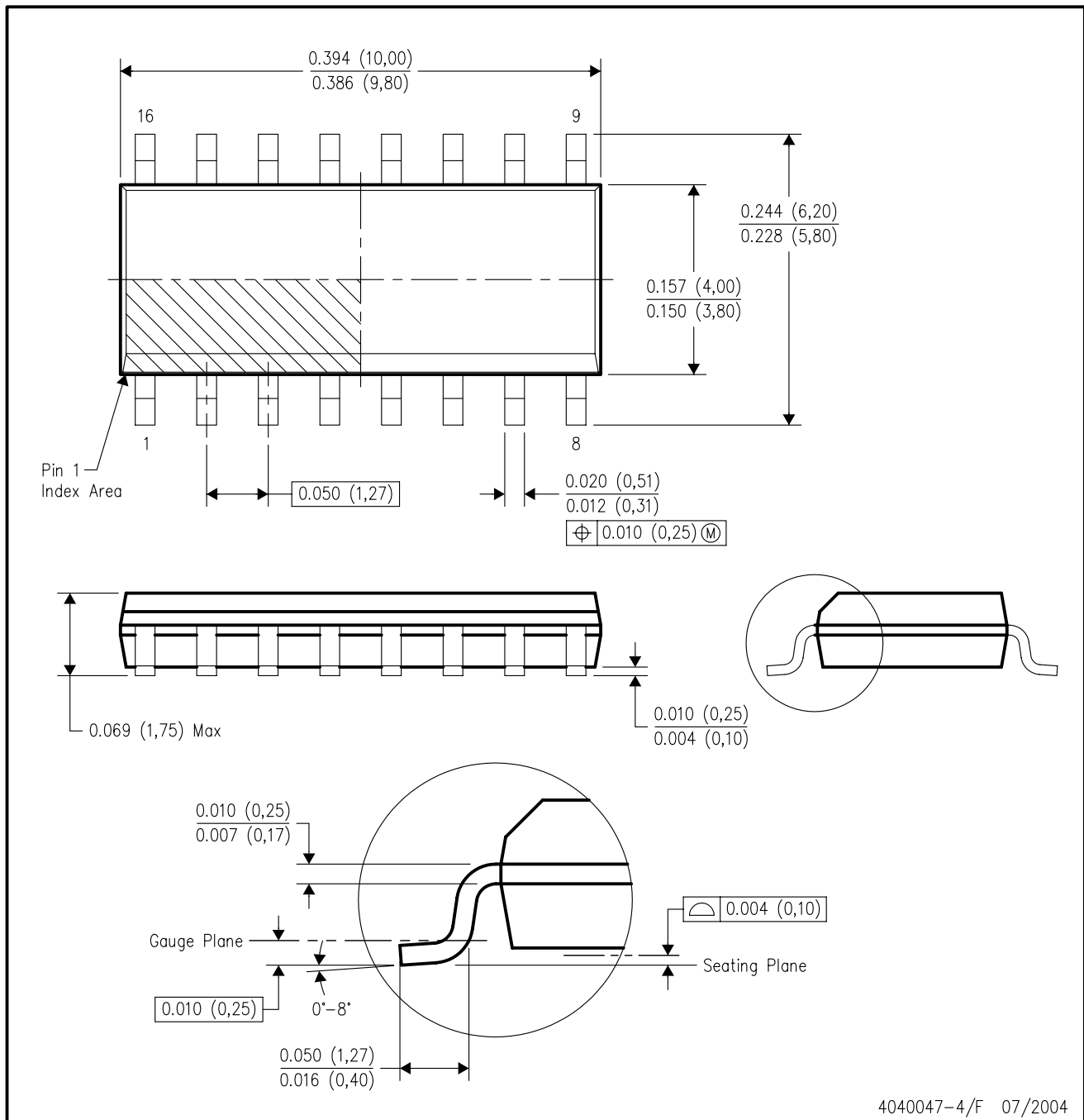
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

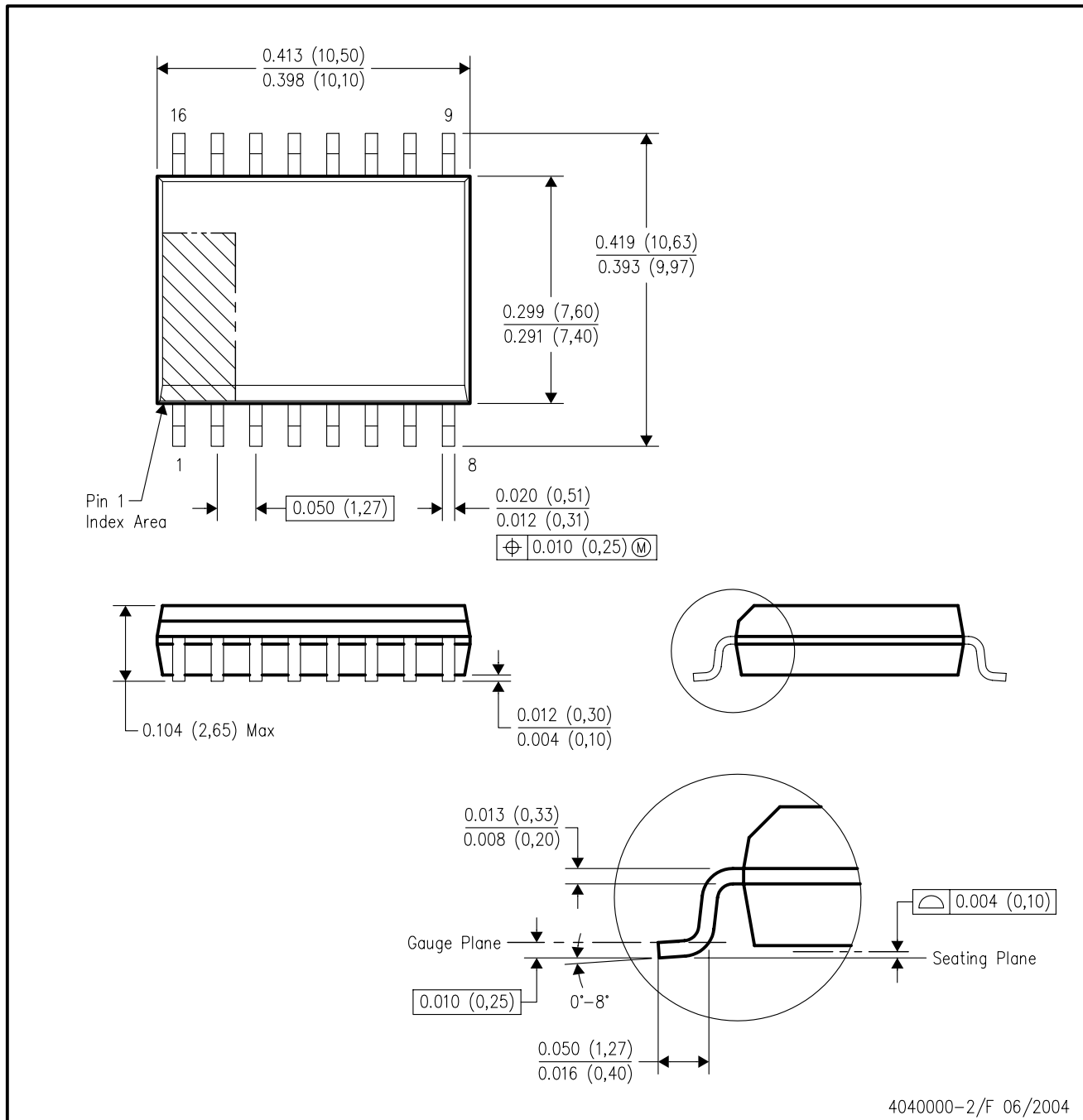
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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