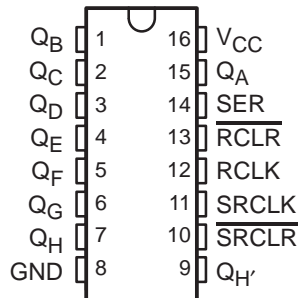


SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

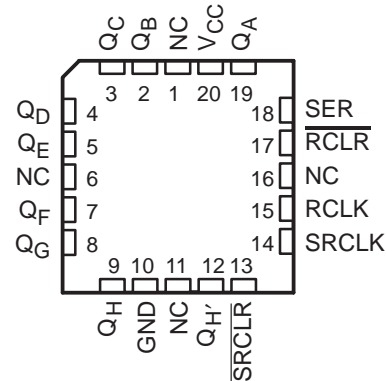
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- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 15$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers

SN54HC594 . . . J OR W PACKAGE
SN74HC594 . . . D, DW, OR N PACKAGE
(TOP VIEW)



SN54HC594 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (\overline{RCLR} , \overline{SRCLR}) inputs are provided on both the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

The parallel (Q_A – Q_H) outputs have high-current capability. $Q_{H'}$ is a standard output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC594N	SN74HC594N
		Tube of 40	SN74HC594D	HC594
	SOIC – D	Reel of 2500	SN74HC594DR	
		Reel of 250	SN74HC594DT	
	SOIC – DW	Tube of 40	SN74HC594DW	
		Reel of 2000	SN74HC594DWR	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC594J	SNJ54HC594J
	CFP – W	Tube of 150	SNJ54HC594W	SNJ54HC594W
	LCCC – FK	Tube of 55	SNJ54HC594FK	SNJ54HC594FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54HC594, SN74HC594
8-BIT SHIFT REGISTERS
WITH OUTPUT REGISTERS

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FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

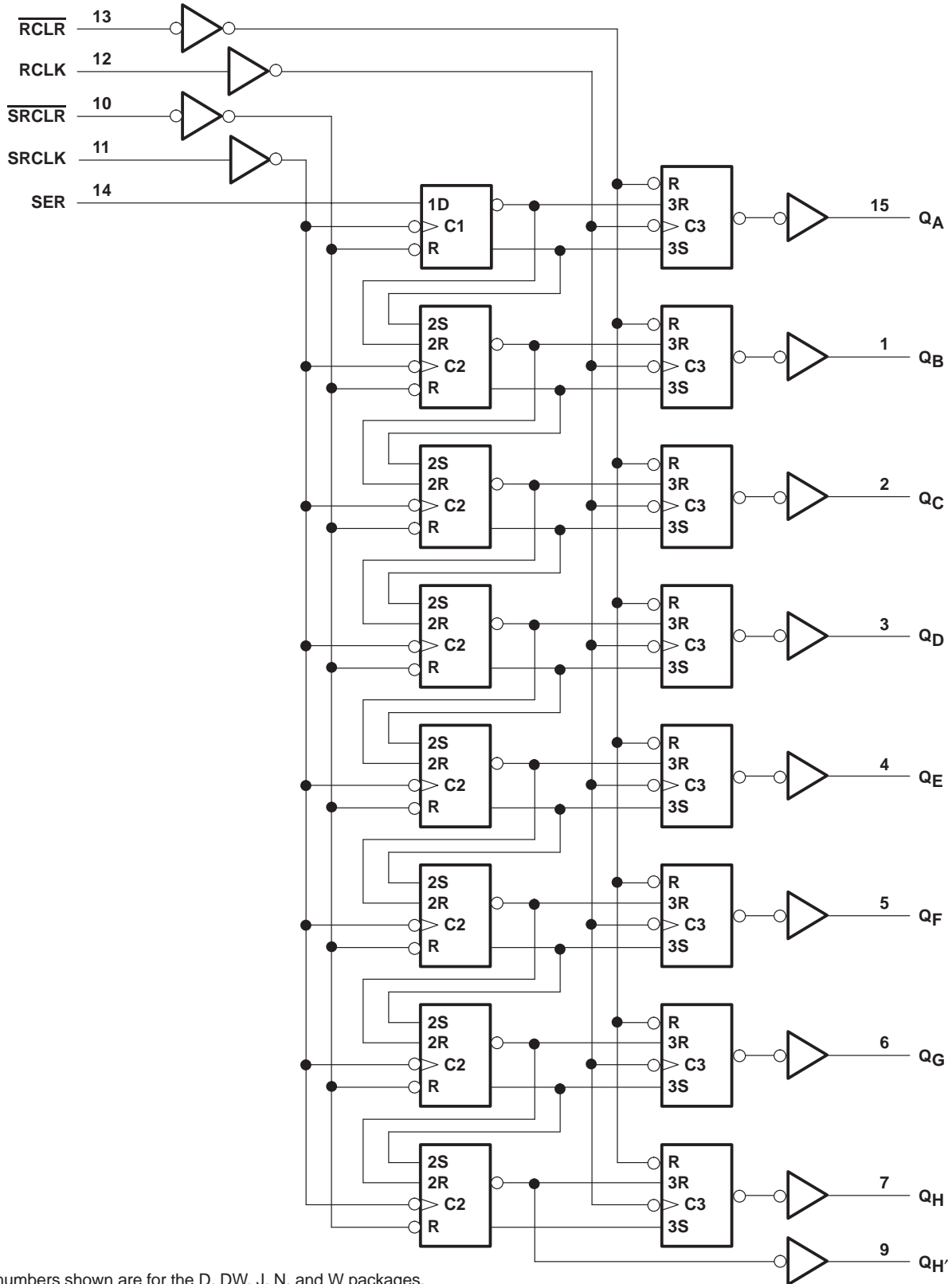


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logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.

SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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recommended operating conditions (see Note 3)

		SN54HC594			SN74HC594			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5		V	
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 6 V			1.8			
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V		1000		1000		ns
		V _{CC} = 4.5 V		500		500		
		V _{CC} = 6 V		400		400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		4.5 V	Q _H ', I _{OH} = -4 mA	3.98	4.3		3.7		3.84		
			Q _A -Q _H , I _{OH} = -6 mA	3.98	4.3		3.7		3.84		
			Q _H ', I _{OH} = -5.2 mA	5.48	5.8		5.2		5.34		
6 V	Q _A -Q _H , I _{OH} = -7.8 mA	5.48	5.8		5.2		5.34				
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		4.5 V	Q _H ', I _{OL} = 4 mA		0.17	0.26		0.4		0.33	
			Q _A -Q _H , I _{OL} = 6 mA		0.17	0.26		0.4		0.33	
			Q _H ', I _{OL} = 5.2 mA		0.15	0.26		0.4		0.33	
6 V	Q _A -Q _H , I _{OL} = 7.8 mA		0.15	0.26		0.4		0.33			
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	μA
C _i			2 V to 6 V		3	10		10		10	pF

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SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC594		SN74HC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	5		3.3		4		MHz
		4.5 V	25		17		20		
		6 V	29		20		24		
t _w	SRCLK or RCLK high or low	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	SRCLR or RCLR low	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
t _{su}	SER before SRCLK↑	2 V	90		135		110		ns
		4.5 V	18		27		22		
		6 V	15		23		19		
	SRCLK↑ before RCLK↑†	2 V	90		135		110		
		4.5 V	18		27		22		
		6 V	15		23		19		
	SRCLR low before RCLK↑	2 V	50		75		63		
		4.5 V	10		15		13		
		6 V	9		13		11		
	SRCLR high (inactive) before SRCLK↑	2 V	20		20		20		
		4.5 V	10		10		10		
		6 V	10		10		10		
	RCLR high (inactive) before SRCLK↑	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		
t _h	Hold time, SER after SRCLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

† This setup time ensures that the output register receives stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5	8		3.3		4	MHz	
			4.5 V	25	35		17		20		
			6 V	29	40		20		24		
t_{pd}	SRCLK	Q_H'	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	RCLK	Q_A-Q_H	2 V		50	150		225		185	
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
t_{PHL}	$\overline{\text{SRCLK}}$	Q_H'	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	$\overline{\text{RCLK}}$	Q_A-Q_H	2 V		50	125		185		155	
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
t_t		Q_H'	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
		Q_A-Q_H	2 V		38	60		90		75	
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	RCLK	Q_A-Q_H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_{PHL}	$\overline{\text{RCLK}}$	Q_A-Q_H	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
t_t		Q_A-Q_H	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	395	pF

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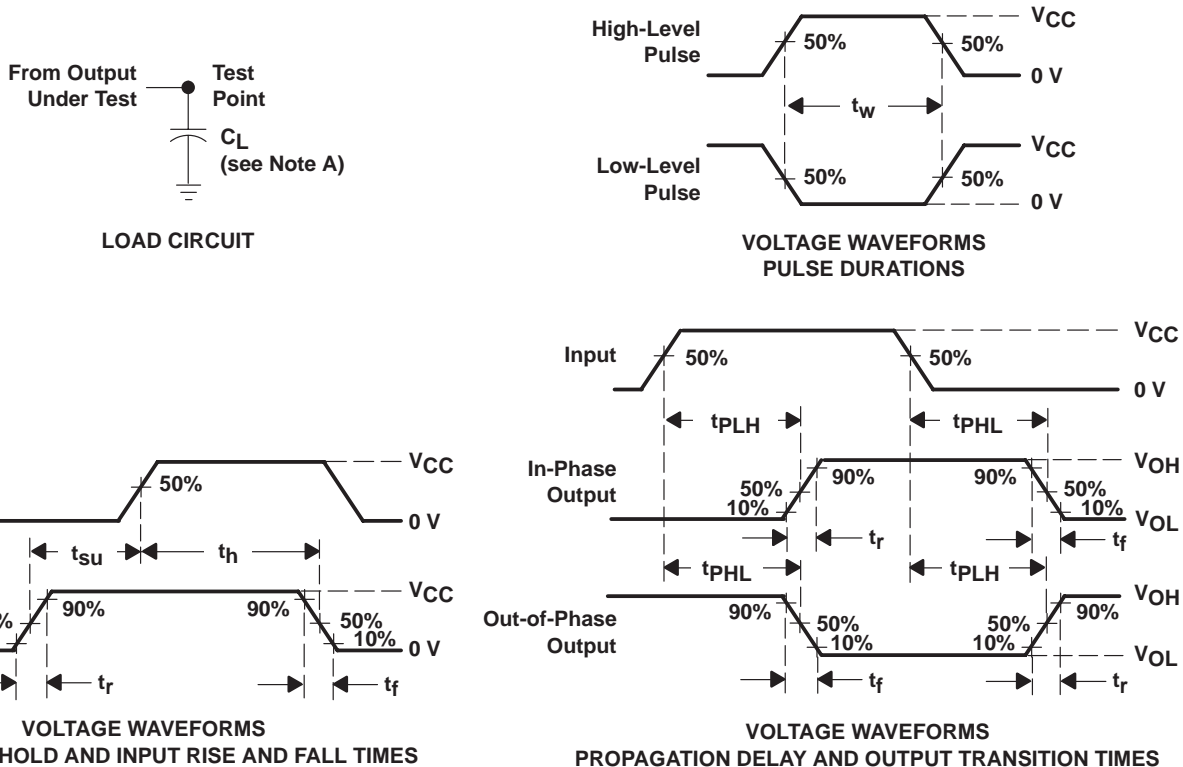


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SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - F. t_f and t_r are the same as t_t .

Figure 1. Load Circuit and Voltage Waveforms

D (R-PDSO-G16)

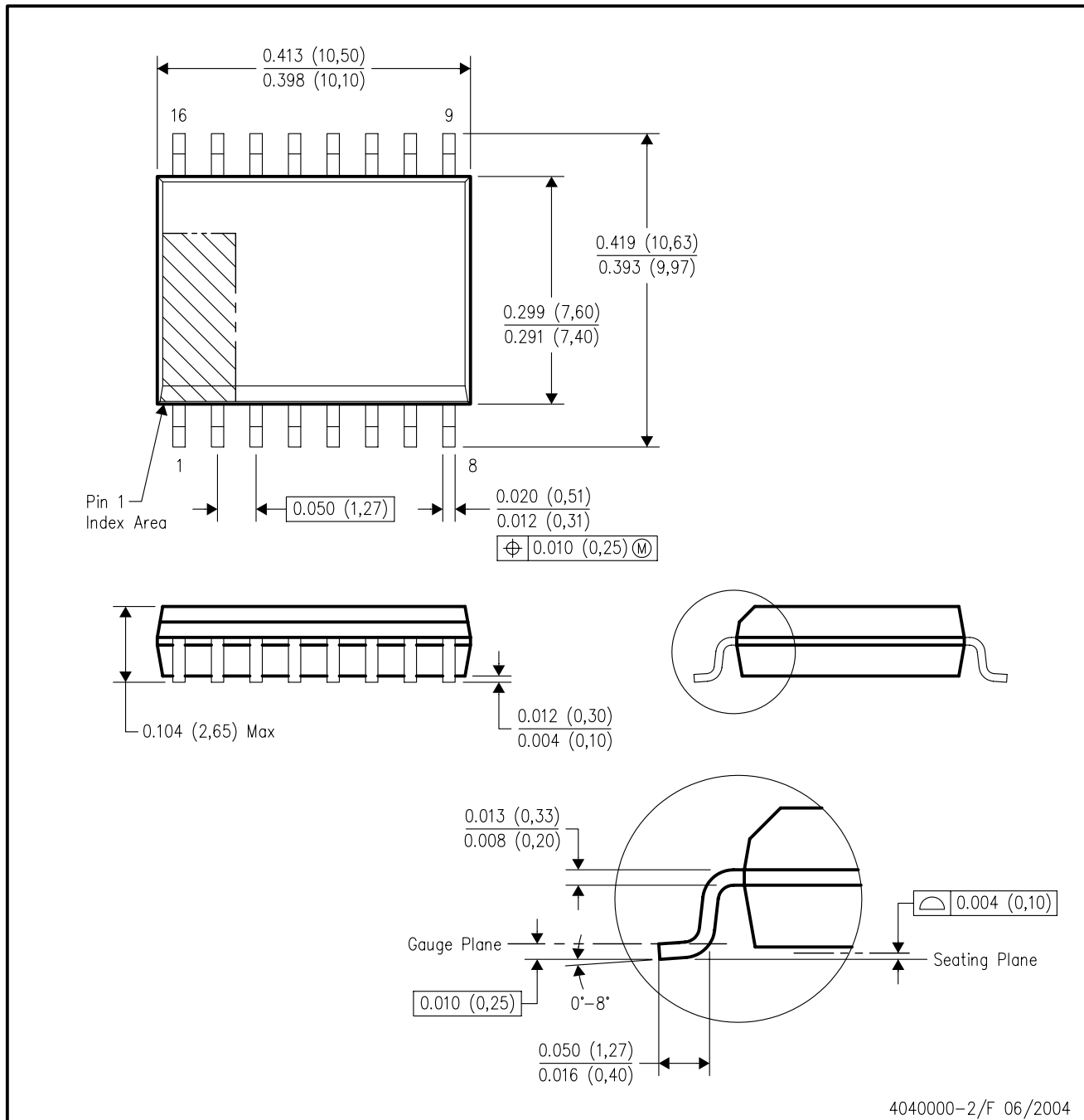
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

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