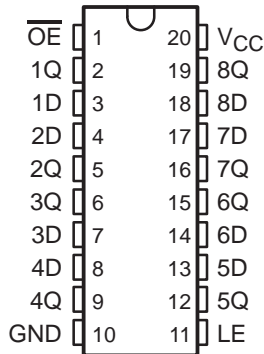


SN54HC373, SN74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

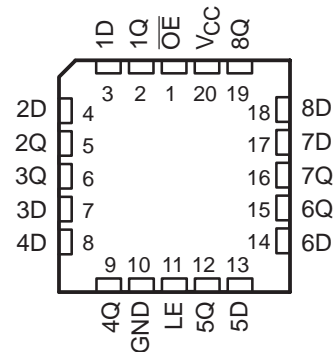
SCLS140D – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Eight High-Current Latches in a Single Package
- Full Parallel Access for Loading

SN54HC373 . . . J OR W PACKAGE
SN74HC373 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC373 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HC373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74HC373N	SN74HC373N
	SOIC – DW	Tube of 25	SN74HC373DW	HC373
		Reel of 2000	SN74HC373DWR	
	SOP – NS	Reel of 2000	SN74HC373NSR	HC373
	SSOP – DB	Reel of 2000	SN74HC373DBR	HC373
	TSSOP – PW	Tube of 70	SN74HC373PW	HC373
Reel of 2000		SN74HC373PWR		
Reel of 250		SN74HC373PWT		
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54HC373J	SNJ54HC373J
	CFP – W	Tube of 85	SNJ54HC373W	SNJ54HC373W
	LCCC – FK	Tube of 55	SNJ54HC373FK	SNJ54HC373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC373, SN74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS140D – DECEMBER 1982 – REVISED AUGUST 2003

description/ordering information (continued)

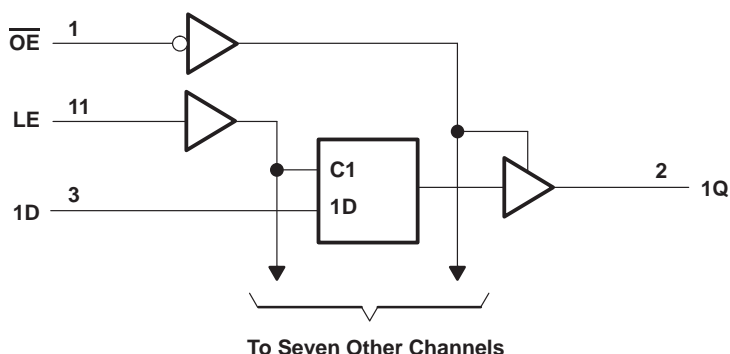
An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC373, SN74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS140D – DECEMBER 1982 – REVISED AUGUST 2003

recommended operating conditions (see Note 3)

		SN54HC373			SN74HC373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5		0.5	V
		V _{CC} = 4.5 V			1.35		1.35	
		V _{CC} = 6 V			1.8		1.8	
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V			1000		1000	ns
		V _{CC} = 4.5 V			500		500	
		V _{CC} = 6 V			400		400	
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	μA
C _i			2 V to 6 V		3	10		10		10	pF



SN54HC373, SN74HC373
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCLS140D – DECEMBER 1982 – REVISED AUGUST 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V_{CC}	$T_A = 25^\circ\text{C}$		SN54HC373		SN74HC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, LE high	2 V	80	120	100				ns
	4.5 V	16	24	20				
	6 V	14	20	17				
t_{su} Setup time, data before LE↓	2 V	50	75	63				ns
	4.5 V	10	15	13				
	6 V	9	13	11				
t_h Hold time, data after LE↓	2 V	20	26	24				ns
	4.5 V	10	13	12				
	6 V	10	13	12				

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		58	150	225	190			ns
			4.5 V		15	30	45	38			
			6 V		13	26	38	32			
	LE	Any Q	2 V		73	175	265	220			
			4.5 V		18	35	53	44			
			6 V		15	30	45	38			
t_{en}	\overline{OE}	Any Q	2 V		65	150	225	190			ns
			4.5 V		17	30	45	38			
			6 V		14	26	38	32			
t_{dis}	\overline{OE}	Any Q	2 V		50	150	225	190			ns
			4.5 V		15	30	45	38			
			6 V		13	26	38	32			
t_t		Any Q	2 V		28	60	90	75			ns
			4.5 V		8	12	18	15			
			6 V		6	10	15	13			



SN54HC373, SN74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS140D – DECEMBER 1982 – REVISED AUGUST 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V	82	200		300		250	ns	
			4.5 V	22	40		60		50		
			6 V	19	34		51		43		
	LE	Any Q	2 V	100	225		335		285		
			4.5 V	24	45		67		57		
			6 V	20	38		57		48		
t_{en}	\overline{OE}	Any Q	2 V	90	200		300		250	ns	
			4.5 V	23	40		60		50		
			6 V	19	34		51		43		
t_t		Any Q	2 V	45	210		315		265	ns	
			4.5 V	17	42		63		53		
			6 V	13	36		53		45		

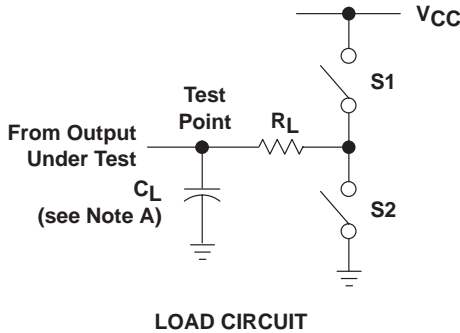
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	No load	100	pF

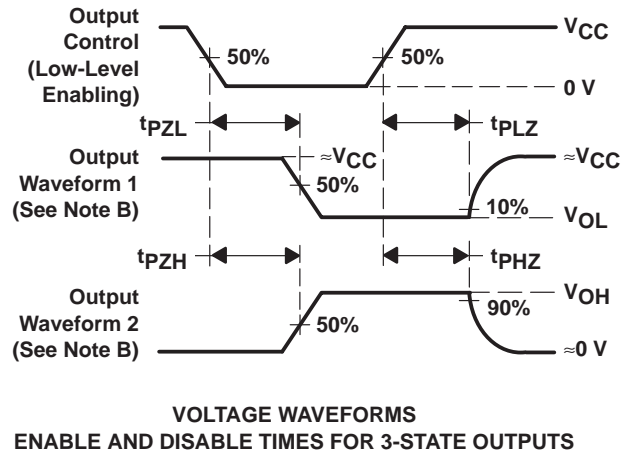
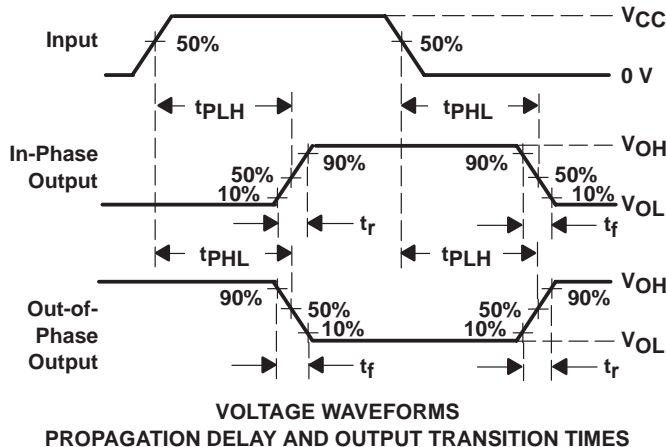
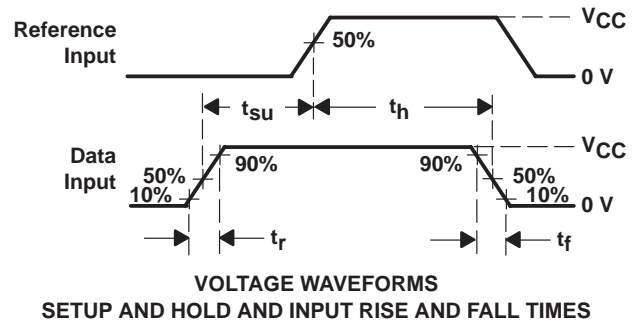
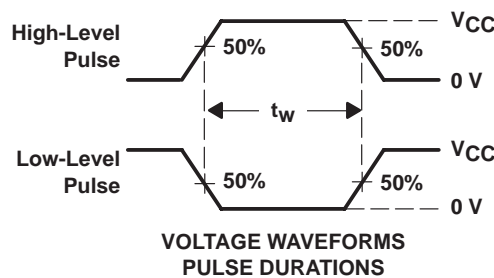
SN54HC373, SN74HC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS140D – DECEMBER 1982 – REVISED AUGUST 2003

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	--	50 pF or 150 pF	Open	Open



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms