

# SN54HC251, SN74HC251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SCLS132E – DECEMBER 1982 – REVISED SEPTEMBER 2003

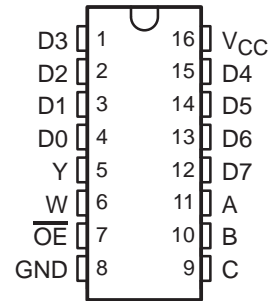
- 3-State Version of 'HC151
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 9$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data

## description/ordering information

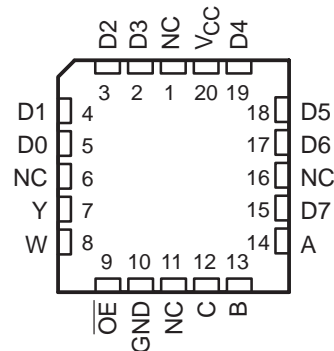
These data selectors/multiplexers contain full binary decoding to select 1-of-8 data sources and feature strobe-controlled complementary 3-state outputs.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Both outputs are controlled by the output-enable ( $\overline{OE}$ ) input. The outputs are disabled when  $\overline{OE}$  is high.

SN54HC251 . . . J OR W PACKAGE  
SN74HC251 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC251 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC251N	SN74HC251N
	SOIC – D	Tube of 40	SN74HC251D	HC251
		Reel of 2500	SN74HC251DR	
		Reel of 250	SN74HC251DT	
	SOP – NS	Reel of 2000	SN74HC251NSR	HC251
	SSOP – DB	Reel of 2000	SN74HC251DBR	HC251
-55°C to 125°C	TSSOP – PW	Tube of 90	SN74HC251PW	HC251
		Reel of 2000	SN74HC251PWR	
		Reel of 250	SN74HC251PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC251J	SNJ54HC251J
	CFP – W	Tube of 150	SNJ54HC251W	SNJ54HC251W
	LCCC – FK	Tube of 55	SNJ54HC251FK	SNJ54HC251FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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**SN54HC251, SN74HC251**  
**DATA SELECTORS/MULTIPLEXERS**  
**WITH 3-STATE OUTPUTS**

SCLS132E – DECEMBER 1982 – REVISED SEPTEMBER 2003

FUNCTION TABLE

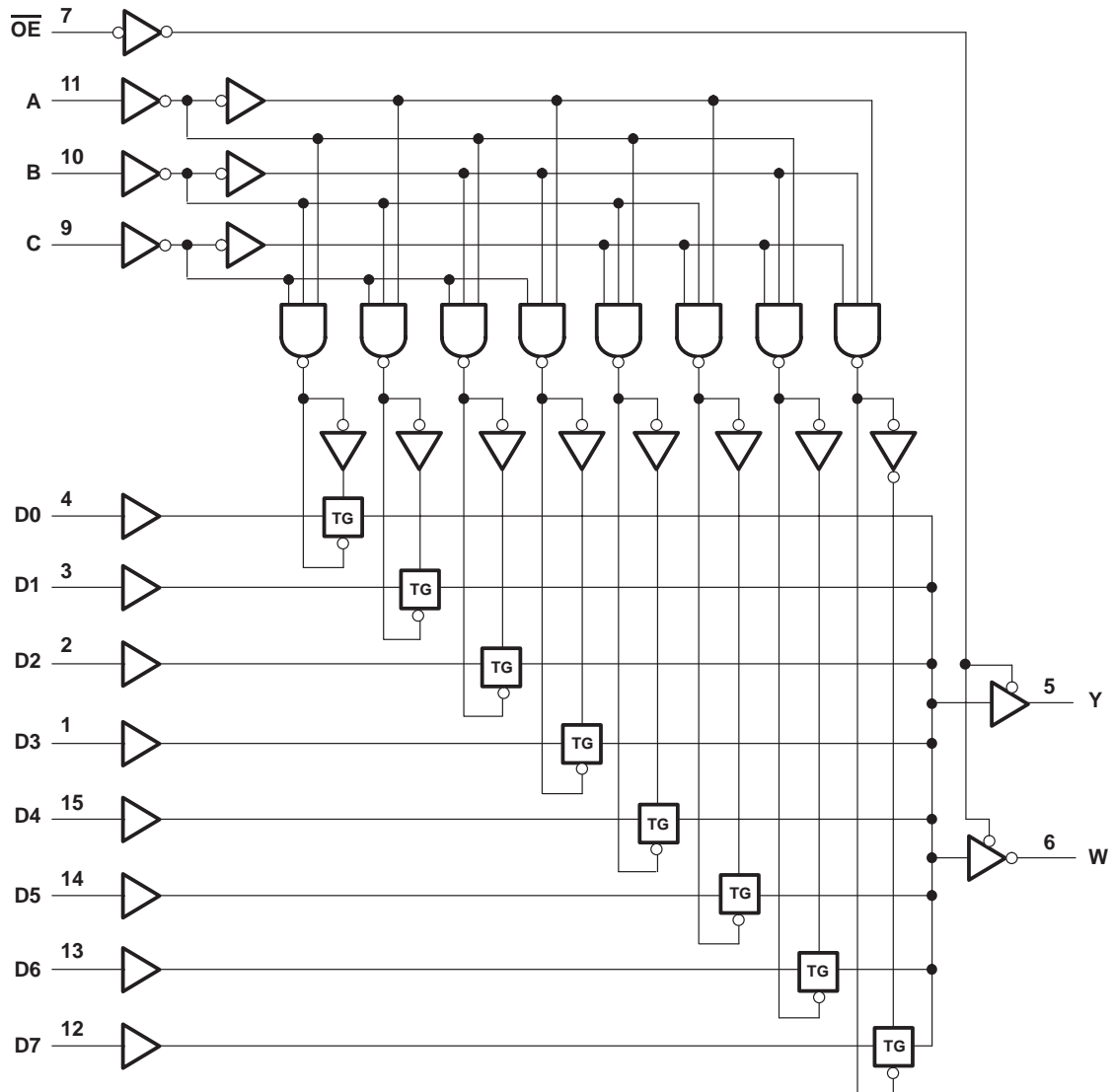
INPUTS				OUTPUTS	
SELECT			$\overline{\text{OE}}$	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{\text{D0}}$
L	L	H	L	D1	$\overline{\text{D1}}$
L	H	L	L	D2	$\overline{\text{D2}}$
L	H	H	L	D3	$\overline{\text{D3}}$
H	L	L	L	D4	$\overline{\text{D4}}$
H	L	H	L	D5	$\overline{\text{D5}}$
H	H	L	L	D6	$\overline{\text{D6}}$
H	H	H	L	D7	$\overline{\text{D7}}$

D0, D1 . . . D7 = the level of the respective D input

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SCLS132E - DECEMBER 1982 - REVISED SEPTEMBER 2003

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

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SCLS132E – DECEMBER 1982 – REVISED SEPTEMBER 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±35 mA
Continuous current through $V_{CC}$ or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54HC251			SN74HC251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5	1.5		V	
		$V_{CC} = 4.5\text{ V}$		3.15	3.15			
		$V_{CC} = 6\text{ V}$		4.2	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$			0.5	0.5	V	
		$V_{CC} = 4.5\text{ V}$			1.35	1.35		
		$V_{CC} = 6\text{ V}$			1.8	1.8		
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$			1000	1000	ns	
		$V_{CC} = 4.5\text{ V}$			500	500		
		$V_{CC} = 6\text{ V}$			400	400		
$T_A$	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SCLS132E – DECEMBER 1982 – REVISED SEPTEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		6 V		±0.01	±0.5		±10		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	W or Y	2 V		58	205		300		256	ns
			4.5 V		21	41		60		51	
			6 V		19	35		51		44	
	Any D	W or Y	2 V		44	195		283		244	
			4.5 V		17	39		57		49	
			6 V		15	33		48		41	
t <sub>en</sub>	$\overline{\text{OE}}$	W or Y	2 V		30	145		210		181	ns
			4.5 V		10	29		42		36	
			6 V		9	25		36		31	
t <sub>dis</sub>	$\overline{\text{OE}}$	W or Y	2 V		25	195		283		244	ns
			4.5 V		15	39		57		49	
			6 V		14	33		48		41	
t <sub>t</sub>		W or Y	2 V		20	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	



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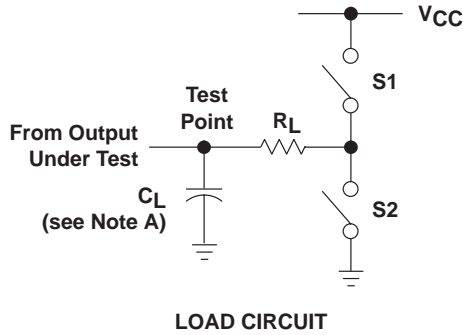
switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$   
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	W or Y	2 V		72	300		450		375	ns
			4.5 V		25	60		90		75	
			6 V		22	52		77		65	
	Any D	W or Y	2 V		59	300		450		375	
			4.5 V		21	60		90		75	
			6 V		18	52		77		65	
$t_{en}$	$\overline{OE}$	W or Y	2 V		50	230		340		285	ns
			4.5 V		17	46		68		57	
			6 V		15	40		58		50	
$t_t$		W or Y	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

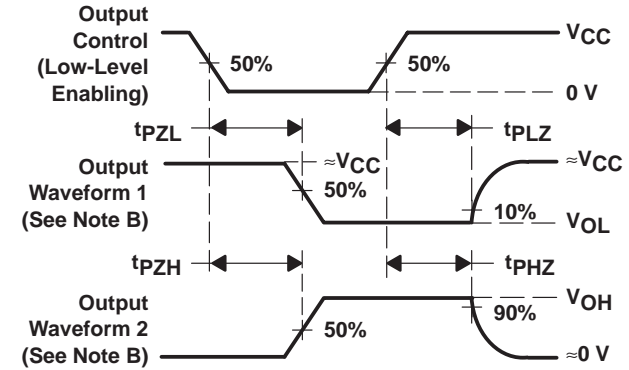
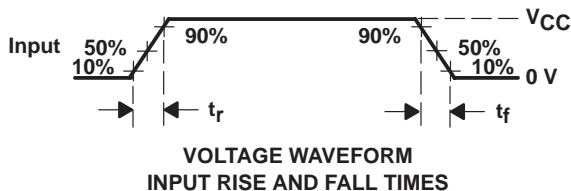
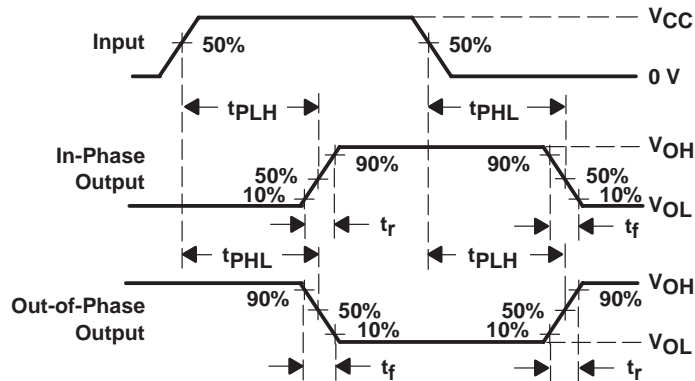
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	70	pF

PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{PZH}$	1 k $\Omega$ 50 pF or 150 pF	Open	Closed
	$t_{PZL}$		Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$ 50 pF	Open	Closed
	$t_{PLZ}$		Closed	Open
$t_{pd}$ or $t_t$	--	50 pF or 150 pF	Open	Open



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Post Office Box 655303 Dallas, Texas 75265