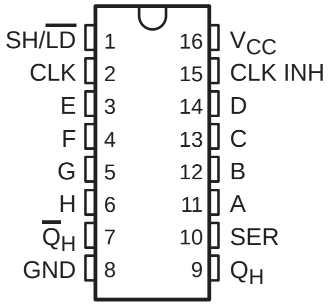
SN54HC165, SN74HC165
8-BIT PARALLEL-LOAD SHIFT REGISTERS

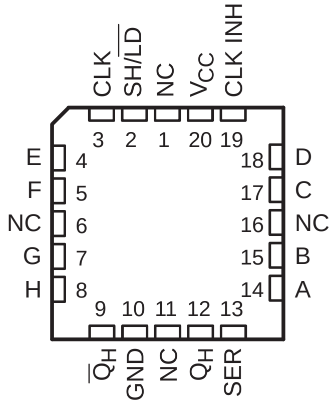
SCLS116E − DECEMBER 1982 − REVISED SEPTEMBER 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-µA Max I_{CC}**
- **Typical t_{pd} = 13 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 µA Max**
- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**

SN54HC165 . . . J OR W PACKAGE
SN74HC165 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC165 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The ’HC165 devices are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A−H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The ’HC165 devices also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74HC165N	SN74HC165N
	SOIC − D	Tube of 40	SN74HC165D	HC165
		Reel of 2500	SN74HC165DR	
		Reel of 250	SN74HC165DT	
	SOP − NS	Reel of 2000	SN74HC165NSR	HC165
	SSOP − DB	Reel of 2000	SN74HC165DBR	HC165
	TSSOP − PW	Tube of 90	SN74HC165PW	HC165
		Reel of 2000	SN74HC165PWR	
		Reel of 250	SN74HC165PWT	
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54HC165J	SNJ54HC165J
	CFP − W	Tube of 150	SNJ54HC165W	SNJ54HC165W
	LCCC − FK	Tube of 55	SNJ54HC165FK	SNJ54HC165FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}		−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)		±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	D package	73°C/W
	DB package	82°C/W
	N package	67°C/W
	NS package	64°C/W
	PW package	108°C/W
Storage temperature range, T_{stg}		−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC165			SN74HC165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$[‡]	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

[‡] If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = −20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = −5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160		80	µA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC165		SN74HC165		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V		36		25		29	
t_w	Pulse duration	SH/$\overline{\mathrm{LD}}$ low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	SH/$\overline{\mathrm{LD}}$ high before CLK↑	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		SER before CLK↑	2 V	40		60		50		
			4.5 V	8		12		10		
			6 V	7		10		9		
		CLK INH low before CLK↑	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK INH high before CLK↑	2 V	40		60		50		
			4.5 V	8		12		10		
			6 V	7		10		9		
		Data before SH/$\overline{\mathrm{LD}}$↓	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time	SER data after CLK↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		PAR data after SH/$\overline{\mathrm{LD}}$↓	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	13		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	62		25		29		
t_{pd}	SH/$\overline{LD}$	Q_H or $\overline{Q}_H$	2 V		80	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		16	26		38		32	
	CLK	Q_H or $\overline{Q}_H$	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	H	Q_H or $\overline{Q}_H$	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	75	pF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
84095012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
8409501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
8409501FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54HC165J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74HC165D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC165DBR	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC165DBRE4	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC165DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC165DT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC165N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HC165N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74HC165NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74HC165PW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC165PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
SN74HC165PWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC165PWT	ACTIVE	TSSOP	PW	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74HC165PWTE4	ACTIVE	TSSOP	PW	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SNJ54HC165FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54HC165J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54HC165W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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