



## SNx4HC00 Quadruple 2-Input Positive-NAND Gates

### 1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption:  $I_{CC}$  20- $\mu$ A (Maximum)
- Typical  $t_{pd}$ : 8 ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current: 1  $\mu$ A (Maximum)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-ray Players and Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom or Server AC/DC Supply (Single Controller: Analog and Digital)
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

### 3 Description

The SN54HC00 and SN74HC00 devices contain four independent, 2-input NAND gates. They perform the Boolean function  $Y = \overline{A \times B}$  or  $Y = \overline{A + B}$  in positive logic.

**Device Information<sup>(1)</sup>**

| PART NUMBER | PACKAGE (PINS) | BODY SIZE (NOM)           |
|-------------|----------------|---------------------------|
| SN54HC00    | CDIP (14)      | 6.92 mm $\times$ 19.94 mm |
|             | CFP (14)       | 6.20 mm $\times$ 9.41 mm  |
|             | LCCC (20)      | 8.89 mm $\times$ 8.89 mm  |
| SN74HC00D   | SOIC (14)      | 8.65 mm $\times$ 3.91 mm  |
| SN74HC00DB  | SSOP (14)      | 6.20 mm $\times$ 5.30 mm  |
| SN74HC00N   | PDIP (14)      | 19.30 mm $\times$ 6.35 mm |
| SN74HC00NS  | SOP (14)       | 10.30 mm $\times$ 5.30 mm |
| SN74HC00PW  | TSSOP (14)     | 5.00 mm $\times$ 4.40 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Logic Diagram (Positive Logic)



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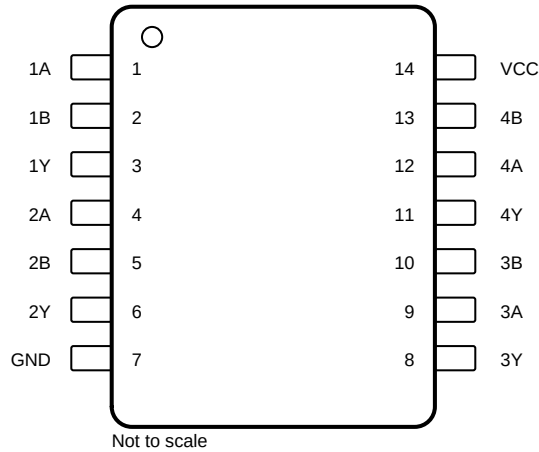
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

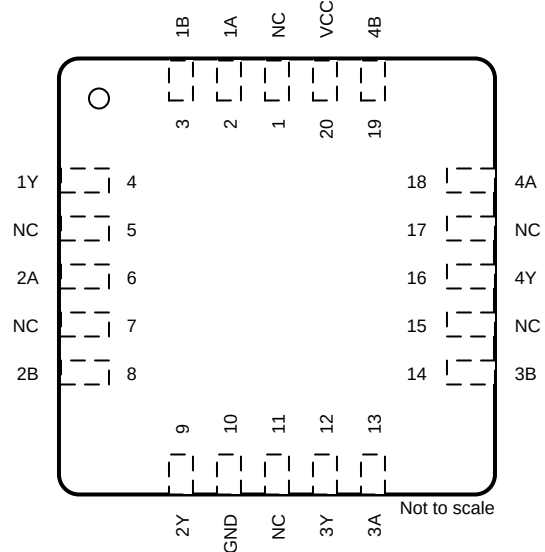
| Changes from Revision E (August 2003) to Revision F                                                                                                                                                                                                                                                                                                                                                                                                        | Page     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| • Added <i>Applications</i> section, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>1</b> |
| • Added Military Disclaimer to Features list .....                                                                                                                                                                                                                                                                                                                                                                                                         | <b>1</b> |
| • Removed <i>Ordering Information</i> table; see POA at the end of data sheet.....                                                                                                                                                                                                                                                                                                                                                                         | <b>1</b> |
| • Changed values in the <i>Thermal Information</i> table to align with JEDEC standards.....                                                                                                                                                                                                                                                                                                                                                                | <b>5</b> |
| • Deleted <i>Operating Characteristics</i> table; moved Cpd row to <i>Electrical Characteristics</i> .....                                                                                                                                                                                                                                                                                                                                                 | <b>5</b> |

## 5 Pin Configuration and Functions

**D, DB, J, N, NS, PW, and W Package**  
**14-Pin SOIC, SSOP, CDIP, PDIP, SOP, TSSOP, and CFP**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**



### Pin Functions

| NAME            | PIN                                           |                        | I/O | DESCRIPTION            |
|-----------------|-----------------------------------------------|------------------------|-----|------------------------|
|                 | SOIC, SSOP,<br>CDIP, PDIP, SOP,<br>TSSOP, CFP | LCCC                   |     |                        |
| 1A              | 1                                             | 2                      | I   | Gate 1 input           |
| 1B              | 2                                             | 3                      | I   | Gate 1 input           |
| 1Y              | 3                                             | 4                      | O   | Gate 1 output          |
| 2A              | 4                                             | 6                      | I   | Gate 2 input           |
| 2B              | 5                                             | 8                      | I   | Gate 2 input           |
| 2Y              | 6                                             | 9                      | O   | Gate 2 output          |
| 3A              | 9                                             | 13                     | I   | Gate 3 input           |
| 3B              | 10                                            | 14                     | I   | Gate 3 input           |
| 3Y              | 8                                             | 12                     | O   | Gate 3 output          |
| 4A              | 12                                            | 18                     | I   | Gate 4 input           |
| 4B              | 13                                            | 19                     | I   | Gate 4 input           |
| 4Y              | 11                                            | 16                     | O   | Gate 4 output          |
| GND             | 7                                             | 10                     | —   | Ground pin             |
| NC              | —                                             | 1, 5, 7,<br>11, 15, 17 | —   | No internal connection |
| V <sub>CC</sub> | 14                                            | 20                     | —   | Power pin              |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                                               | MIN  | MAX | UNIT |
|-------------------------------------------------------------------------------|------|-----|------|
| Supply voltage, $V_{CC}$                                                      | –0.5 | 7   | V    |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) <sup>(2)</sup>  |      | ±20 | mA   |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) <sup>(2)</sup> |      | ±20 | mA   |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                    |      | ±25 | mA   |
| Continuous current through $V_{CC}$ or GND                                    |      | ±50 | mA   |
| Storage temperature, $T_{stg}$                                                | –65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                     |                                     | MIN              | NOM  | MAX      | UNIT |
|---------------------|-------------------------------------|------------------|------|----------|------|
| $V_{CC}$            | Supply voltage                      | 2                | 5    | 6        | V    |
| $V_{IH}$            | High-level input voltage            | $V_{CC} = 2$ V   | 1.5  |          | V    |
|                     |                                     | $V_{CC} = 4.5$ V | 3.15 |          |      |
|                     |                                     | $V_{CC} = 6$ V   | 4.2  |          |      |
| $V_{IL}$            | Low-level input voltage             | $V_{CC} = 2$ V   |      | 0.5      | V    |
|                     |                                     | $V_{CC} = 4.5$ V |      | 1.35     |      |
|                     |                                     | $V_{CC} = 6$ V   |      | 1.8      |      |
| $V_I$               | Input voltage                       | 0                |      | $V_{CC}$ | V    |
| $V_O$               | Output voltage                      | 0                |      | $V_{CC}$ | V    |
| $\Delta t/\Delta v$ | Input transition rise and fall time | $V_{CC} = 2$ V   |      | 1000     | ns   |
|                     |                                     | $V_{CC} = 4.5$ V |      | 500      |      |
|                     |                                     | $V_{CC} = 6$ V   |      | 400      |      |
| $T_A$               | Operating free-air temperature      | SN54HC00         | –55  | 125      | °C   |
|                     |                                     | SN74HC00         | –40  | 85       |      |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to [Implications of Slow or Floating CMOS Inputs](#) application report.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74HC00 |           |          |          |            | UNIT |
|-------------------------------|----------------------------------------------|----------|-----------|----------|----------|------------|------|
|                               |                                              | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SOP) | PW (TSSOP) |      |
|                               |                                              | 14 PINS  | 14 PINS   | 14 PINS  | 14 PINS  | 14 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 94.7     | 108.3     | 57.5     | 91       | 122.9      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 54.6     | 60.3      | 45.1     | 48.8     | 51.5       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 49       | 55.7      | 37.3     | 49.8     | 64.6       | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 21.1     | 25        | 30.3     | 18.4     | 6.6        | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 48.7     | 55.2      | 37.2     | 49.5     | 64         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

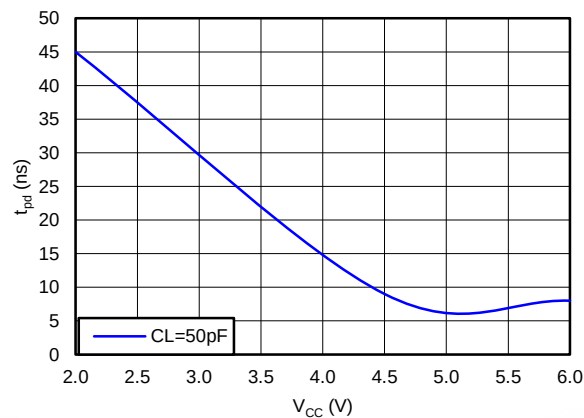
| PARAMETER | TEST CONDITIONS                                                       |                                          | MIN                | TYP       | MAX        | UNIT    |
|-----------|-----------------------------------------------------------------------|------------------------------------------|--------------------|-----------|------------|---------|
| $V_{OH}$  | $V_I = V_{IH} \text{ or } V_{IL}$                                     | $I_{OH} = -20 \mu A$                     | $V_{CC} = 2 V$     | 1.9       | 1.998      | V       |
|           |                                                                       |                                          | $V_{CC} = 4.5 V$   | 4.4       | 4.499      |         |
|           |                                                                       |                                          | $V_{CC} = 6 V$     | 5.9       | 5.999      |         |
|           |                                                                       | $I_{OH} = -4 \text{ mA}, V_{CC} = 4.5 V$ | $T_A = 25^\circ C$ | 3.98      | 4.3        |         |
|           |                                                                       |                                          | SN54HC00           | 3.7       |            |         |
|           |                                                                       |                                          | SN74HC00           | 3.84      |            |         |
|           |                                                                       | $I_{OH} = -5.2 \text{ mA}, V_{CC} = 6 V$ | $T_A = 25^\circ C$ | 5.48      | 5.8        |         |
|           |                                                                       |                                          | SN54HC00           | 5.2       |            |         |
|           |                                                                       |                                          | SN74HC00           | 5.34      |            |         |
| $V_{OL}$  | $V_I = V_{IH} \text{ or } V_{IL}$                                     | $I_{OL} = 20 \mu A$                      | $V_{CC} = 2 V$     | 0.002     | 0.1        | V       |
|           |                                                                       |                                          | $V_{CC} = 4.5 V$   | 0.001     | 0.1        |         |
|           |                                                                       |                                          | $V_{CC} = 6 V$     | 0.001     | 0.1        |         |
|           |                                                                       | $I_{OL} = 4 \text{ mA}, V_{CC} = 4.5 V$  | $T_A = 25^\circ C$ | 0.17      | 0.26       |         |
|           |                                                                       |                                          | SN54HC00           |           | 0.4        |         |
|           |                                                                       |                                          | SN74HC00           |           | 0.33       |         |
|           |                                                                       | $I_{OL} = 5.2 \text{ mA}, V_{CC} = 6 V$  | $T_A = 25^\circ C$ | 0.15      | 0.26       |         |
|           |                                                                       |                                          | SN54HC00           |           | 0.4        |         |
|           |                                                                       |                                          | SN74HC00           |           | 0.33       |         |
| $I_I$     | $V_I = V_{CC} \text{ or } 0, V_{CC} = 6 V$                            | $T_A = 25^\circ C$                       |                    | $\pm 0.1$ | $\pm 100$  | nA      |
|           |                                                                       | SNx4HC00                                 |                    |           | $\pm 1000$ |         |
| $I_{CC}$  | $V_I = V_{CC} \text{ or } 0, I_O = 0, V_{CC} = 6 V$                   | $T_A = 25^\circ C$                       |                    |           | 2          | $\mu A$ |
|           |                                                                       | SN54HC00                                 |                    |           | 40         |         |
|           |                                                                       | SN74HC00                                 |                    |           | 20         |         |
| $C_i$     | $V_{CC} = 2 V \text{ to } 6 V$                                        |                                          |                    | 3         | 10         | pF      |
| $C_{pd}$  | Power dissipation capacitance per gate<br>No load, $T_A = 25^\circ C$ |                                          |                    | 20        |            | pF      |

## 6.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF, see [Figure 2](#) (unless otherwise noted)

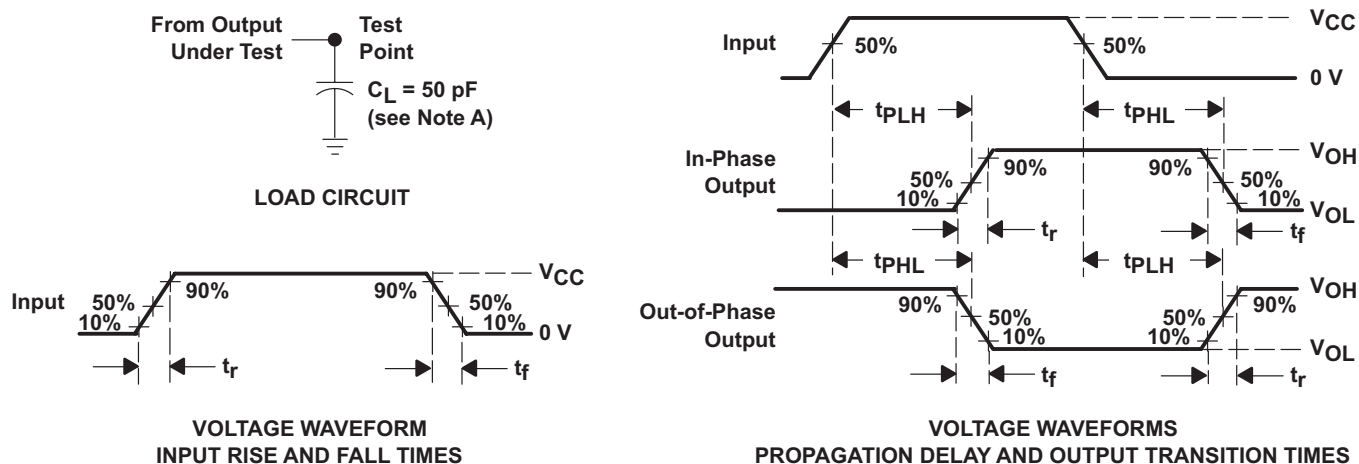
| PARAMETER | TEST CONDITIONS                   |                  |                          | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------|------------------|--------------------------|-----|-----|-----|------|
| $t_{pd}$  | From A or B (input) to Y (output) | $V_{CC} = 2$ V   | $T_A = 25^\circ\text{C}$ |     | 45  | 90  | ns   |
|           |                                   |                  | SN54HC00                 |     |     | 135 |      |
|           |                                   |                  | SN74HC00                 |     |     | 115 |      |
|           |                                   | $V_{CC} = 4.5$ V | $T_A = 25^\circ\text{C}$ |     | 9   | 18  |      |
|           |                                   |                  | SN54HC00                 |     |     | 27  |      |
|           |                                   |                  | SN74HC00                 |     |     | 23  |      |
|           |                                   | $V_{CC} = 6$ V   | $T_A = 25^\circ\text{C}$ |     | 8   | 15  |      |
|           |                                   |                  | SN54HC00                 |     |     | 23  |      |
|           |                                   |                  | SN74HC00                 |     |     | 20  |      |
| $t_t$     | To Y (output)                     | $V_{CC} = 2$ V   | $T_A = 25^\circ\text{C}$ |     | 38  | 75  | ns   |
|           |                                   |                  | SN54HC00                 |     |     | 110 |      |
|           |                                   |                  | SN74HC00                 |     |     | 95  |      |
|           |                                   | $V_{CC} = 4.5$ V | $T_A = 25^\circ\text{C}$ |     | 8   | 15  |      |
|           |                                   |                  | SN54HC00                 |     |     | 22  |      |
|           |                                   |                  | SN74HC00                 |     |     | 19  |      |
|           |                                   | $V_{CC} = 6$ V   | $T_A = 25^\circ\text{C}$ |     | 6   | 13  |      |
|           |                                   |                  | SN54HC00                 |     |     | 19  |      |
|           |                                   |                  | SN74HC00                 |     |     | 16  |      |

## 6.7 Typical Characteristics



**Figure 1. Propagation Delay vs  $V_{CC}$**

## 7 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and test-fixtue capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

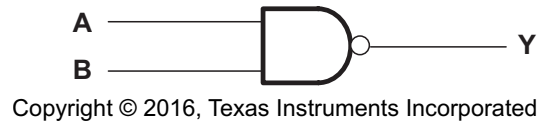
**Figure 2. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SNx4HC00 devices perform the NAND Boolean function  $Y = \overline{A} \times \overline{B}$  or  $Y = \overline{A + B}$  in positive logic. The devices have a wide operating range of  $V_{CC}$  from 2 V to 6 V.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The SNx4HC00 devices have a wide operating voltage range that operates from 2 V to 6 V. They allow inputs and outputs up to  $V_{CC}$ . The devices can drive outputs at 4 mA at 5-V  $V_{CC}$ .

### 8.4 Device Functional Modes

[Table 1](#) lists the functional modes for the SNx4HC00.

**Table 1. Function Table**

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | L      |
| L      | X | H      |
| X      | L | H      |



## 9 Application and Implementation

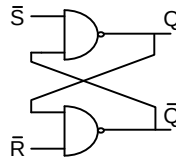
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4HC00 is a low-power, wide-operating-voltage NAND gate. This device can drive up to 10 LSTTL loads and can drive 4-mA outputs at 5-V  $V_{CC}$ .

### 9.2 Typical Application



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**Figure 3. Typical NAND Gate Application and Supply Voltage**

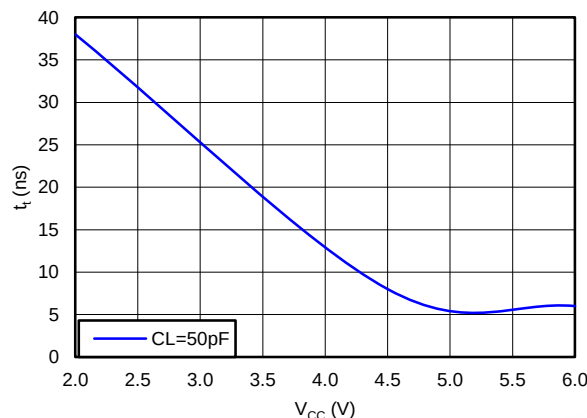
#### 9.2.1 Design Requirements

The SNx4HC00 devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it drives currents that would exceed maximum limits. The high drive also creates fast edges into light loads. Routing and load conditions must be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#).
- Recommended output conditions:
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs must not be pulled above  $V_{CC}$ .

#### 9.2.3 Application Curve



**Figure 4. Transition Time vs  $V_{CC}$**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in [Recommended Operating Conditions](#).

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F bypass capacitor; if there are multiple  $V_{CC}$  pins, then TI recommends 0.01- $\mu$ F or 0.022- $\mu$ F bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu$ F and a 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

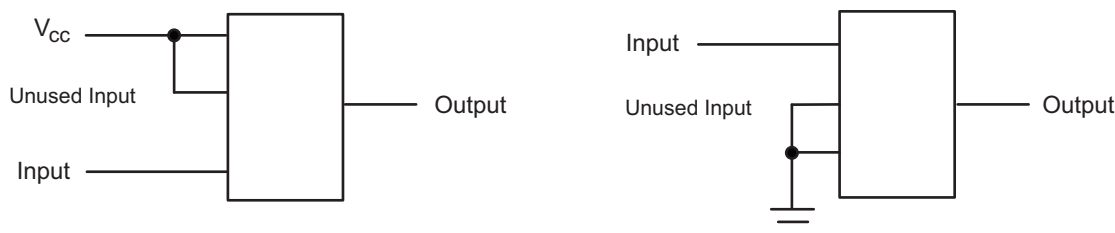
## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 5](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

### 11.2 Layout Example



**Figure 5. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54HC00 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74HC00 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

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**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)           | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|--------------------------------------|----------------------|--------------|-----------------------------------|-------------------------|
| 5962-8403701VCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8403701VC<br>A<br>SNV54HC00J | <a href="#">Samples</a> |
| 5962-8403701VDA  | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8403701VD<br>A<br>SNV54HC00W | <a href="#">Samples</a> |
| 84037012A        | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | 84037012A<br>SNJ54HC<br>00FK      | <a href="#">Samples</a> |
| 8403701CA        | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 8403701CA<br>SNJ54HC00J           | <a href="#">Samples</a> |
| 8403701DA        | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 8403701DA<br>SNJ54HC00W           | <a href="#">Samples</a> |
| JM38510/65001B2A | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65001B2A              | <a href="#">Samples</a> |
| JM38510/65001BCA | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65001BCA              | <a href="#">Samples</a> |
| JM38510/65001BDA | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65001BDA              | <a href="#">Samples</a> |
| M38510/65001B2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65001B2A              | <a href="#">Samples</a> |
| M38510/65001BCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65001BCA              | <a href="#">Samples</a> |
| M38510/65001BDA  | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65001BDA              | <a href="#">Samples</a> |
| SN54HC00J        | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54HC00J                         | <a href="#">Samples</a> |
| SN74HC00D        | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                              | <a href="#">Samples</a> |
| SN74HC00DBR      | ACTIVE        | SSOP         | DB                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                              | <a href="#">Samples</a> |
| SN74HC00DE4      | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                              | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)      | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|--------------------------------------|----------------------|--------------|------------------------------|-------------------------|
| SN74HC00DG4      | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00DR       | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00DRE4     | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00DRG4     | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00DT       | ACTIVE        | SOIC         | D                  | 14   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00DTE4     | ACTIVE        | SOIC         | D                  | 14   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00DTG4     | ACTIVE        | SOIC         | D                  | 14   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00N        | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU   SN                          | N / A for Pkg Type   | -40 to 85    | SN74HC00N                    | <a href="#">Samples</a> |
| SN74HC00NE4      | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HC00N                    | <a href="#">Samples</a> |
| SN74HC00NSR      | ACTIVE        | SO           | NS                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00PW       | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00PWR      | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00PWRG4    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SN74HC00PWT      | ACTIVE        | TSSOP        | PW                 | 14   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HC00                         | <a href="#">Samples</a> |
| SNJ54HC00FK      | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | 84037012A<br>SNJ54HC<br>00FK | <a href="#">Samples</a> |
| SNJ54HC00J       | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 8403701CA<br>SNJ54HC00J      | <a href="#">Samples</a> |
| SNJ54HC00W       | ACTIVE        | CFP          | W                  | 14   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 8403701DA<br>SNJ54HC00W      | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

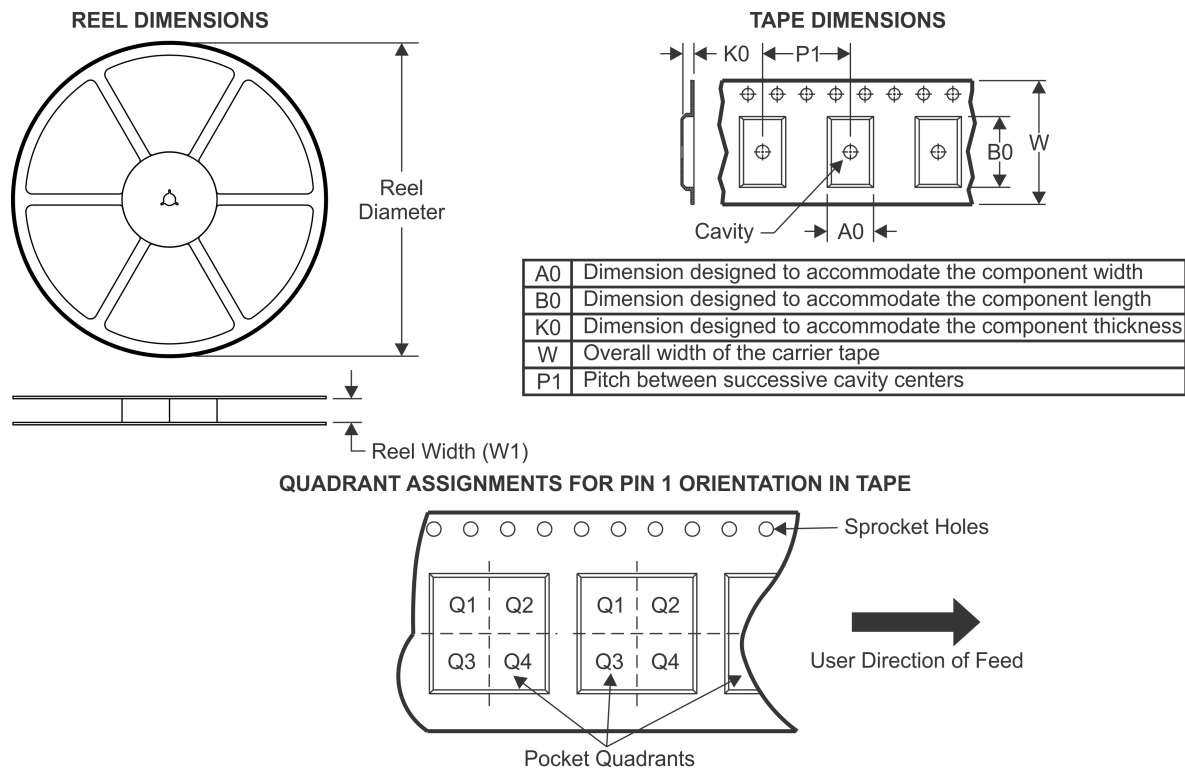
**OTHER QUALIFIED VERSIONS OF SN54HC00, SN54HC00-SP, SN74HC00 :**

- Catalog: [SN74HC00](#), [SN54HC00](#)
- Automotive: [SN74HC00-Q1](#), [SN74HC00-Q1](#)
- Military: [SN54HC00](#)

- Space: [SN54HC00-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

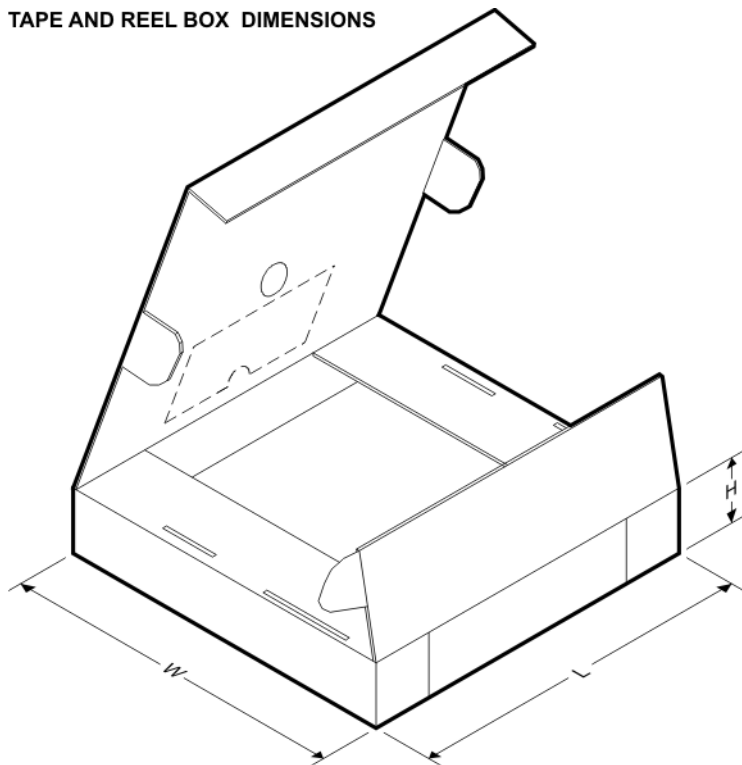
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC00DR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC00DR    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC00DRG4  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC00DT    | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC00PWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HC00PWR   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HC00PWRG4 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HC00PWT   | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS

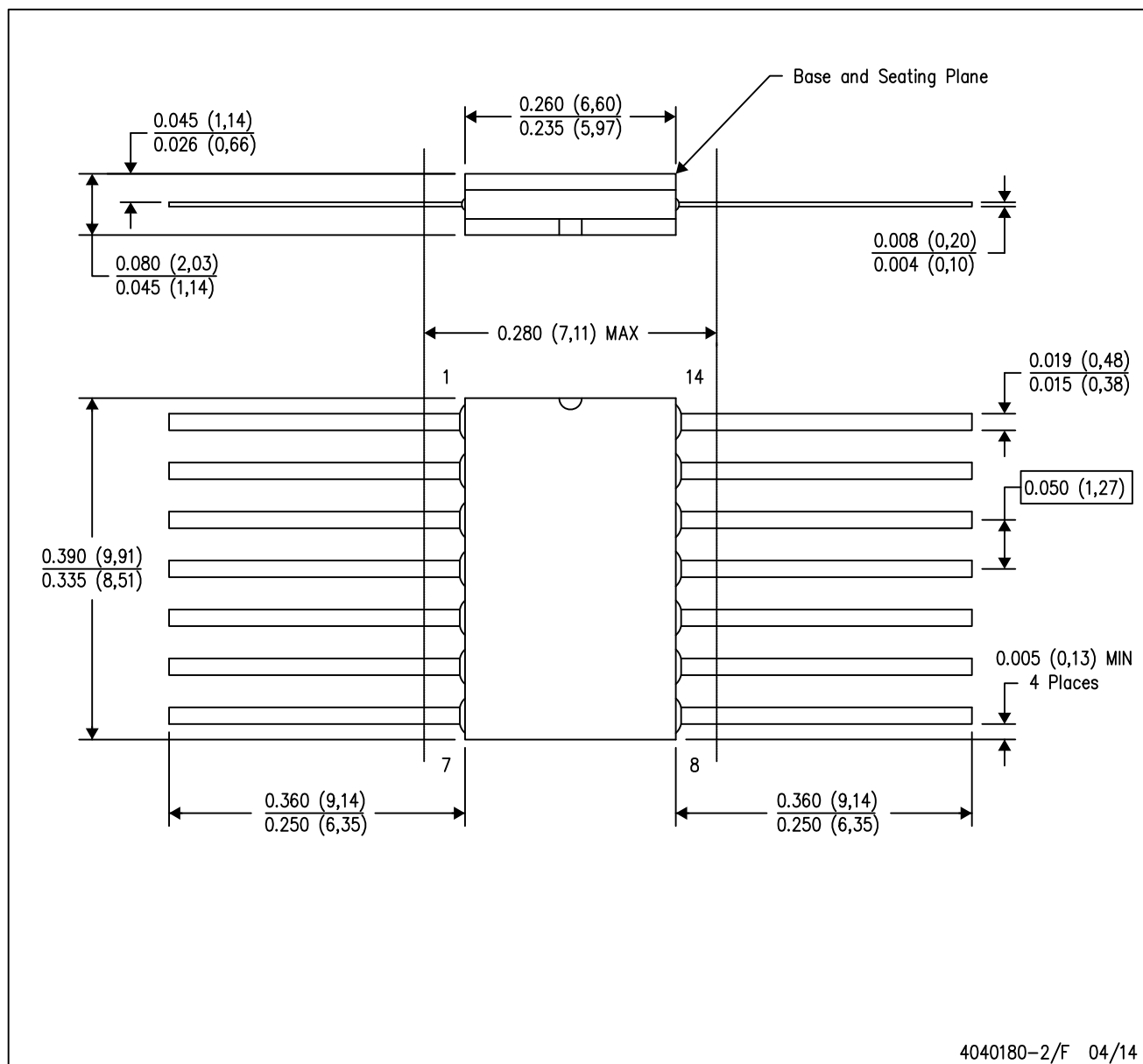


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC00DR    | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74HC00DR    | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74HC00DRG4  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74HC00DT    | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |
| SN74HC00PWR   | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74HC00PWR   | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74HC00PWRG4 | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74HC00PWT   | TSSOP        | PW              | 14   | 250  | 367.0       | 367.0      | 35.0        |

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



## NOTES:

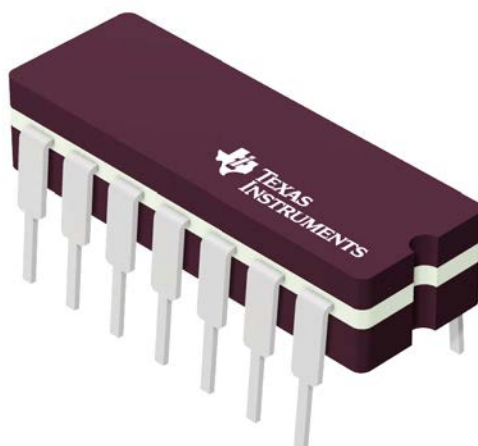
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14

**J 14**

## GENERIC PACKAGE VIEW

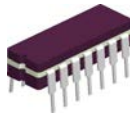
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

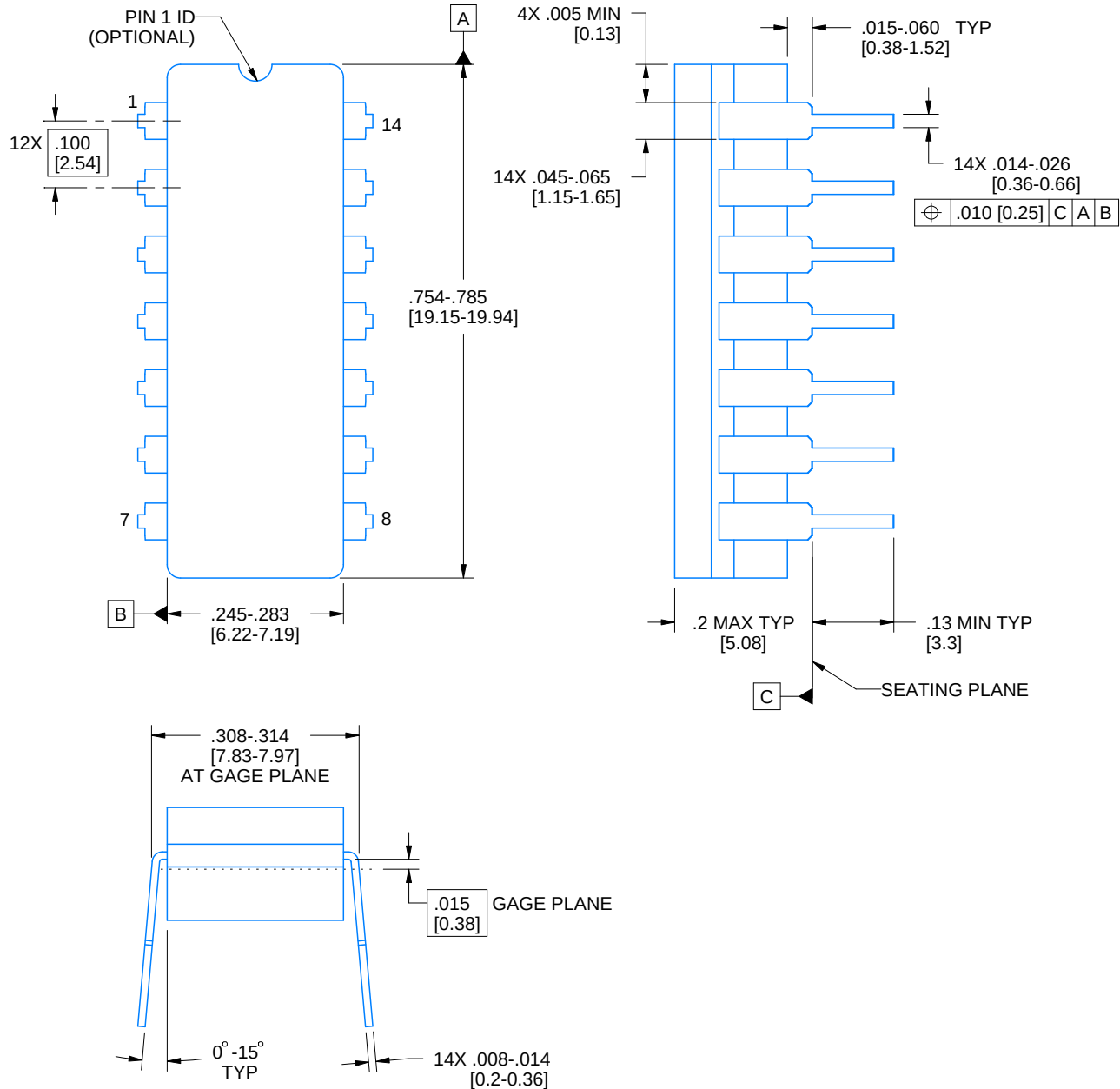


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



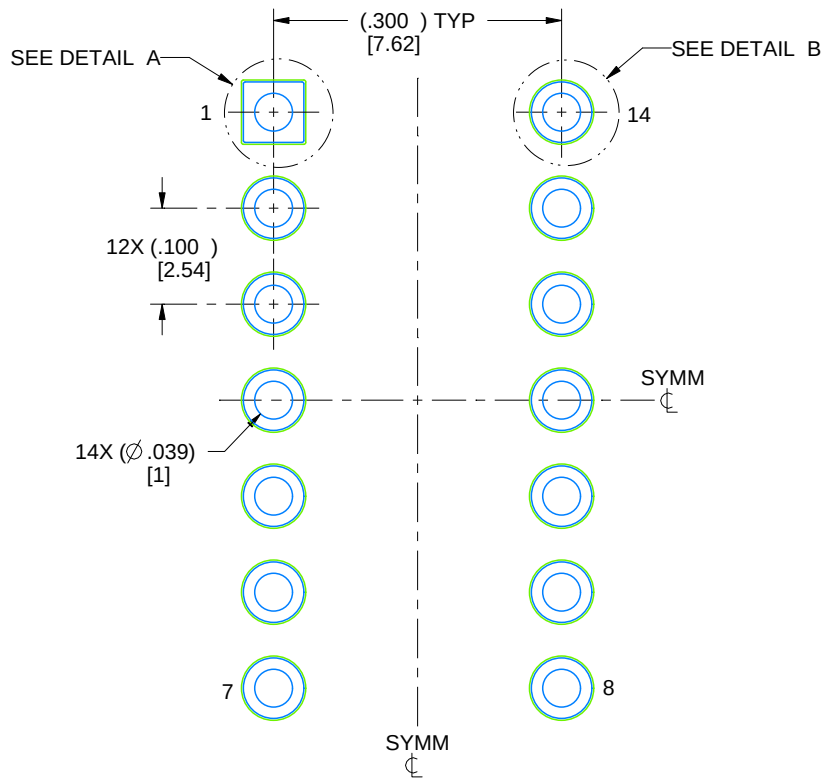
**TEXAS  
INSTRUMENTS**  
www.ti.com

# EXAMPLE BOARD LAYOUT

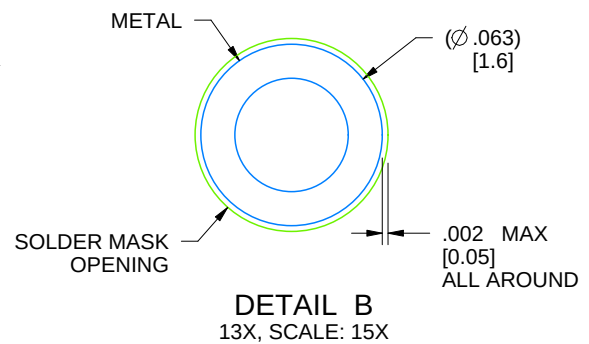
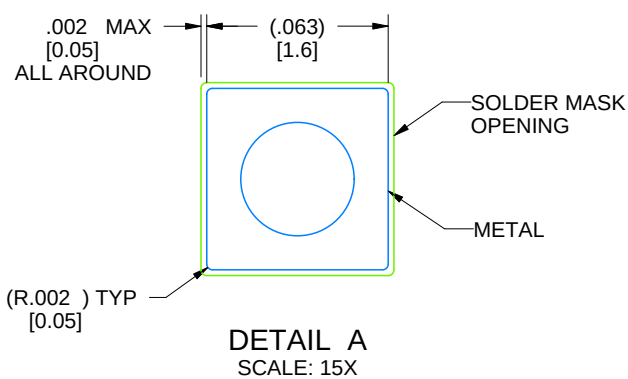
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



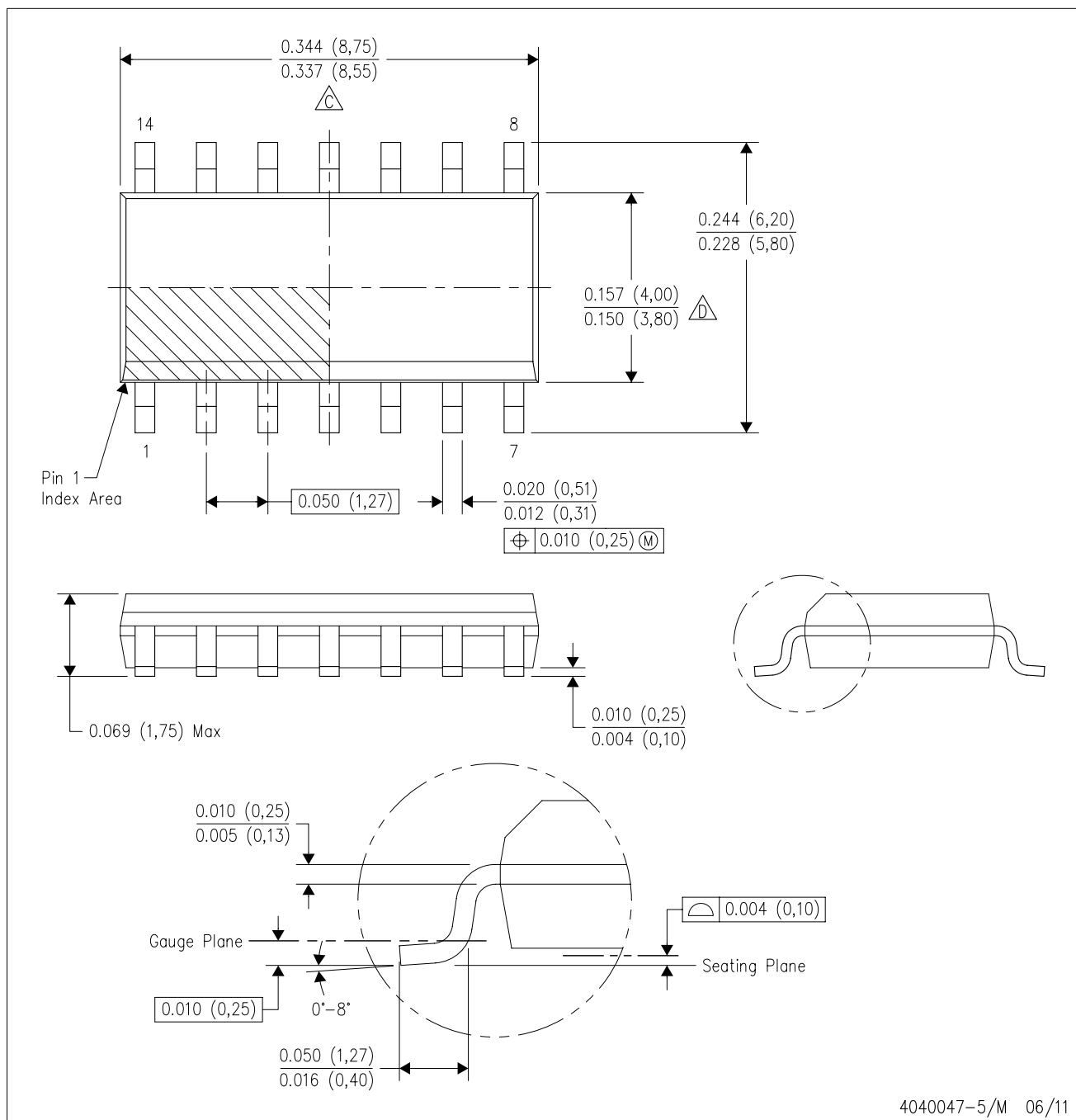
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



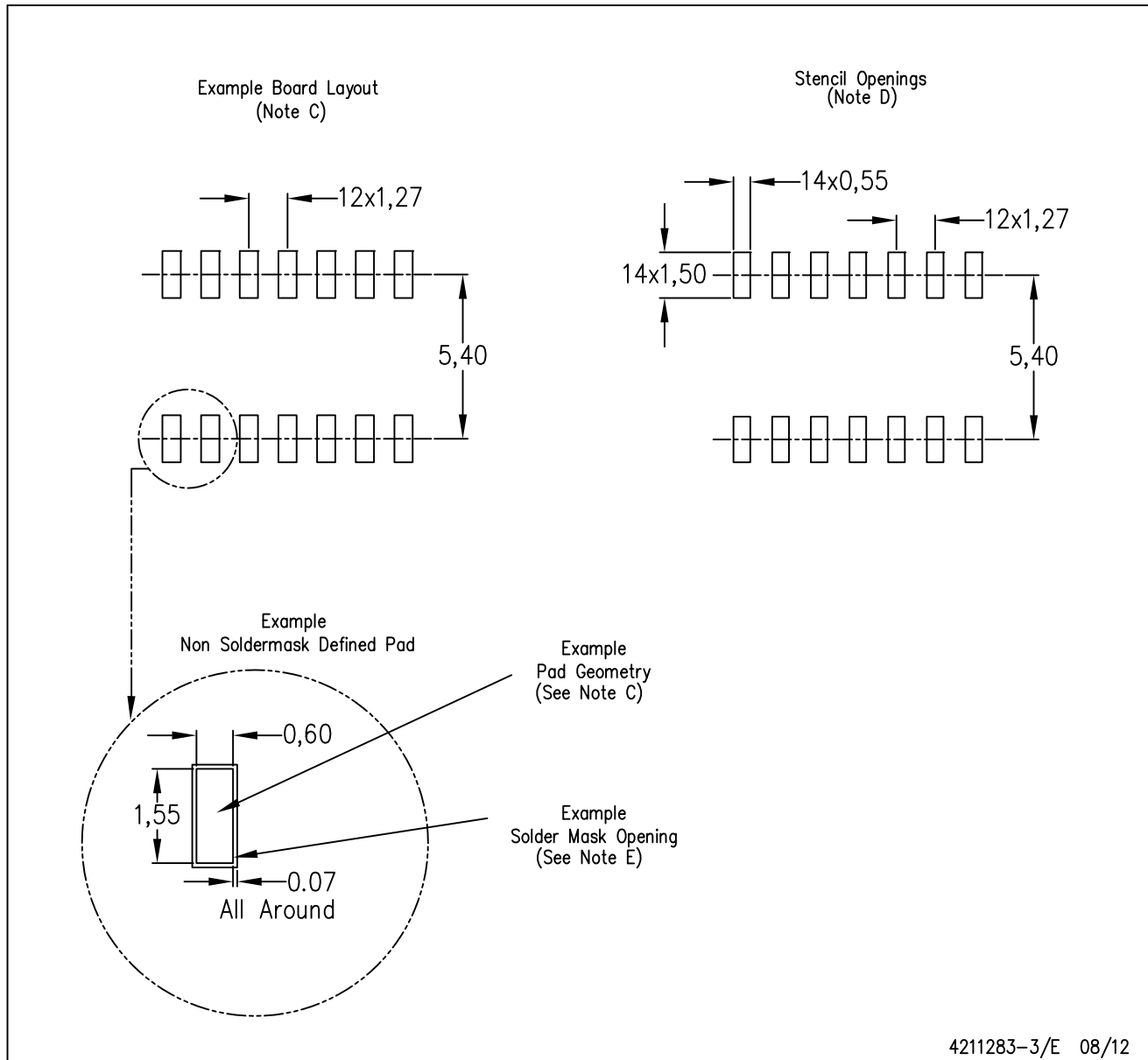
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

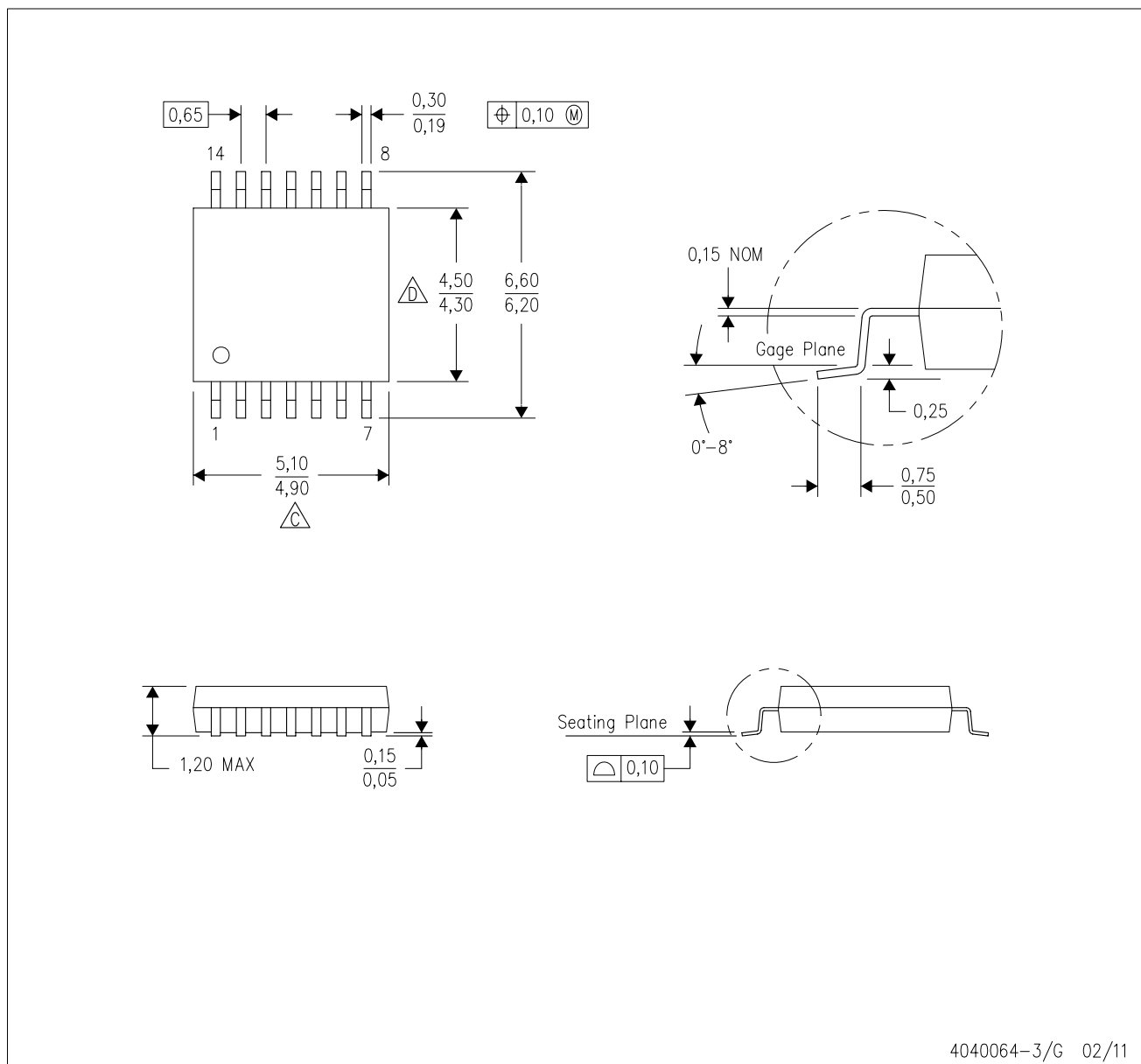
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

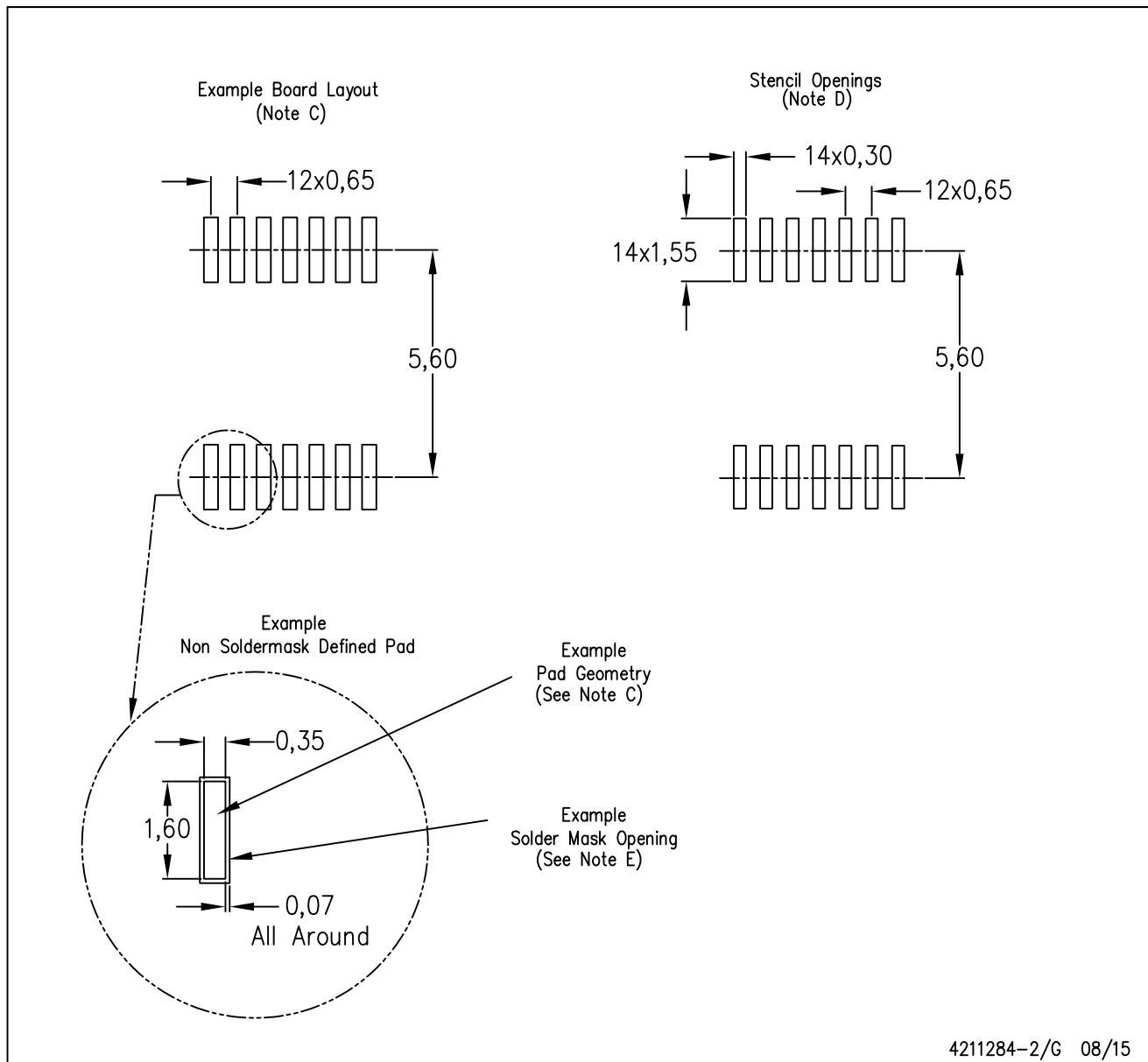
PLASTIC SMALL OUTLINE





PW (R-PDSO-G14)

# PLASTIC SMALL OUTLINE



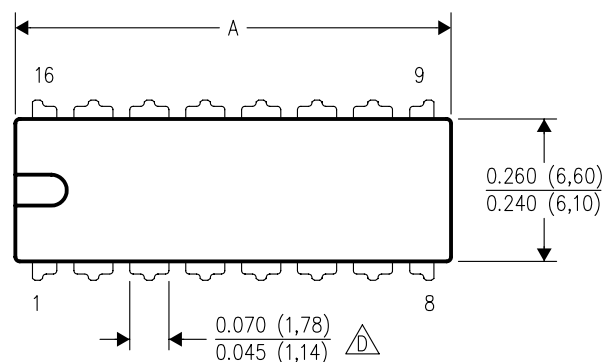
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

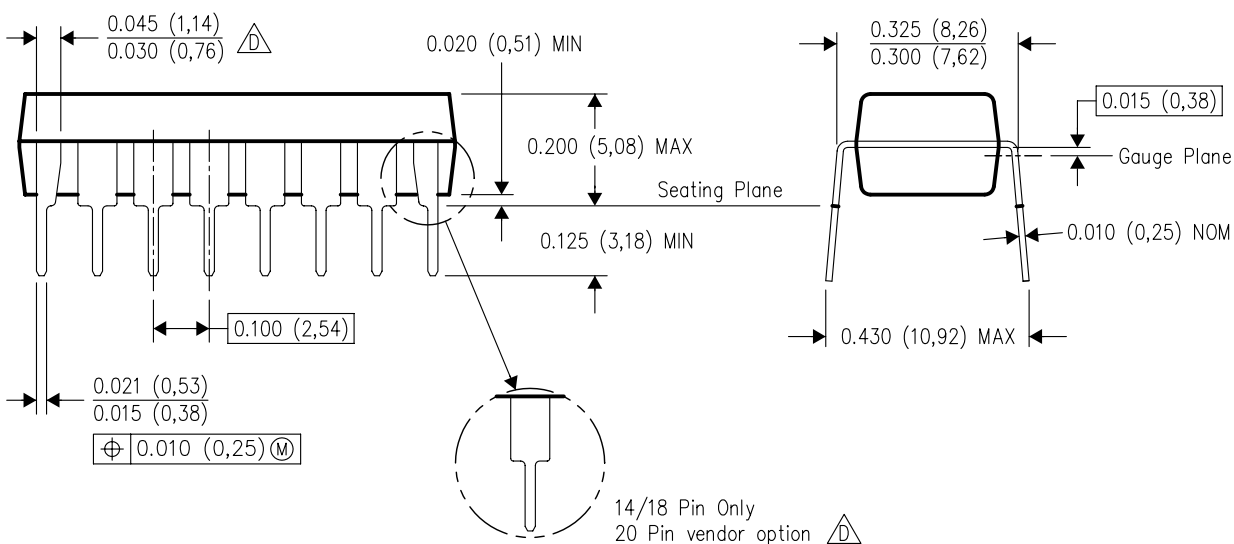
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

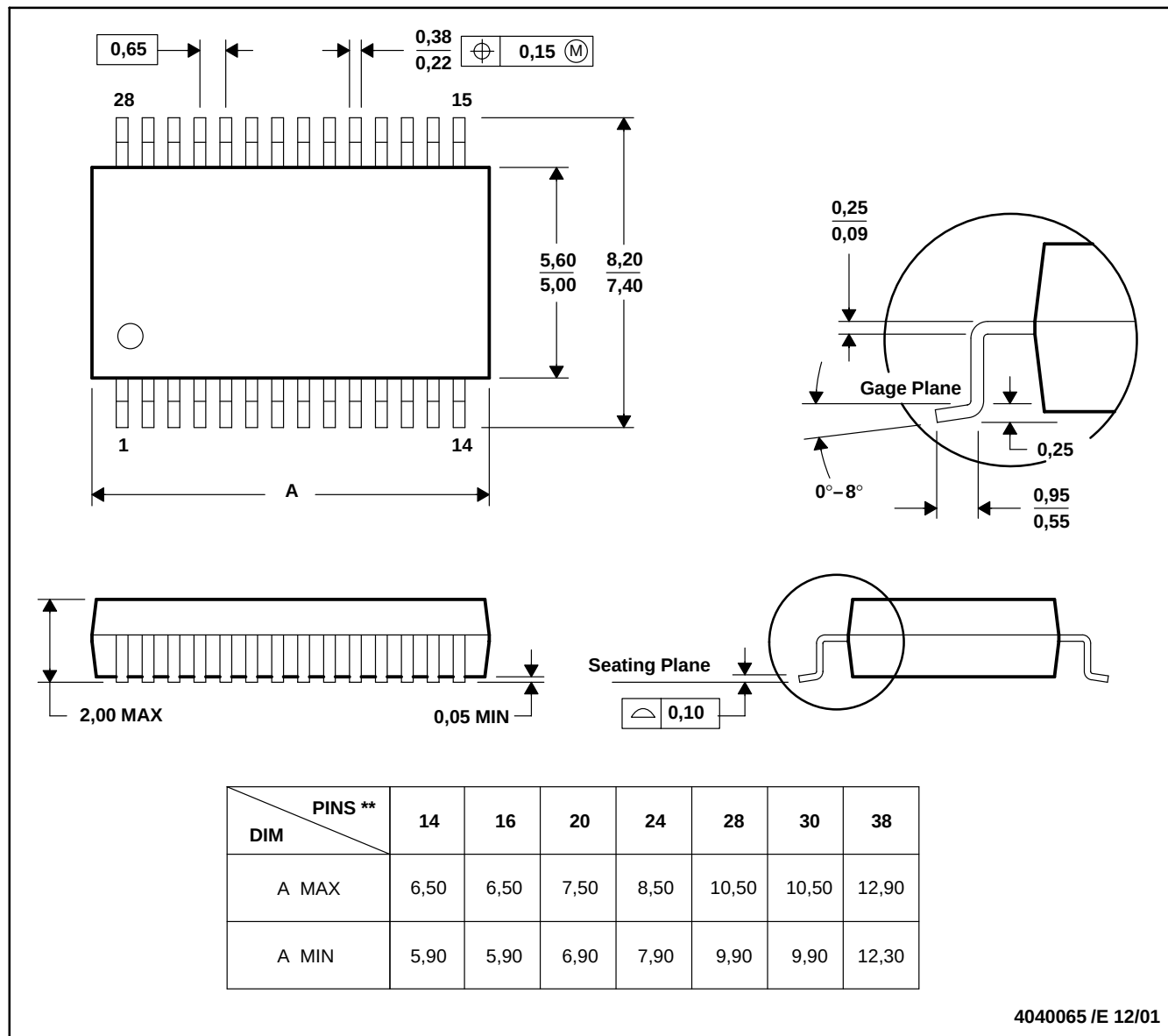
NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

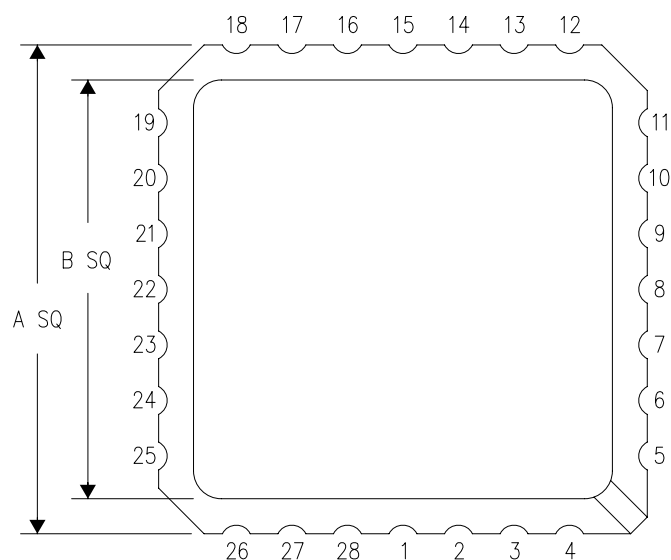


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

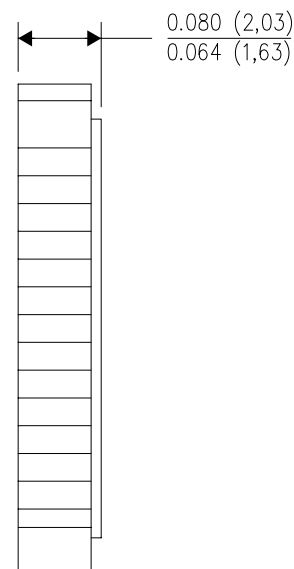
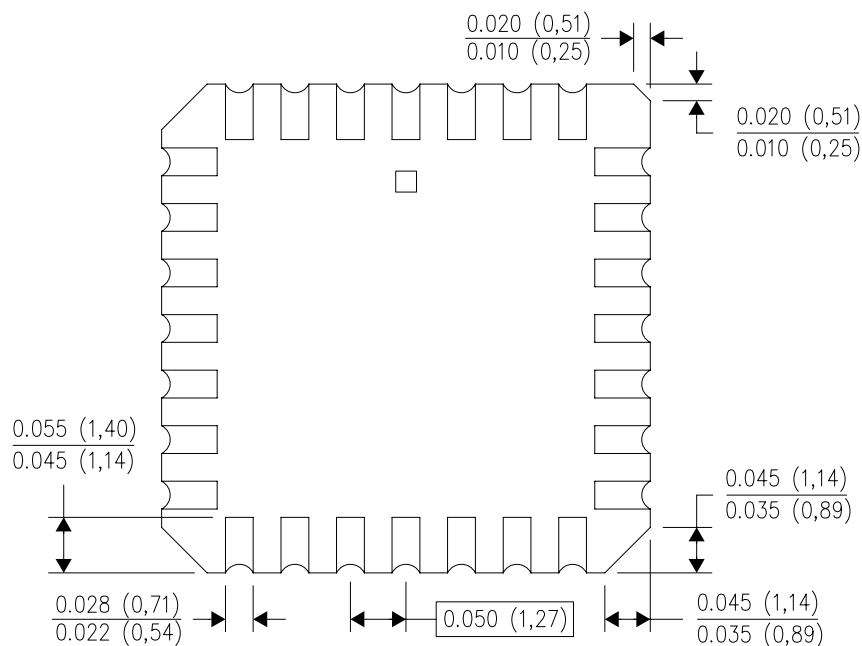
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

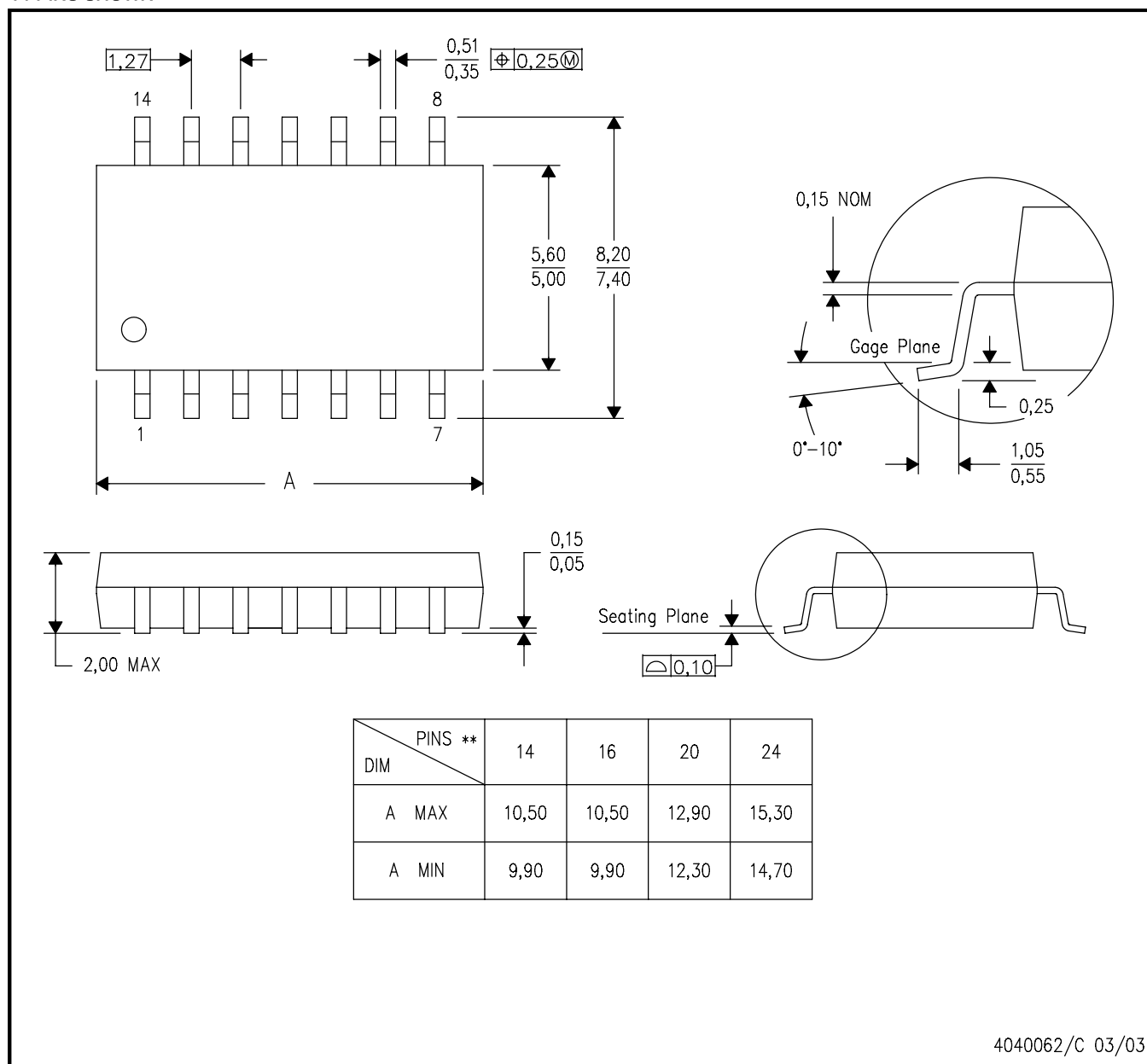
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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