

# SN74GTLPH1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

- Member of the Texas Instruments Widebus™ Family
- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTTL Logic Levels
- LVTTTL Interfaces Are 5-V Tolerant
- High-Drive GTLP Outputs (100 mA)
- LVTTTL Outputs (–24 mA/24 mA)
- Variable Edge-Rate Control ( $\overline{\text{ERC}}$ ) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- $I_{\text{off}}$ , Power-Up 3-State, and BIAS  $V_{\text{CC}}$  Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed  $V_{\text{CC}}$  and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

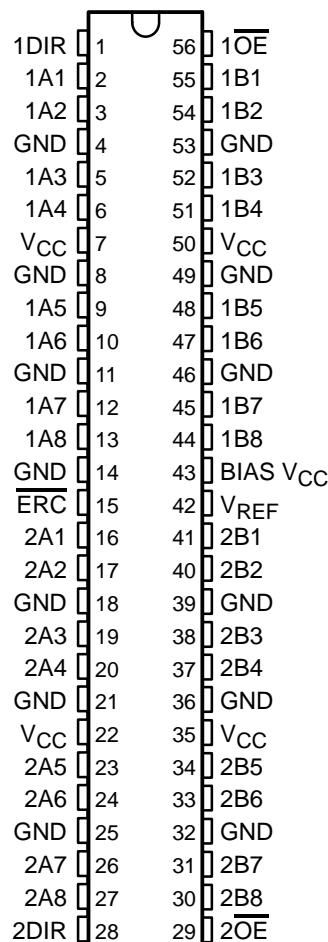
### description

The SN74GTLPH1645 is a high-drive, 16-bit bus transceiver that provides LVTTTL-to-GTLP and GTLP-to-LVTTTL signal-level translation. It is partitioned as two 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11  $\Omega$ .

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1645 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ( $V_{\text{TT}} = 1.2 \text{ V}$  and  $V_{\text{REF}} = 0.8 \text{ V}$ ) or GTLP ( $V_{\text{TT}} = 1.5 \text{ V}$  and  $V_{\text{REF}} = 1 \text{ V}$ ) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.  $V_{\text{REF}}$  is the B-port differential input reference voltage.

DGG OR DGV PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

OEC, TI-OPC, and Widebus are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

# SN74GTLPH1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### description (continued)

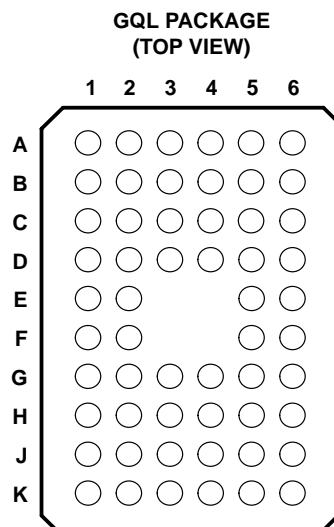
This device is fully specified for live-insertion applications using  $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ( $\overline{ERC}$ ). Changing the  $\overline{ERC}$  input voltage between GND and  $V_{CC}$  adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ( $\overline{OE}$ ) input should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



### terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	1DIR	$\overline{1OE}$	1B1	1B2
B	1A4	1A3	GND	GND	1B3	1B4
C	1A5	GND	$V_{CC}$	$V_{CC}$	GND	1B5
D	1A7	1A6	GND	GND	1B6	1B7
E	GND	1A8			1B8	BIAS $V_{CC}$
F	$\overline{ERC}$	2A1			2B1	$V_{REF}$
G	2A2	2A3	GND	GND	2B3	2B2
H	2A4	GND	$V_{CC}$	$V_{CC}$	GND	2B4
J	2A5	2A6	GND	GND	2B6	2B5
K	2A7	2A8	2DIR	$\overline{2OE}$	2B8	2B7

### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1645DGGR	GTLPH1645
	TVSOP – DGV	Tape and reel	SN74GTLPH1645DGVR	GL45
	VFBGA – GQL	Tape and reel	SN74GTLPH1645GQLR	GL45

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



# SN74GTLP1645

## 16-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### functional description

The SN74GTLP1645 is a high-drive (100 mA), 16-bit bus transceiver partitioned as two 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input.  $\overline{OE}$  can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

For A-to-B data flow, when  $\overline{OE}$  is low and DIR is high, the B outputs take on the logic value of the A inputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except  $\overline{OE}$  and DIR are low.

### Function Tables

OUTPUT CONTROL

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

B-PORT EDGE-RATE CONTROL ( $\overline{ERC}$ )

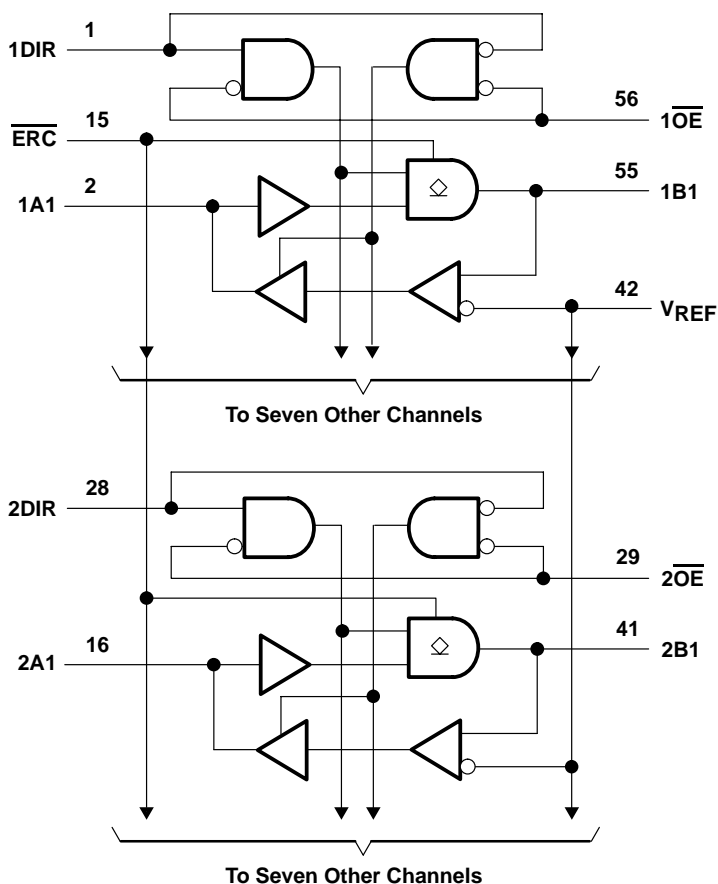
INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V <sub>CC</sub>	Fast

# SN74GTLPH1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN74GTLP1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ and BIAS $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): A port, $\overline{ERC}$ , and control inputs .....	–0.5 V to 7 V
B port and $V_{REF}$ .....	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1): A port .....	–0.5 V to 7 V
B port .....	–0.5 V to 4.6 V
Current into any output in the low state, $I_O$ : A port .....	48 mA
B port .....	200 mA
Current into any A port output in the high state, $I_O$ (see Note 2) .....	48 mA
Continuous current through each $V_{CC}$ or GND .....	±100 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	64°C/W
DGV package .....	48°C/W
GQL package .....	42°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



# SN74GTLPH1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### recommended operating conditions (see Notes 4 through 7)

		MIN	NOM	MAX	UNIT	
$V_{CC}$ , BIAS $V_{CC}$	Supply voltage	3.15	3.3	3.45	V	
$V_{TT}$	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
$V_{REF}$	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
$V_I$	Input voltage	B port	$V_{TT}$		V	
		Except B port	$V_{CC}$	5.5		
$V_{IH}$	High-level input voltage	B port	$V_{REF}+0.05$		V	
		$\overline{ERC}$	$V_{CC}-0.6$	$V_{CC}$		5.5
		Except B port and $\overline{ERC}$	2			
$V_{IL}$	Low-level input voltage	B port	$V_{REF}-0.05$		V	
		$\overline{ERC}$	GND	0.6		
		Except B port and $\overline{ERC}$	0.8			
$I_{IK}$	Input clamp current			-18	mA	
$I_{OH}$	High-level output current	A port			-24	mA
$I_{OL}$	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	20			$\mu$ s/V	
$T_A$	Operating free-air temperature	-40		85	$^{\circ}$ C	

- NOTES: 4. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS  $V_{CC} = 3.3$  V first, I/O second, and  $V_{CC} = 3.3$  V last, because the BIAS  $V_{CC}$  precharge circuitry is disabled when any  $V_{CC}$  pin is connected. The control and  $V_{REF}$  inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6.  $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded.
7.  $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ . TI-OPC circuitry is enabled in the A-to-B direction and is activated when  $V_{TT} > 0.7$  V above  $V_{REF}$ . If operated in the A-to-B direction,  $V_{REF}$  should be set to within 0.6 V of  $V_{TT}$  to minimize current drain.



# SN74GTLPH1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

**electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.15\text{ V}$ , $I_I = -18\text{ mA}$				-1.2	V
$V_{OH}$	A port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			V
		$V_{CC} = 3.15\text{ V}$ , $I_{OH} = -12\text{ mA}$		2.4			
		$V_{CC} = 3.15\text{ V}$ , $I_{OH} = -24\text{ mA}$		2			
$V_{OL}$	A port	$V_{CC} = 3.15\text{ V to }3.45\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$				0.2	V
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 12\text{ mA}$				0.4	
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 24\text{ mA}$				0.5	
	B port	$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 10\text{ mA}$				0.2	
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 64\text{ mA}$				0.4	
		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 100\text{ mA}$				0.55	
$I_I$		Control inputs, $V_{CC} = 3.45\text{ V}$ , $V_I = 0\text{ or }5.5\text{ V}$				$\pm 10$	$\mu\text{A}$
$I_{OZH}^\ddagger$	A port	$V_{CC} = 3.45\text{ V}$ , $V_O = V_{CC}$				10	$\mu\text{A}$
	B port	$V_{CC} = 3.45\text{ V}$ , $V_O = 1.5\text{ V}$				10	
$I_{OZL}^\ddagger$		A and B ports, $V_{CC} = 3.45\text{ V}$ , $V_O = \text{GND}$				-10	$\mu\text{A}$
$I_{BHL}^\S$		A port, $V_{CC} = 3.15\text{ V}$ , $V_I = 0.8\text{ V}$				75	$\mu\text{A}$
$I_{BHH}^\parallel$		A port, $V_{CC} = 3.15\text{ V}$ , $V_I = 2\text{ V}$				-75	$\mu\text{A}$
$I_{BHLO}^\#$		A port, $V_{CC} = 3.45\text{ V}$ , $V_I = 0\text{ to }V_{CC}$				500	$\mu\text{A}$
$I_{BHHO}^\parallel$		A port, $V_{CC} = 3.45\text{ V}$ , $V_I = 0\text{ to }V_{CC}$				-500	$\mu\text{A}$
$I_{CC}$	A or B port	$V_{CC} = 3.45\text{ V}$ , $I_O = 0$ , $V_I$ (A or control input) = $V_{CC}$ or GND, $V_I$ (B port) = $V_{TT}$ or GND		Outputs high		40	mA
				Outputs low		40	
				Outputs disabled		40	
$\Delta I_{CC}^\star$		$V_{CC} = 3.45\text{ V}$ , One A-port or control input at $V_{CC} - 0.6\text{ V}$ , Other A or control inputs at $V_{CC}$ or GND				1.5	mA
$C_i$		Control inputs, $V_I = 3.15\text{ V or }0$			4	5	pF
$C_{io}$	A port	$V_O = 3.15\text{ V or }0$			6.5	7.5	pF
	B port	$V_O = 1.5\text{ V or }0$			9.5	11	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{ILmax}$ .  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{ILmax}$ .

¶ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IHmin}$ .  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IHmin}$ .

# An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

|| An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

\* This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

### hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ ,	BIAS $V_{CC} = 0$ ,	$V_I$ or $V_O = 0\text{ to }5.5\text{ V}$		10	$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ ,	$V_O = 0.5\text{ V to }3\text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ ,	$V_O = 0.5\text{ V to }3\text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$



# SN74GTLPH1645

## 16-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0,$	BIAS $V_{CC} = 0,$	$V_I$ or $V_O = 0$ to 1.5 V	10		$\mu A$
$I_{OZPU}$	$V_{CC} = 0$ to 1.5 V,	BIAS $V_{CC} = 0,$	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$	$\pm 30$		$\mu A$
$I_{OZPD}$	$V_{CC} = 1.5$ V to 0,	BIAS $V_{CC} = 0,$	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$	$\pm 30$		$\mu A$
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0$ to 3.15 V	BIAS $V_{CC} = 3.15$ V to 3.45 V,	$V_O$ (B port) = 0 to 1.5 V	5		mA
	$V_{CC} = 3.15$ V to 3.45 V			10		$\mu A$
$V_O$	$V_{CC} = 0,$	BIAS $V_{CC} = 3.3$ V,	$I_O = 0$	0.95	1.05	V
$I_O$	$V_{CC} = 0,$	BIAS $V_{CC} = 3.15$ V to 3.45 V,	$V_O$ (B port) = 0.6 V	-1		$\mu A$

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{PLH}$	A	B	Slow	3.9		7.2	ns
$t_{PHL}$				3.1		8.4	
$t_{PLH}$	A	B	Fast	2.6		5.7	ns
$t_{PHL}$				2.1		5.8	
$t_{en}$	$\overline{OE}$	B	Slow	4.1		7.3	ns
$t_{dis}$				4		9.4	
$t_{en}$	$\overline{OE}$	B	Fast	2.9		5.9	ns
$t_{dis}$				4		6.9	
$t_r$	Rise time, B outputs (20% to 80%)		Slow	3		ns	
			Fast	1.5			
$t_f$	Fall time, B outputs (80% to 20%)		Slow	4		ns	
			Fast	2.5			
$t_{PLH}$	B	A	—	0.5		6.7	ns
$t_{PHL}$				1.2		4.5	
$t_{en}$	$\overline{OE}$	A	—	1.1		6.3	ns
$t_{dis}$				1.7		5.1	

† Slow ( $\overline{ERC} = GND$ ) and Fast ( $\overline{ERC} = V_{CC}$ )

‡ All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ C$ .

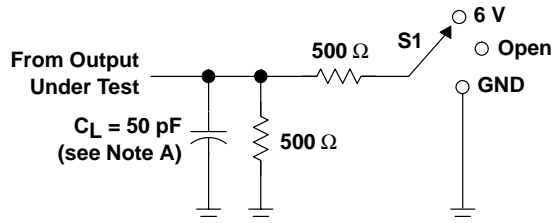


# SN74GTLPH1645

## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

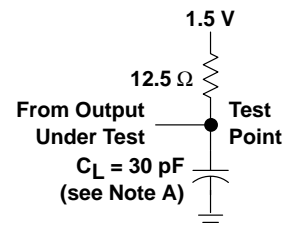
SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

### PARAMETER MEASUREMENT INFORMATION

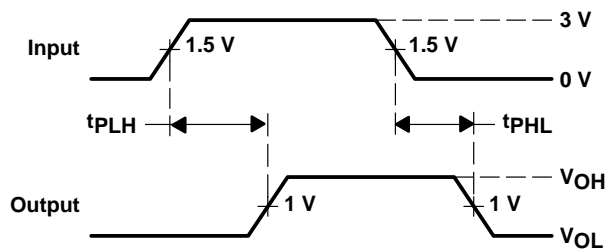


**LOAD CIRCUIT FOR A OUTPUTS**

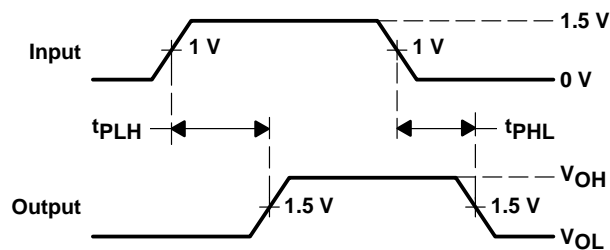
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



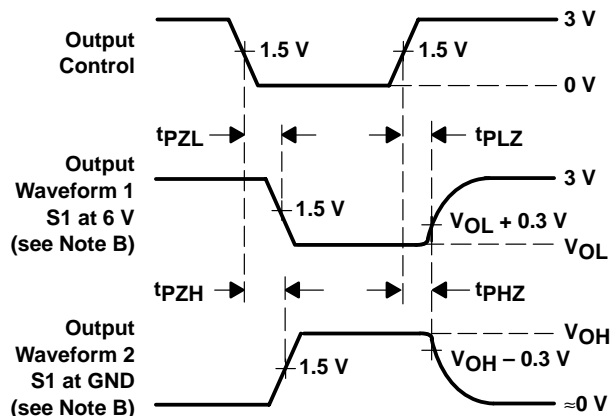
**LOAD CIRCUIT FOR B OUTPUTS**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(A port to B port)**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(B port to A port)**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
(A port)**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\approx$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \approx 2$  ns,  $t_f \approx 2$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

# SN74GTLP1645 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVER

SCES290D – OCTOBER 1999 – REVISED SEPTEMBER 2001

## DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See [www.ti.com/sc/gtlp](http://www.ti.com/sc/gtlp) for more information.

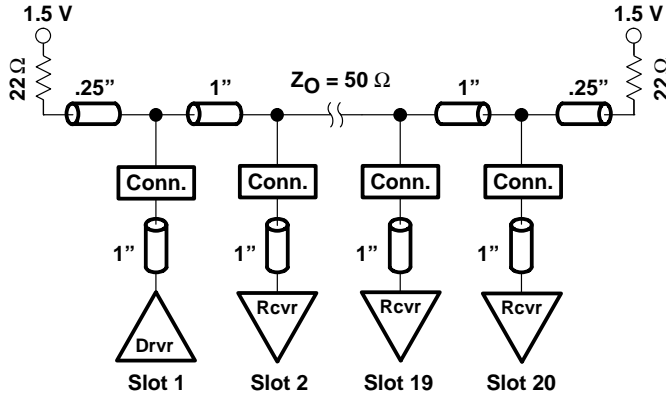


Figure 2. High-Drive Test Backplane

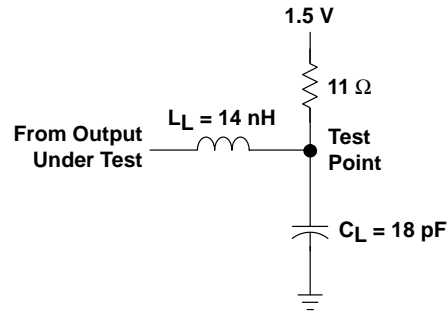


Figure 3. High-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
$t_{PLH}$	A	B	Slow	4.9	ns
$t_{PHL}$				4.9	
$t_{PLH}$	A	B	Fast	3.7	ns
$t_{PHL}$				3.7	
$t_{en}$	$\overline{OE}$	B	Slow	5.1	ns
$t_{dis}$				5.4	
$t_{en}$	$\overline{OE}$	B	Fast	4.1	ns
$t_{dis}$				4.1	
$t_r$	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
$t_f$	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ( $\overline{ERC} = GND$ ) and Fast ( $\overline{ERC} = V_{CC}$ )

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . All values are derived from TI-SPIICE models.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

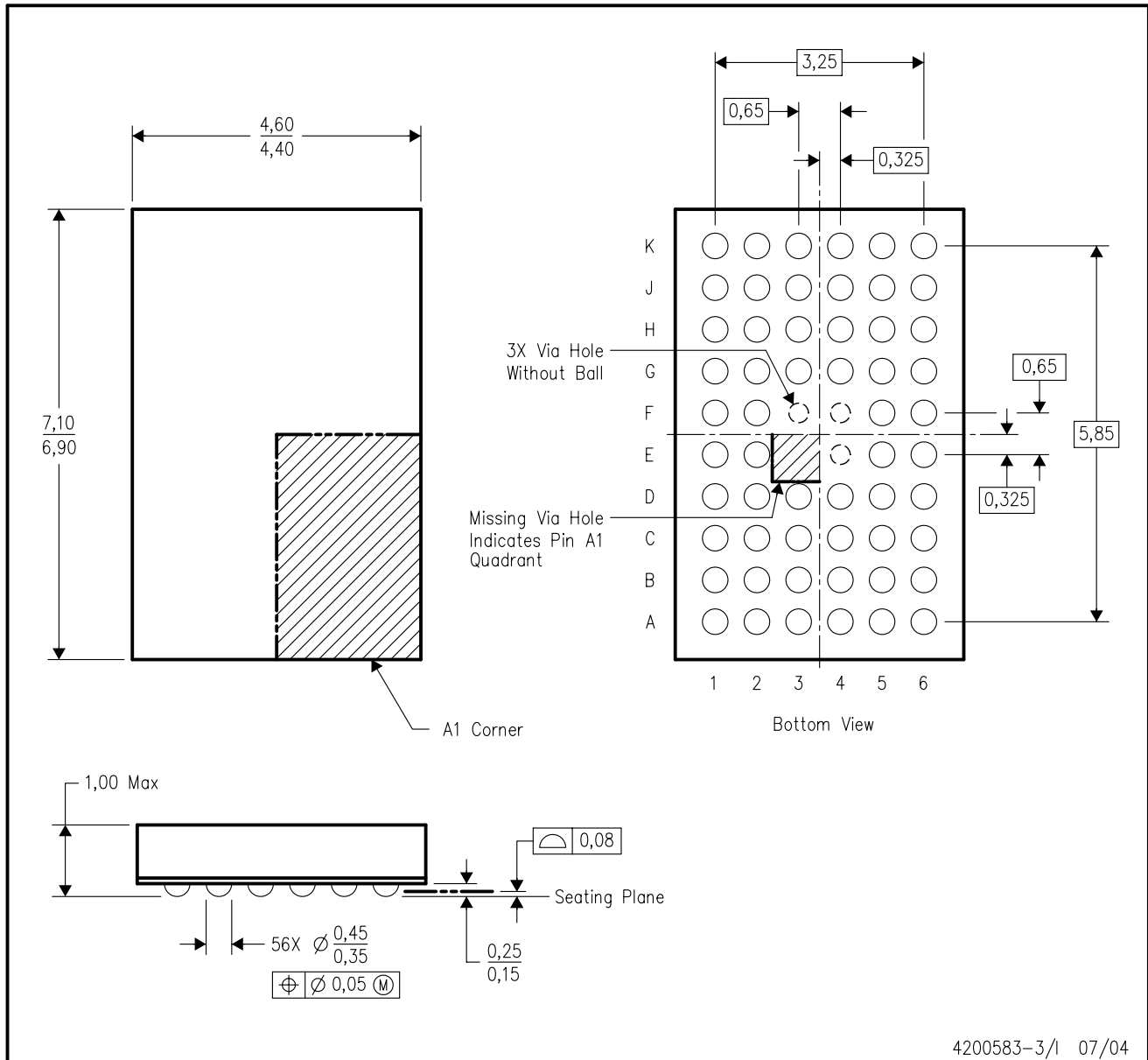


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated