

# SN54F299, SN74F299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

The SN54F299 is obsolete and no longer supplied.

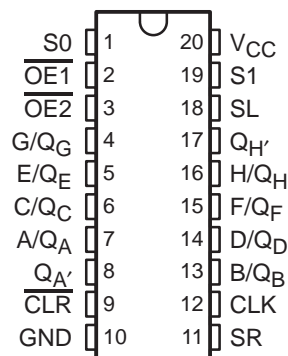
- **Four Modes of Operation:**
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- **Operates With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - Stacked or Pushdown Registers
  - Buffer Storage
  - Accumulator Registers

### description/ordering information

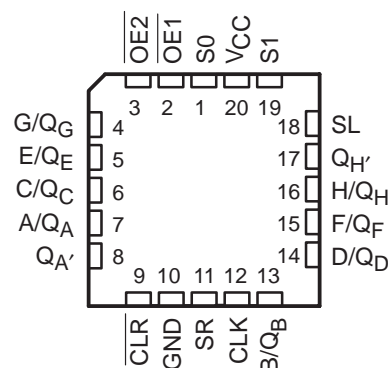
These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0, S_1$ ) inputs and two output-enable ( $\overline{OE1}, \overline{OE2}$ ) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE1}$  or  $\overline{OE2}$  high disables the outputs but has no effect on clearing, shifting, or storage of data.

SN54F299 . . . J PACKAGE  
SN74F299 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54F299 . . . FK PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN74F299N	SN74F299N
	SOIC – DW	Tube of 25	SN74F299DW	F299
		Reel of 2000	SN74F299DWR	
	SOP – NS	Reel of 2000	SN74F299NSR	74F299

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
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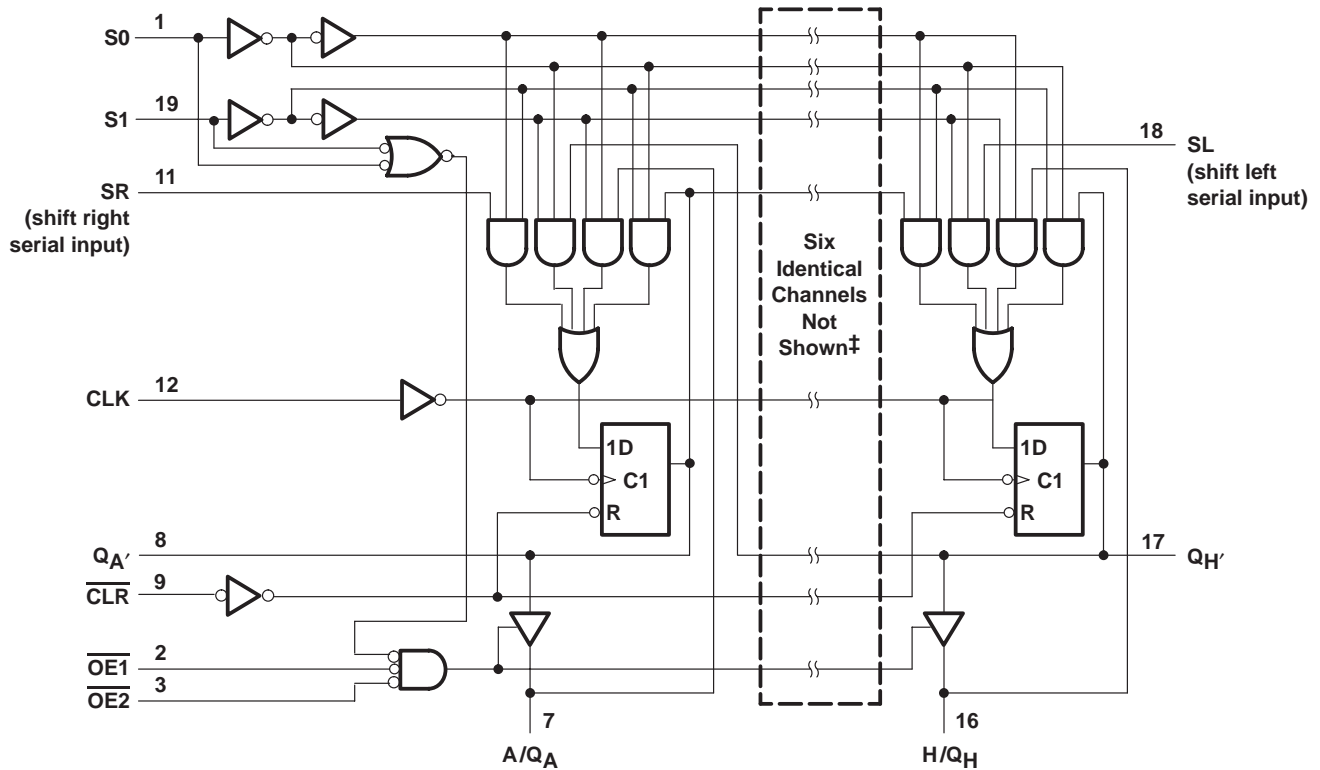
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS					
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '				
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L		
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L			L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>				
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>				
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>				
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>				
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H				
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L				
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h				

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

### logic diagram (positive logic)



‡ I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

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# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–1.2 V to 7 V
Input current range .....	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state .....	–0.5 V to 5.5 V
Voltage range applied to any output in the high state .....	–0.5 V to $V_{CC}$
Current into any output in the low state: $Q_{A'}$ or $Q_{H'}$ .....	40 mA
SN54F299 ( $Q_A$ thru $Q_H$ ) .....	40 mA
SN74F299 ( $Q_A$ thru $Q_H$ ) .....	48 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54F299			SN74F299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current	$Q_{A'}$ or $Q_{H'}$		–1	$Q_{A'}$ or $Q_{H'}$		–1	mA
		$Q_A$ thru $Q_H$		–3	$Q_A$ thru $Q_H$		–3	
$I_{OL}$	Low-level output current	$Q_{A'}$ or $Q_{H'}$		20	$Q_{A'}$ or $Q_{H'}$		20	mA
		$Q_A$ thru $Q_H$		20	$Q_A$ thru $Q_H$		24	
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

SDFS071B – MARCH 1987 – REVISED APRIL 2004

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F299			SN74F299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5 V, I_I = -18 mA$		-1.2			-1.2			V
$V_{OH}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5 V$	$I_{OH} = -1 mA$	2.5	3.4		2.5	3.4	V	
	$Q_A$ thru $Q_H$		$I_{OH} = -1 mA$	2.5	3.4		2.5	3.4		
			$I_{OH} = -3 mA$	2.4	3.3		2.4	3.3		
Any output		$V_{CC} = 4.75 V,$	$I_{OH} = -1 mA$ to $-3 mA$				2.7			
$V_{OL}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5 V$	$I_{OL} = 20 mA$	0.3		0.5	0.3		0.5	V
	$Q_A$ thru $Q_H$		$I_{OL} = 20 mA$	0.3		0.5				
			$I_{OL} = 24 mA$				0.35	0.5		
$I_I$	A thru H	$V_{CC} = 5.5 V$	$V_I = 5.5 V$	1			1			mA
	Any other		$V_I = 7 V$	0.1			0.1			
$I_{IH}‡$	A thru H	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$	70			70			$\mu A$
	Any other			20			20			
$I_{IL}‡$	A thru H	$V_{CC} = 5.5 V,$	$V_I = 0.5 V$	-0.65			-0.65			mA
	S0 or S1			-1.2			-1.2			
	Any other			-0.6			-0.6			
$I_{OS}§$		$V_{CC} = 5.5 V,$	$V_O = 0$	-60	-150		-60	-150		mA
$I_{CC}$		$V_{CC} = 5.5 V,$	See Note 4	68		95	68		95	mA

† All typical values are at  $V_{CC} = 5 V, T_A = 25^\circ C$ .

‡ For I/O ports ( $Q_A$  thru  $Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with  $\overline{OE}1, \overline{OE}2,$  and CLK at 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				$V_{CC} = 5 V,$ $T_A = 25^\circ C$		SN54F299		SN74F299		UNIT	
				'F299							
				MIN	MAX	MIN	MAX	MIN	MAX		
$f_{clock}$	Clock frequency			70		65		70		MHz	
$t_w$	Pulse duration		CLK high or low		7		8		7		ns
			$\overline{CLR}$ low		7		8		7		
$t_{su}$	Setup time before CLK↑		S0 or S1	High or low	8.5		9.5		8.5		ns
			A/ $Q_A$ thru H/ $Q_H$ , SR, or SL	High or low	5.5		6.5		5.5		
	Inactive-state setup time before CLK↑†		$\overline{CLR}$	High	7		13		7		
$t_h$	Hold time after CLK↑		S0 or S1	High or low	0		0		0		ns
			A/ $Q_A$ thru H/ $Q_H$ , SR, or SL	High or low	2		2		2		

† Inactive-state setup time also is referred to as recovery time.



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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			70	100		65		70	MHz	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.2	6.6	9	2.7	10.5	3.2	10	ns
t <sub>PHL</sub>			2.7	6.1	8.5	2.2	10	2.7	9.5	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	3.2	6.6	9	2.7	11	3.2	10	ns
t <sub>PHL</sub>			4.2	8.1	11	3.7	12.5	4.2	12	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q <sub>A</sub> thru Q <sub>H</sub>	5.7	10.6	14	5	15.5	5.7	15	
t <sub>PZH</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	2.7	5.6	8	2.2	10.5	2.7	9	ns
t <sub>PZL</sub>			3.2	6.6	10	2.7	12	3.2	11	
t <sub>PHZ</sub>	$\overline{\text{OE1}}$ or $\overline{\text{OE2}}$	Q <sub>A</sub> thru Q <sub>H</sub>	1.7	4.1	6	1.7	9	1.7	7	ns
t <sub>PLZ</sub>			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

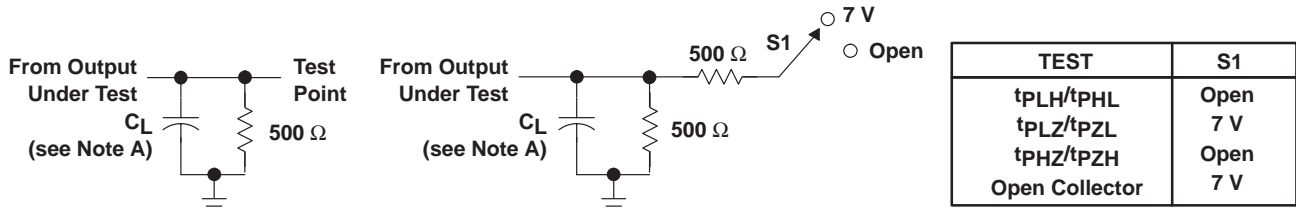
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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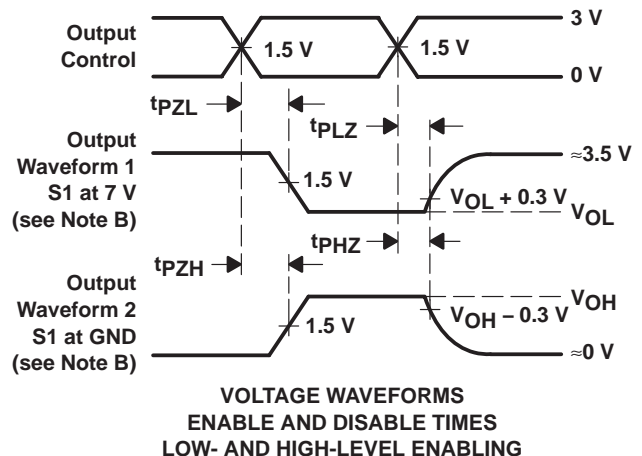
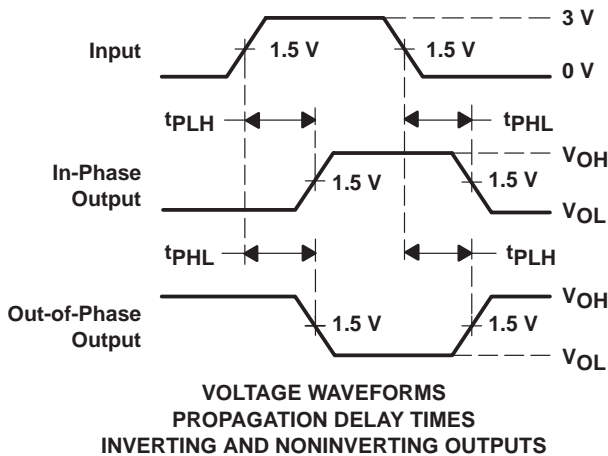
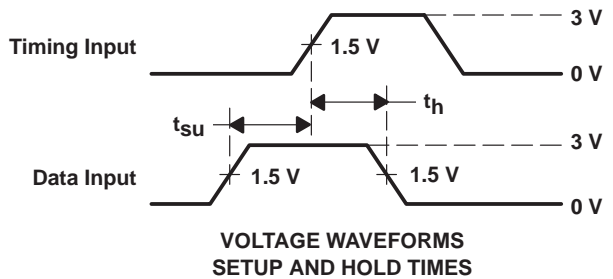
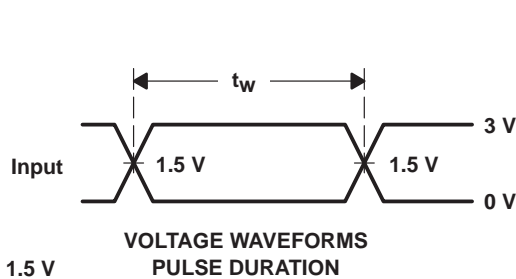
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## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.  
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

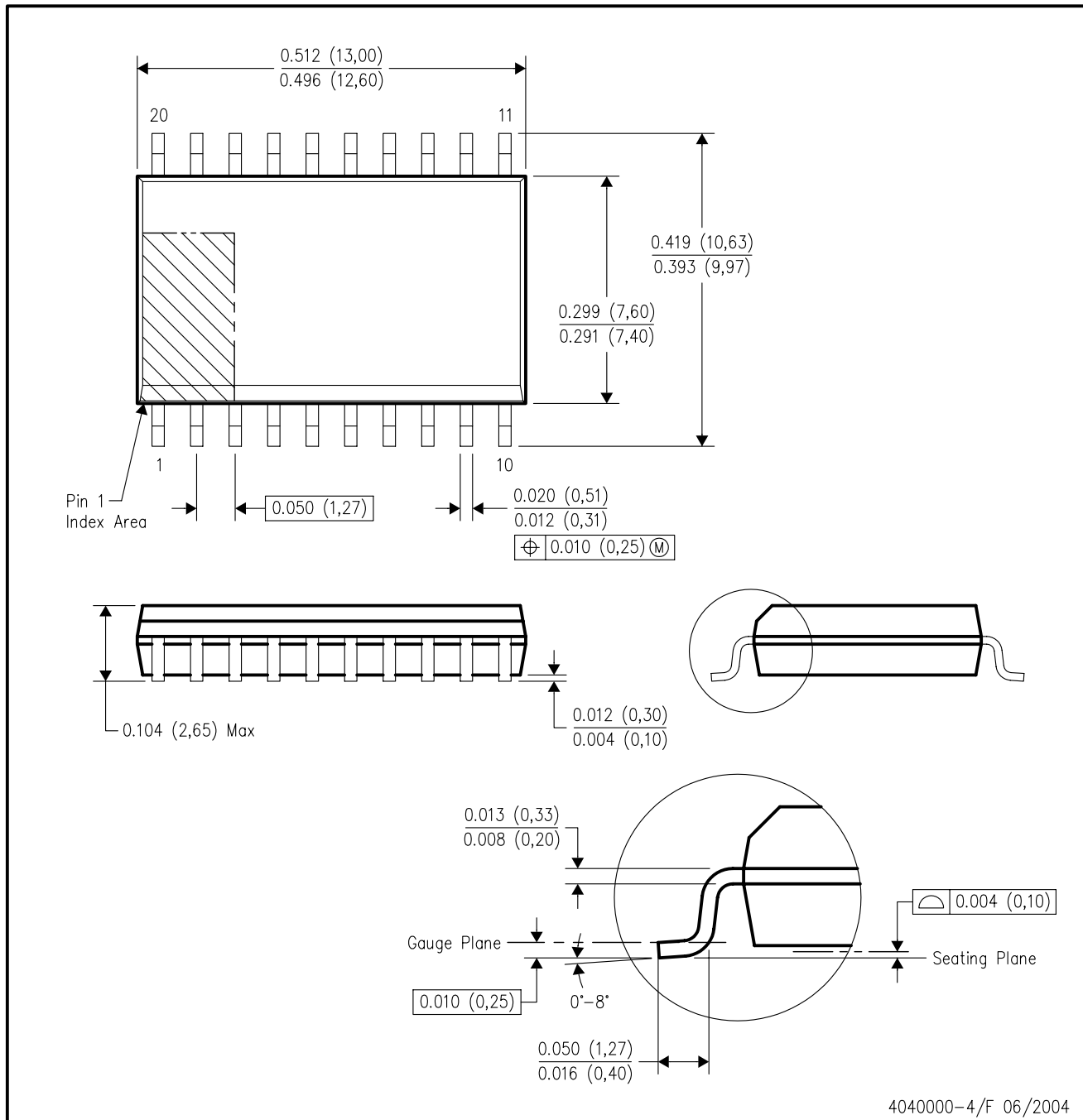
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments  
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