

# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for N-Bit Cascading
- Fully Synchronous Operation for Counting

## description

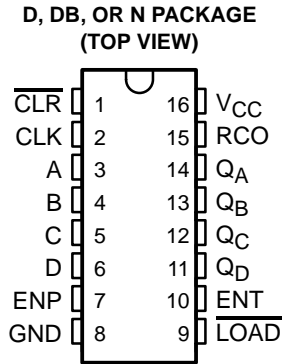
This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load ( $\overline{\text{LOAD}}$ ) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is synchronous, and a low logic level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs to low after the next low-to-high transition of the clock, regardless of the levels of ENP and ENT. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F163A features a fully independent clock circuit. Changes at ENP, ENT, or  $\overline{\text{LOAD}}$  that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F163AN	SN74F163AN
	SOIC – D	Tube	SN74F163AD	F163A
		Tape and reel	SN74F163ADR	
		SSOP – DB	Tape and reel	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

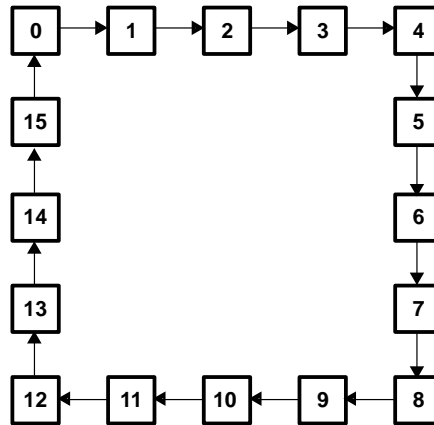
Copyright © 2001, Texas Instruments Incorporated

# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

---

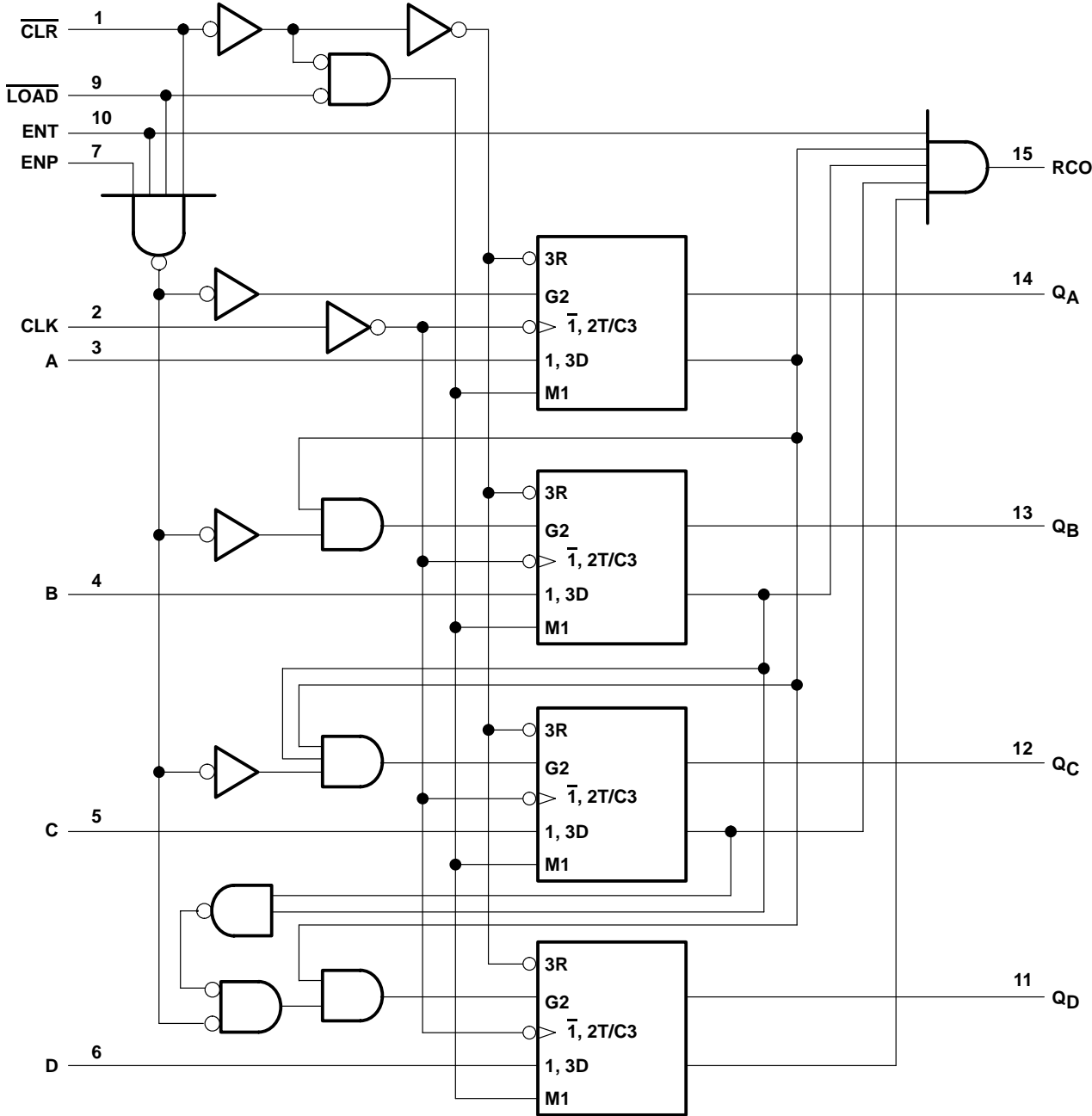
## state diagram



# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

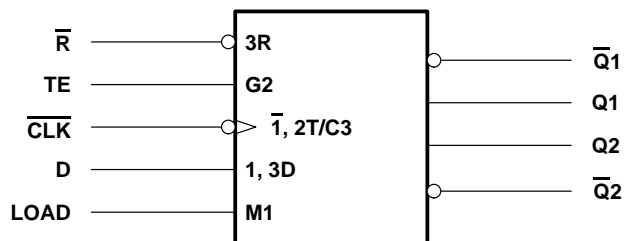
logic diagram (positive logic)



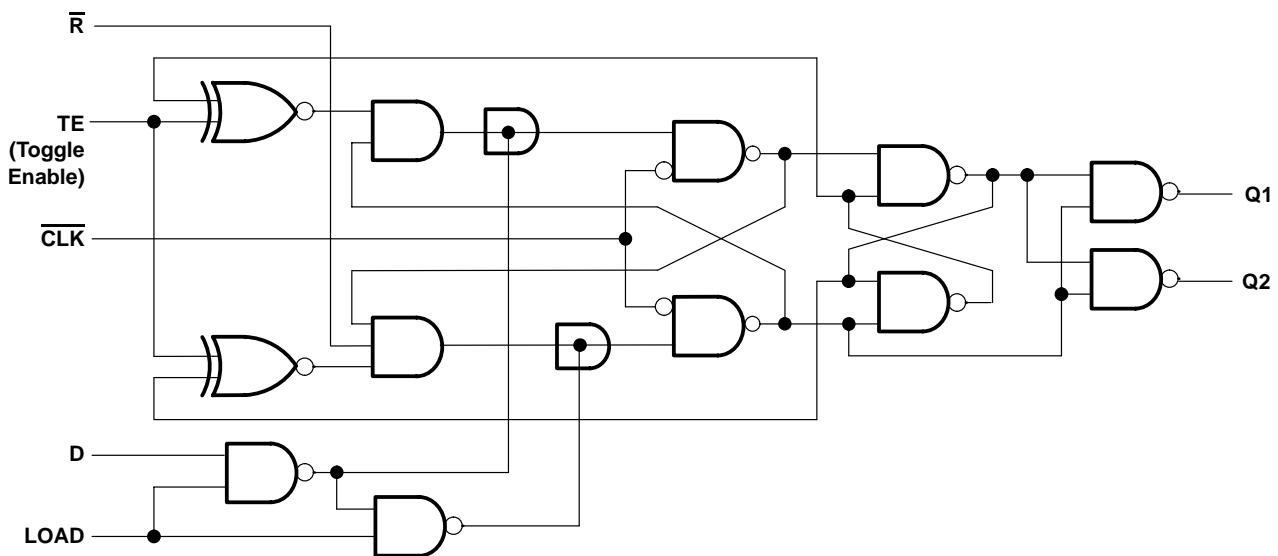
# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

## logic symbol, each flip-flop



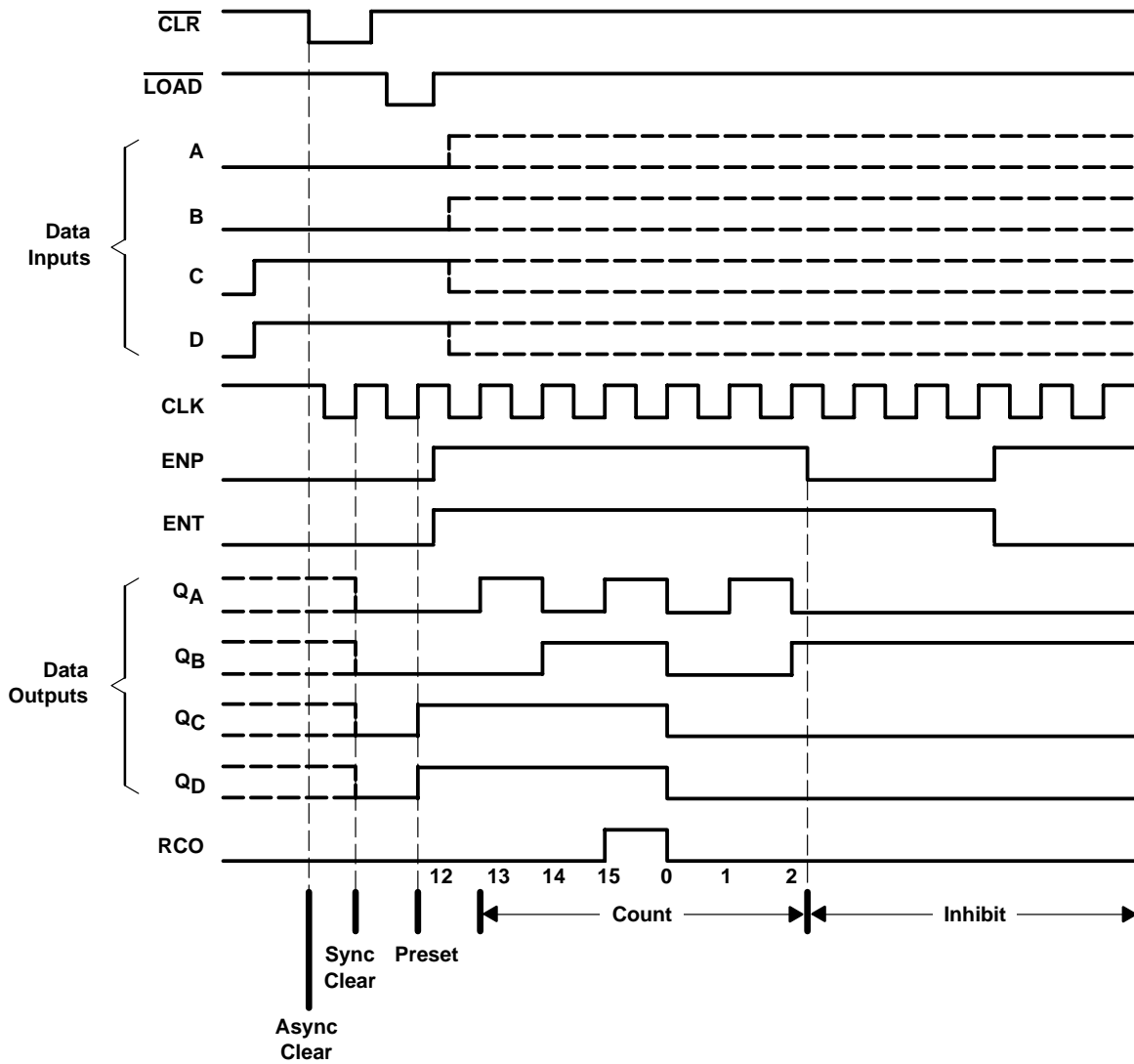
## logic diagram, each flip-flop (positive logic)



**typical clear, preset, count, and inhibit sequences**

The following timing sequence is illustrated below:

1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state	40 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{IK}$ Input clamp current			–18	mA
$I_{OH}$ High-level output current			–1	mA
$I_{OL}$ Low-level output current			20	mA
$T_A$ Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA	2.7			
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.3	0.5	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	µA
$I_{IL}$	ENP, CLK, A, B, C, D	$V_{CC} = 5.5$ V, $V_I = 0.5$ V		–0.6	mA
	ENT, LOAD			–1.2	
	CLR			–1.2	
$I_{OS}§$	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	mA
$I_{CC}$	$V_{CC} = 5.5$ V		37	55	mA

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f <sub>clock</sub>	Clock frequency		0	100	0	90	MHz
t <sub>w</sub>	Pulse duration	CLK high or low (loading)	5		5		ns
		CLK (counting)	High	4	4		
			Low	6	7		
t <sub>su</sub>	Setup time	Data before CLK↑	High or low	5	5		ns
		LOAD and CLR before CLK↑	High	11	11.5		
			Low	8.5	9.5		
		ENP and ENT before CLK↑	High	11	11.5		
			Low	5	5		
t <sub>h</sub>	Hold time	Data after CLK↑	High or low	2	2		ns
		LOAD and CLR after CLK↑	High	2	2		
			Low	0	0		
		ENP and ENT after CLK↑	High or low	0	0		

### switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 PF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V TO 5.5 V, C <sub>L</sub> = 50 PF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN TO MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			100	120		90		MHz
t <sub>PLH</sub>	CLK (LOAD high)	Any Q	2.7	5.1	7.5	2.7	8.5	ns
t <sub>PHL</sub>			2.7	7.1	10	2.7	11	
t <sub>PLH</sub>	CLK (LOAD low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns
t <sub>PHL</sub>			3.2	5.6	8.5	3.2	9.5	
t <sub>PLH</sub>	CLK	RCO	4.2	9.6	14	4.2	15	ns
t <sub>PHL</sub>			4.2	9.6	14	4.2	15	
t <sub>PLH</sub>	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
t <sub>PHL</sub>			1.7	4.1	7.5	1.7	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

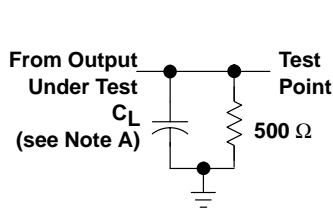
NOTE 4: Load circuits and waveforms are shown in Figure 1.



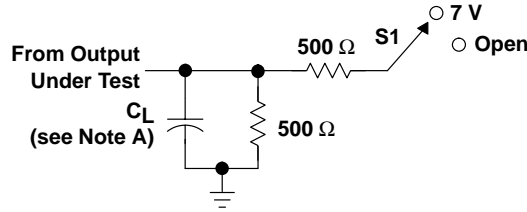
# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

## PARAMETER MEASUREMENT INFORMATION

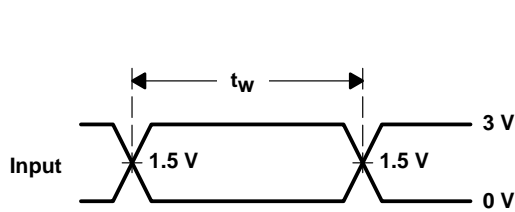


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

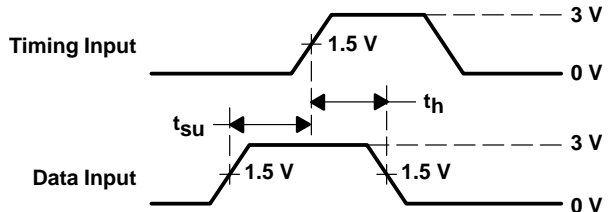


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

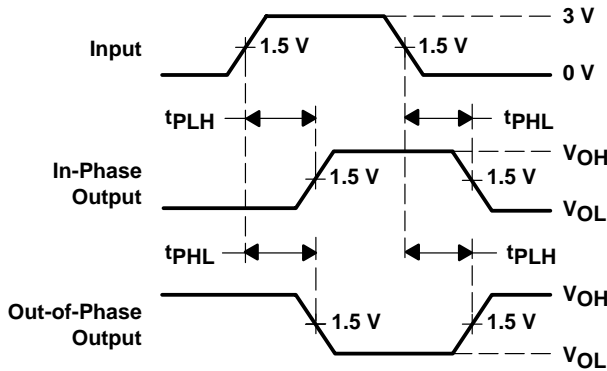
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open
Open Collector	7 V



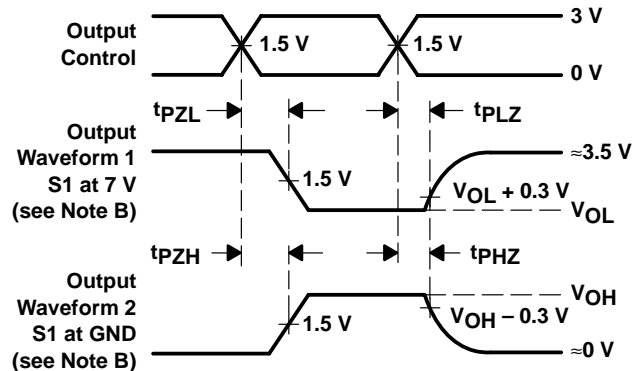
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265