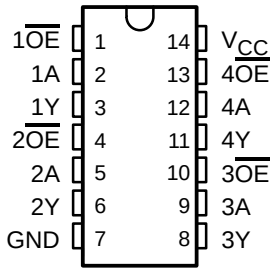
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

**D, DB, N, OR NS PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN74F125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

**ORDERING INFORMATION**

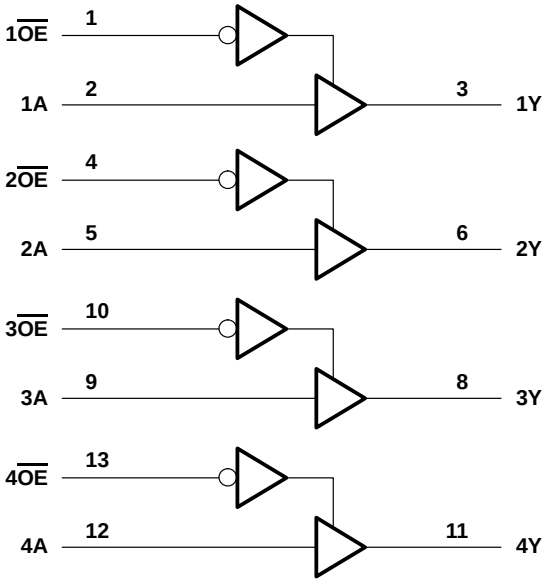
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP – N | Tube | SN74F125N | SN74F125N |
| | SOIC – D | Tube | SN74F125D | F125 |
| | | Tape and reel | SN74F125DR | |
| | SOP – NS | Tape and reel | SN74F125NSR | 74F125 |
| | SSOP – DB | Tape and reel | SN74F125DBR | F125 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . 128 mA
Current into any output in the low state . . . . . ±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | – 15 | mA |
| $I_{OL}$ | Low-level output current | | | 64 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | V |
| | | $I_{OH}$ = – 15 mA | 2 | 3.1 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 3 mA | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 64 mA | | 0.4 | 0.55 | V |
| $I_I$ | $V_{CC}$ = 0, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | –20 | µA |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | µA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –100 | | –225 | mA |
| $I_{CCH}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 17 | 24 | mA |
| $I_{CCL}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 28 | 40 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | Outputs open | | 25 | 35 | mA |

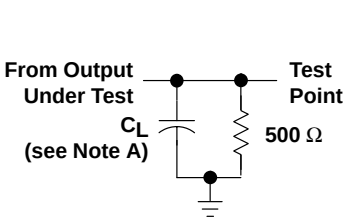
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Figure 1)

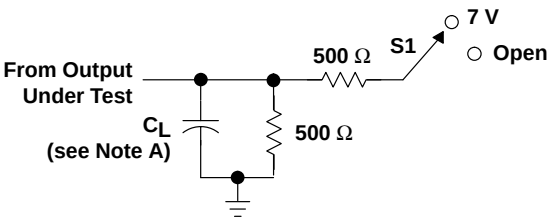
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.2 | 3.6 | 6 | 1.2 | 6.5 | ns |
| $t_{PHL}$ | | | 2.2 | 5.1 | 7.5 | 2.2 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 2.7 | 5.1 | 7.5 | 2.7 | 8.5 | ns |
| $t_{PZL}$ | | | 3.2 | 5.6 | 8 | 3.2 | 9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1 | 3.1 | 5 | 1 | 6 | ns |
| $t_{PLZ}$ | | | 1 | 3.1 | 5.5 | 1 | 6 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## PARAMETER MEASUREMENT INFORMATION

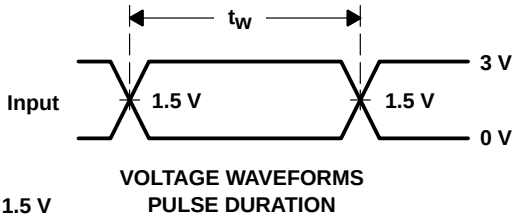



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

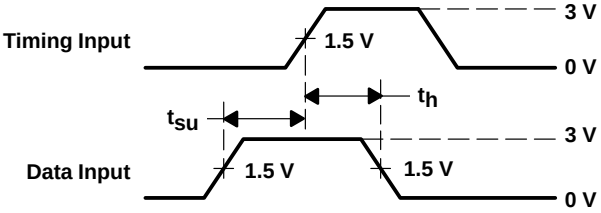



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |
| Open Collector | 7 V |

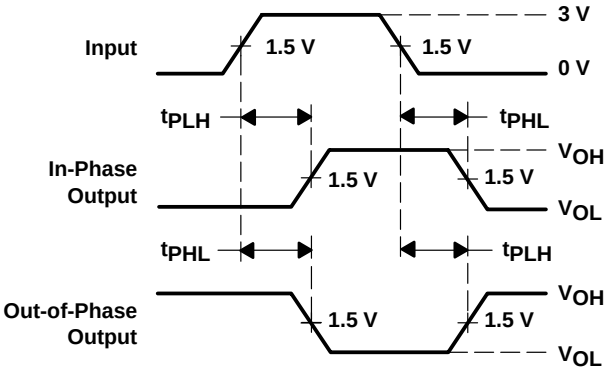



VOLTAGE WAVEFORMS
PULSE DURATION

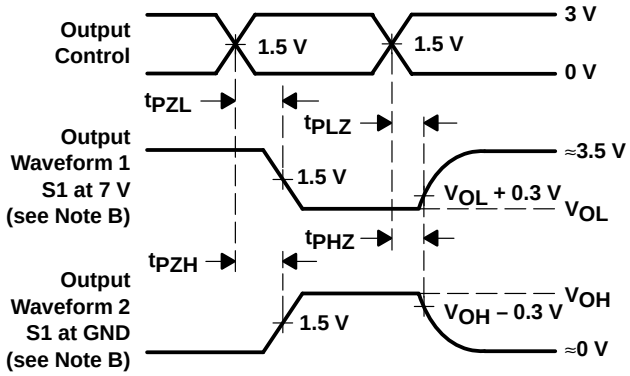



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

1.5 V




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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