

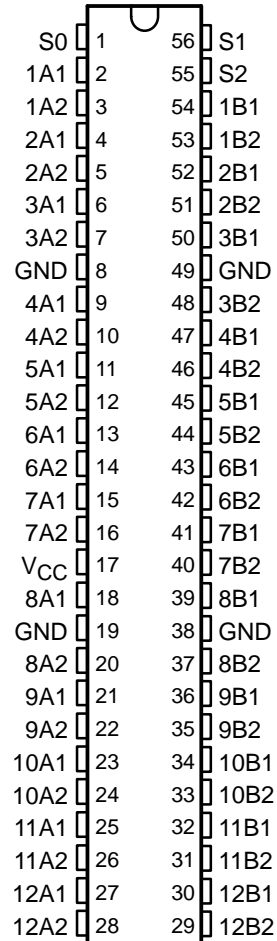
- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description

The SN74CBTS16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 24-bit bus switch or as a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBTS16212DL	CBTS16212
		Tape and reel	SN74CBTS16212DLR	
	TSSOP – DGG	Tape and reel	SN74CBTS16212DGGR	CBTS16212
	TVSOP – DGV	Tape and reel	SN74CBTS16212DGVR	CYS212

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN74CBTS16212
24-BIT FET BUS-EXCHANGE SWITCH
WITH SCHOTTKY DIODE CLAMPING

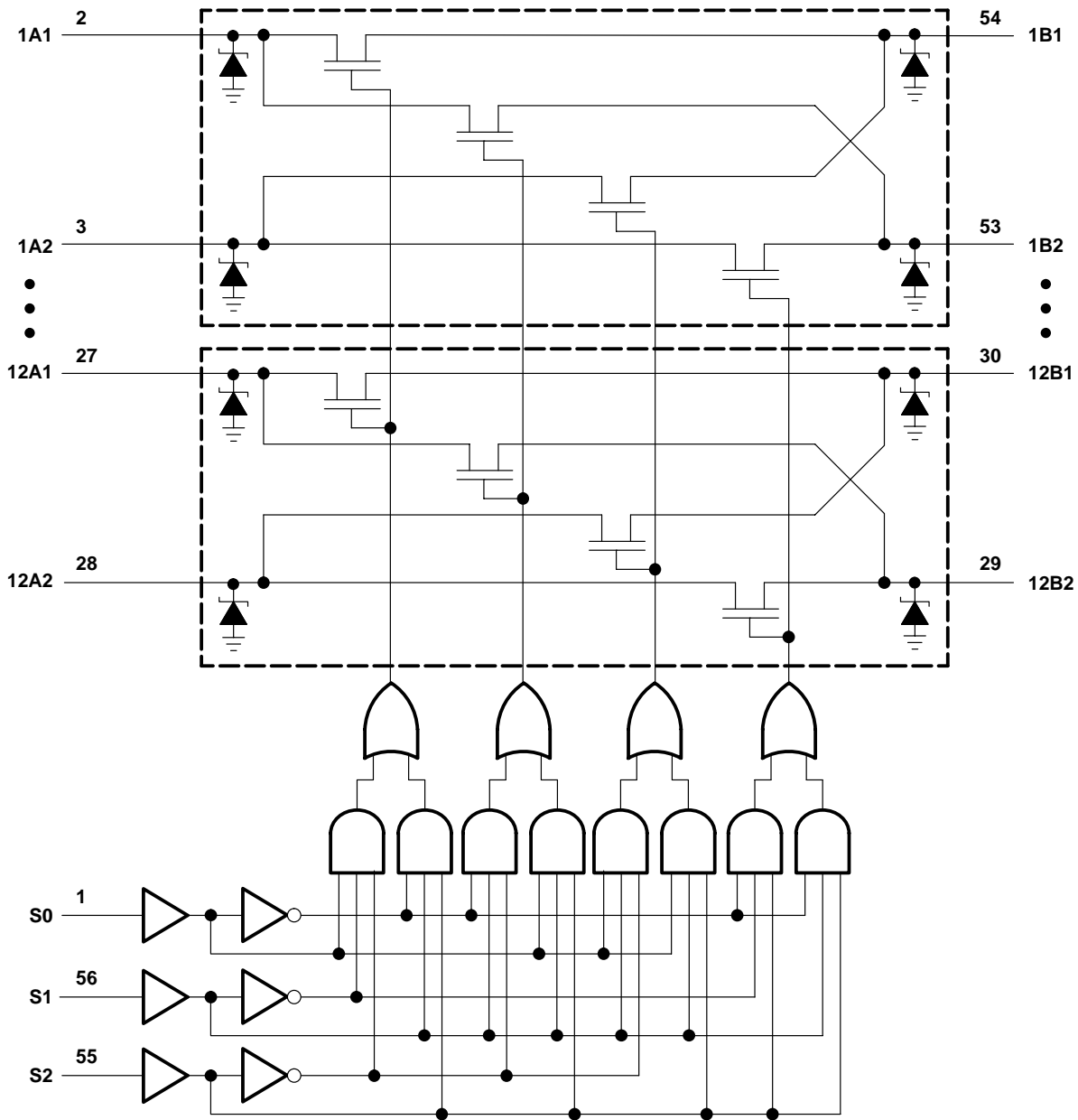
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FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port



logic diagram (positive logic)



SN74CBTS16212

24-BIT FET BUS-EXCHANGE SWITCH WITH SCHOTTKY DIODE CLAMPING

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA				–1.2	V
I_I	I_{IL}	$V_{CC} = 5.5$ V, $V_I = GND$			–1	μ A
	I_{IH}	$V_{CC} = 5.5$ V, $V_I = 5.5$ V			150	
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND				3	μ A
ΔI_{CC} §	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3$ V or 0		2.5		pF
$C_{io(OFF)}$		$V_O = 3$ V or 0, $S_0, S_1,$ and $S_2 = GND$		10.5		pF
r_{on} ¶	$V_{CC} = 4$ V, $V_I = 2.4$ V, $I_I = 15$ mA				20	Ω
	$V_{CC} = 4.5$ V	$V_I = 0$		4	7	
		$V_I = 2.4$ V, $I_I = 30$ mA		4	7	
		$V_I = 2.4$ V, $I_I = 15$ mA		6	12	

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

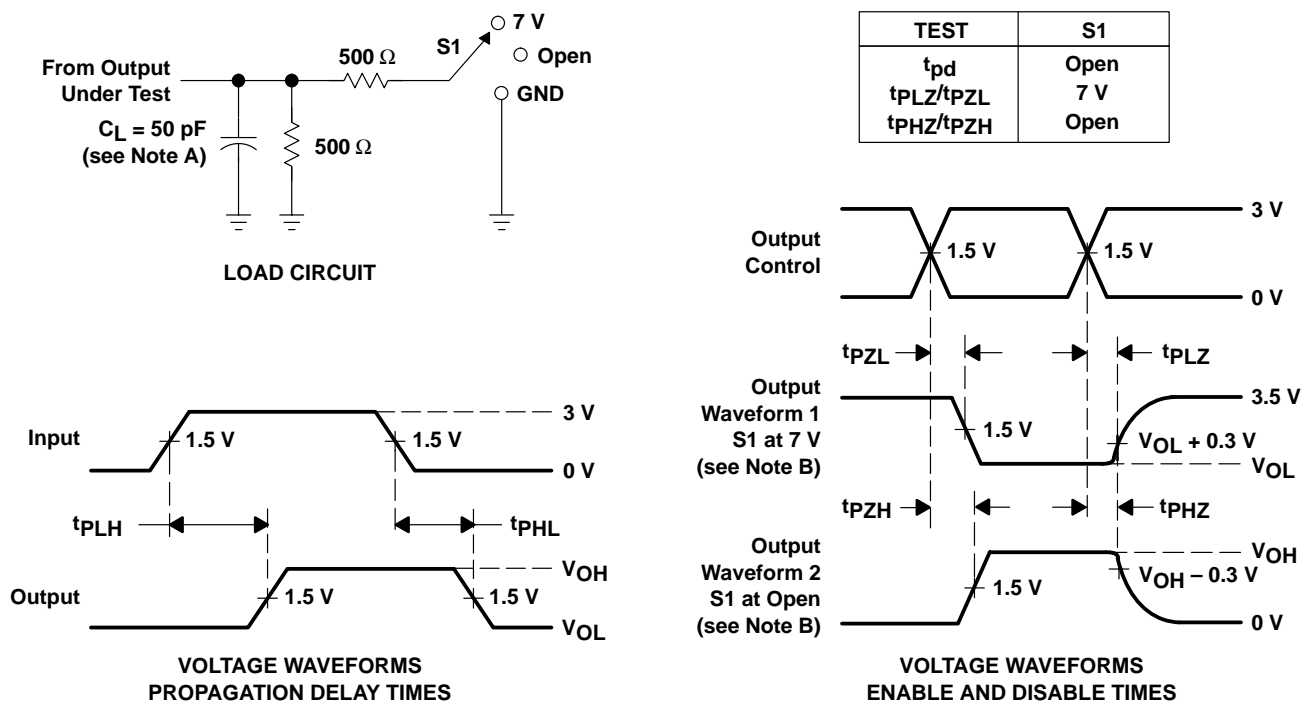


switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^\dagger	A or B	B or A	0.35		0.25		ns
t_{pd}	S	A or B	10		1.5	9.1	ns
t_{en}	S	A or B	10.4		1.5	9.7	ns
t_{dis}	S	A or B	9.2		1.5	8.8	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω , $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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