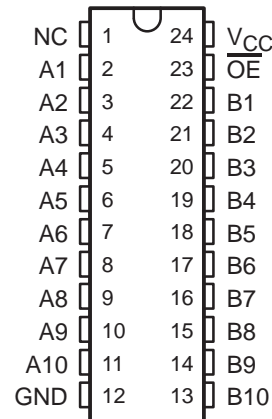


# SN74CBTLV3861 LOW-VOLTAGE 10-BIT FET BUS SWITCH

SCDS041H – DECEMBER 1997 – REVISED OCTOBER 2003

- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DBQ, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN74CBTLV3861 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 10-bit bus switch. When output enable ( $\overline{OE}$ ) is low, the 10-bit bus switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – DBQ	Tape and reel	SN74CBTLV3861DBQR	CL861
	SOIC – DW	Tube	SN74CBTLV3861DW	CBTLV3861
		Tape and reel	SN74CBTLV3861DWR	
	SOP – NS	Tape and reel	SN74CBTLV3861NSR	CBTLV3861
	TSSOP – PW	Tape and reel	SN74CBTLV3861PWR	CL861
TVSOP – DGV	Tape and reel	SN74CBTLV3861DGV	CL861	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

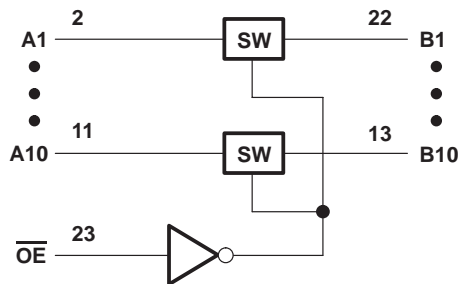
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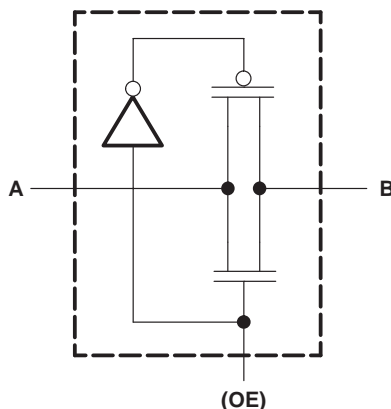
# SN74CBTLV3861 LOW-VOLTAGE 10-BIT FET BUS SWITCH

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## logic diagram (positive logic)



## simplified schematic, each FET switch



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 4.6 V
Continuous channel current .....	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DBQ package .....	61°C/W
DGV package .....	86°C/W
DW package .....	46°C/W
NS package .....	65°C/W
PW package .....	88°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V <sub>IK</sub>		V <sub>CC</sub> = 3 V,	I <sub>I</sub> = -18 mA			-1.2	V	
I <sub>I</sub>		V <sub>CC</sub> = 3.6 V,	V <sub>I</sub> = V <sub>CC</sub> or GND			±1	μA	
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V			10	μA	
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V,	I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			10	μA	
ΔI <sub>CC</sub> ‡	Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V, Other inputs at V <sub>CC</sub> or GND			300	μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0				3	pF	
C <sub>io(OFF)</sub>		V <sub>O</sub> = 3 V or 0,	$\overline{OE}$ = V <sub>CC</sub>			5	pF	
r <sub>on</sub> §	V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA			5	8	Ω
			I <sub>I</sub> = 24 mA			5	8	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 1.7 V,	I <sub>I</sub> = 15 mA			27	40	
			I <sub>I</sub> = 64 mA			5	7	
	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0	I <sub>I</sub> = 24 mA			5	7	
			I <sub>I</sub> = 15 mA			10	15	

† All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A	0.15		0.25		ns
t <sub>en</sub>	$\overline{OE}$	A or B	2.1	5.5	2.1	4.9	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	1.7	5.5	2.5	5.8	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

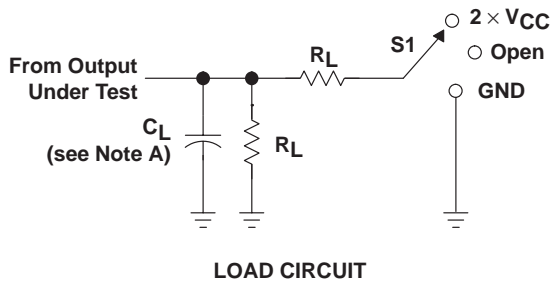


# SN74CBTLV3861

## LOW-VOLTAGE 10-BIT FET BUS SWITCH

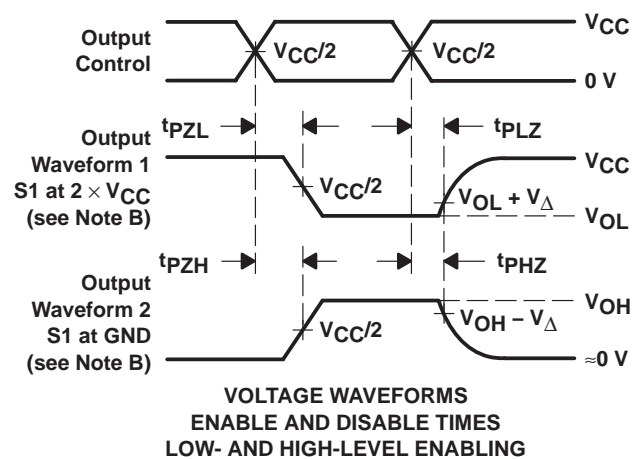
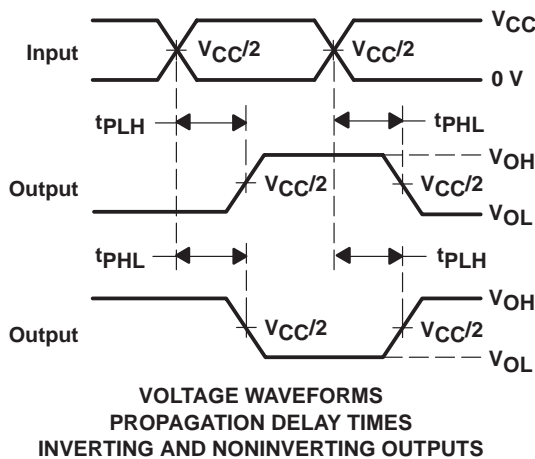
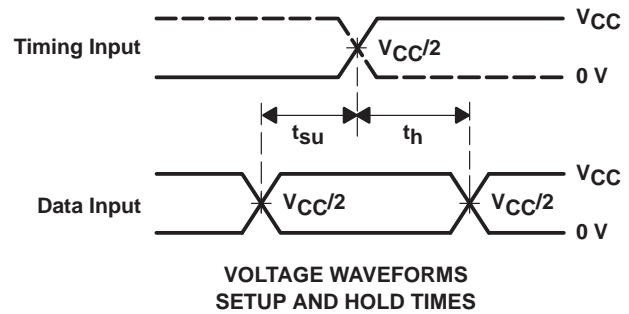
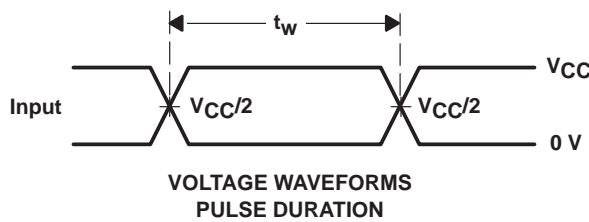
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### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 $\Omega$	0.3 V



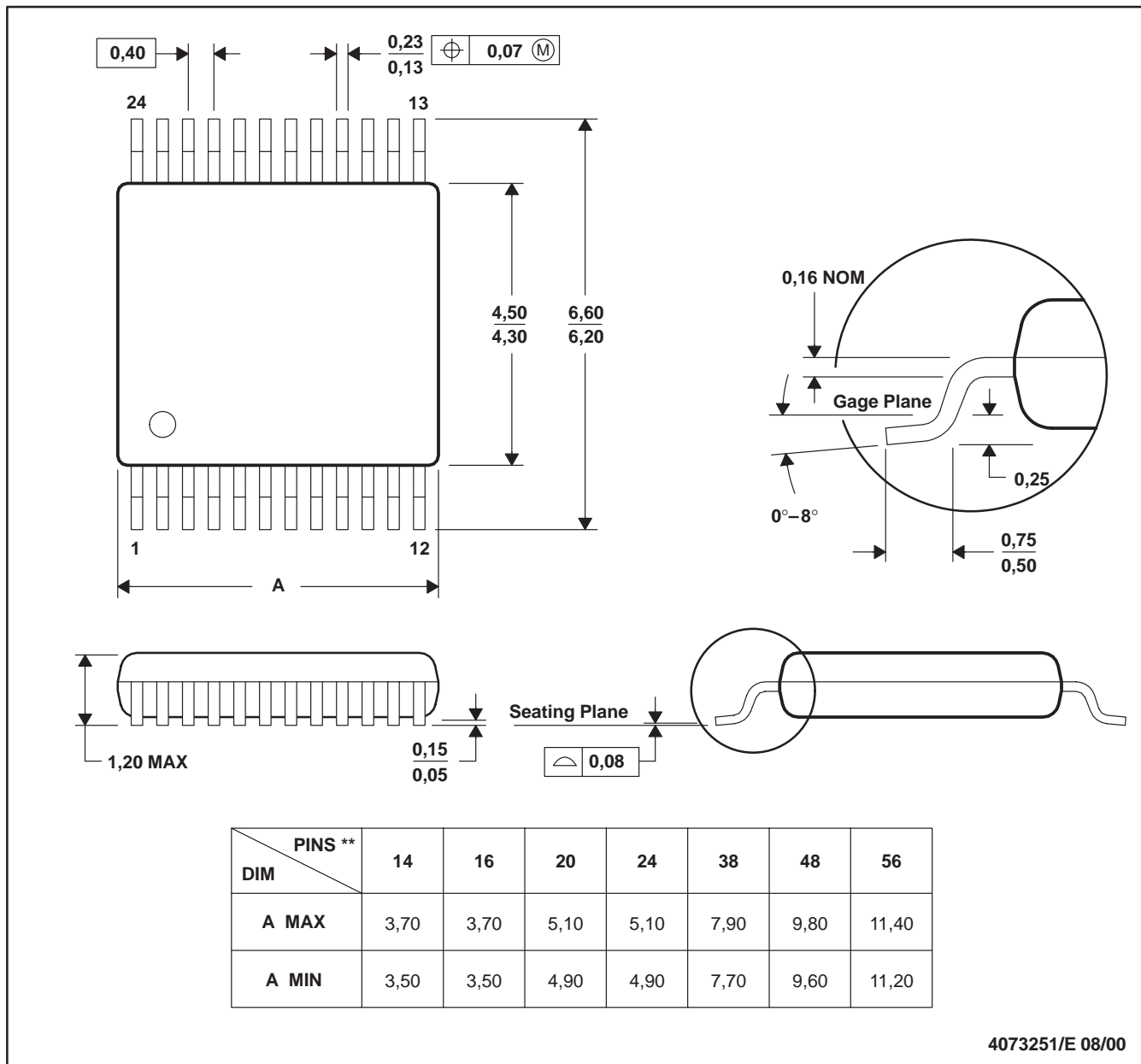
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



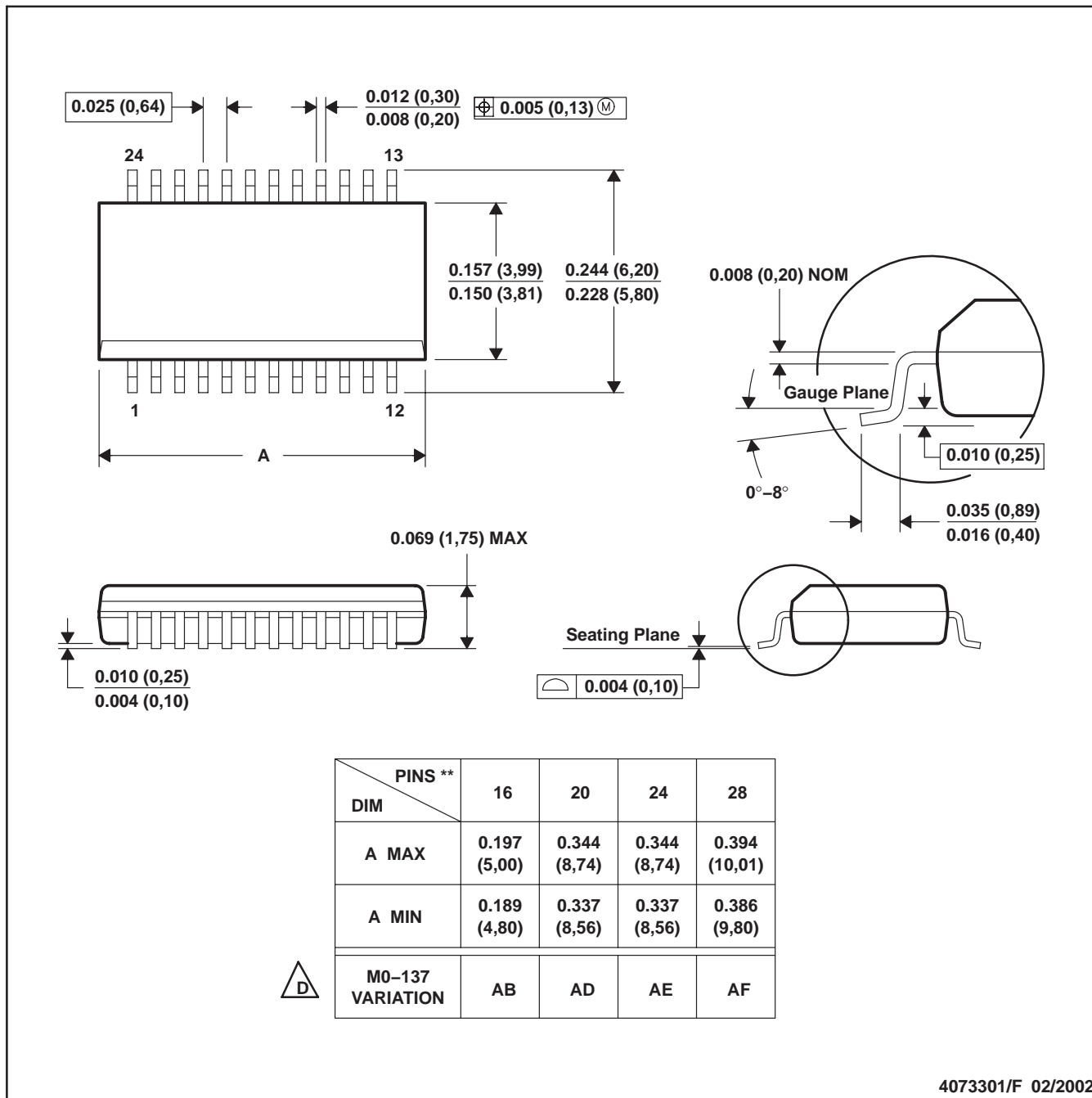
4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



DBQ (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-137.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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