

SN74CBTLV3384

LOW-VOLTAGE 10-BIT FET BUS SWITCH

SCDS059G – MARCH 1998 – REVISED JUNE 2004

- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

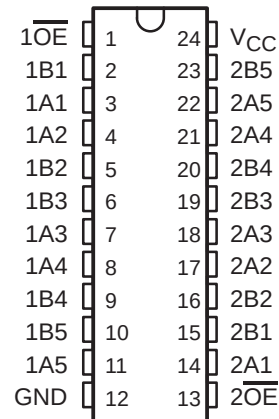
The SN74CBTLV3384 provides ten bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. It can be used as two 5-bit bus switches or one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is on, and A port is connected to B port. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – DBQ	Tape and reel	SN74CBTLV3384DBQR	CBTLV3384
	SOIC – DW	Tube	SN74CBTLV3384DW	CBTLV3384
		Tape and reel	SN74CBTLV3384DWR	
	TSSOP – PW	Tape and reel	SN74CBTLV3384PWR	CL384
	TVSOP – DGV	Tape and reel	SN74CBTLV3384DGV	CL384

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$\overline{1OE}$	$\overline{2OE}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

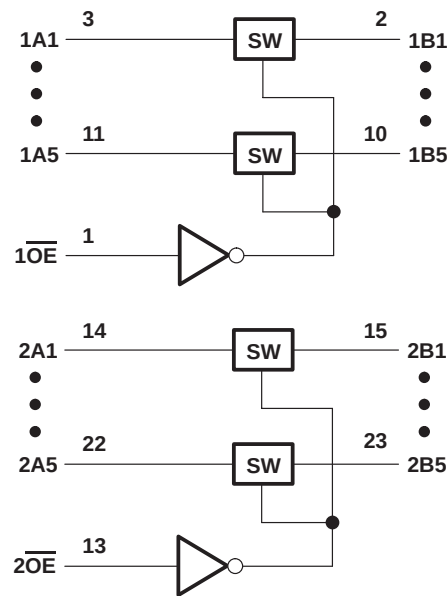
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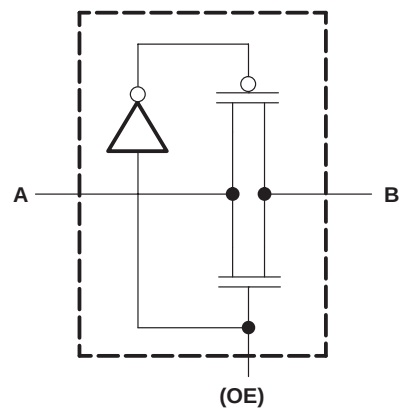
SN74CBTLV3384 LOW-VOLTAGE 10-BIT FET BUS SWITCH

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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{IO} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	
T_A	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$				-1.2	V
I_I		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND				±1	μA
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 3.6 V				10	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND				10	μA
$\Delta I_{CC}^{\ddagger}$	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V, Other inputs at V_{CC} or GND				300	μA
C_i	Control inputs	$V_I = 3\text{ V or }0$				4.5	pF
$C_{io(OFF)}$		$V_O = 3\text{ V or }0$, $\overline{OE} = V_{CC}$				10	pF
$r_{on}^{\S}$	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$		5	8	Ω
			$I_I = 24\text{ mA}$		5	8	
		$V_I = 1.7\text{ V}$	$I_I = 15\text{ mA}$		27	40	
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$		5	7	
			$I_I = 24\text{ mA}$		5	7	
		$V_I = 2.4\text{ V}$	$I_I = 15\text{ mA}$		10	15	

[†] All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{\parallel}$	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	5	1	4.3	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	5.5	ns

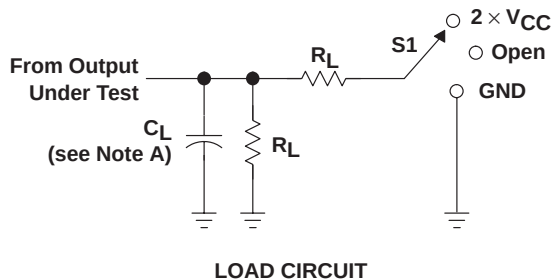
^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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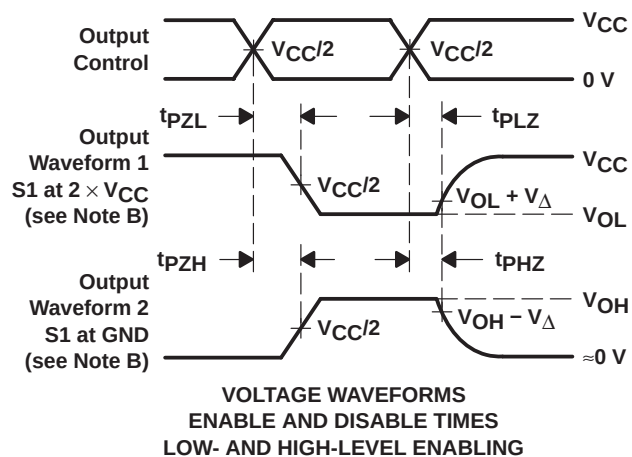
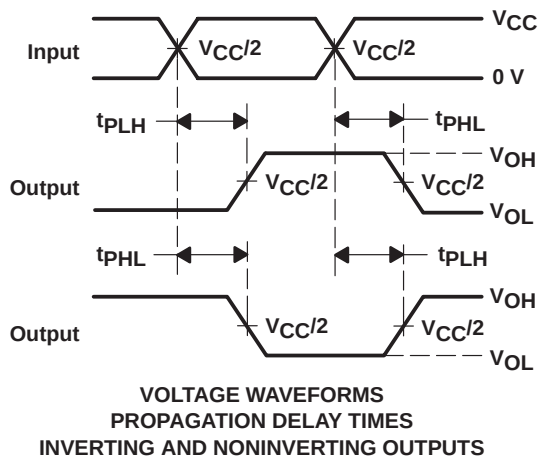
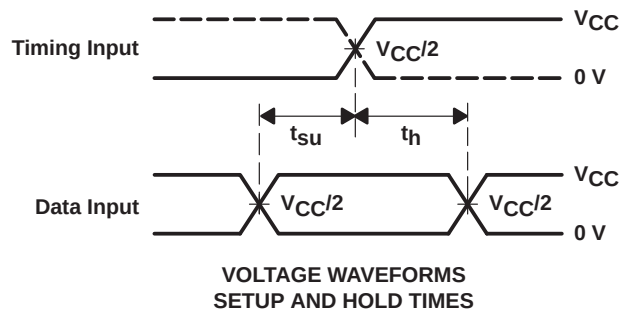
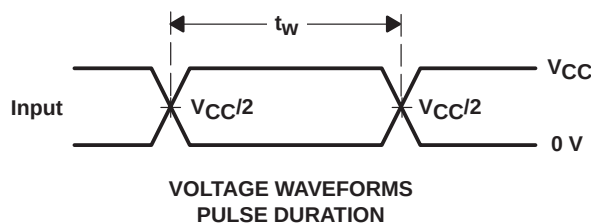
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 Ω	0.3 V



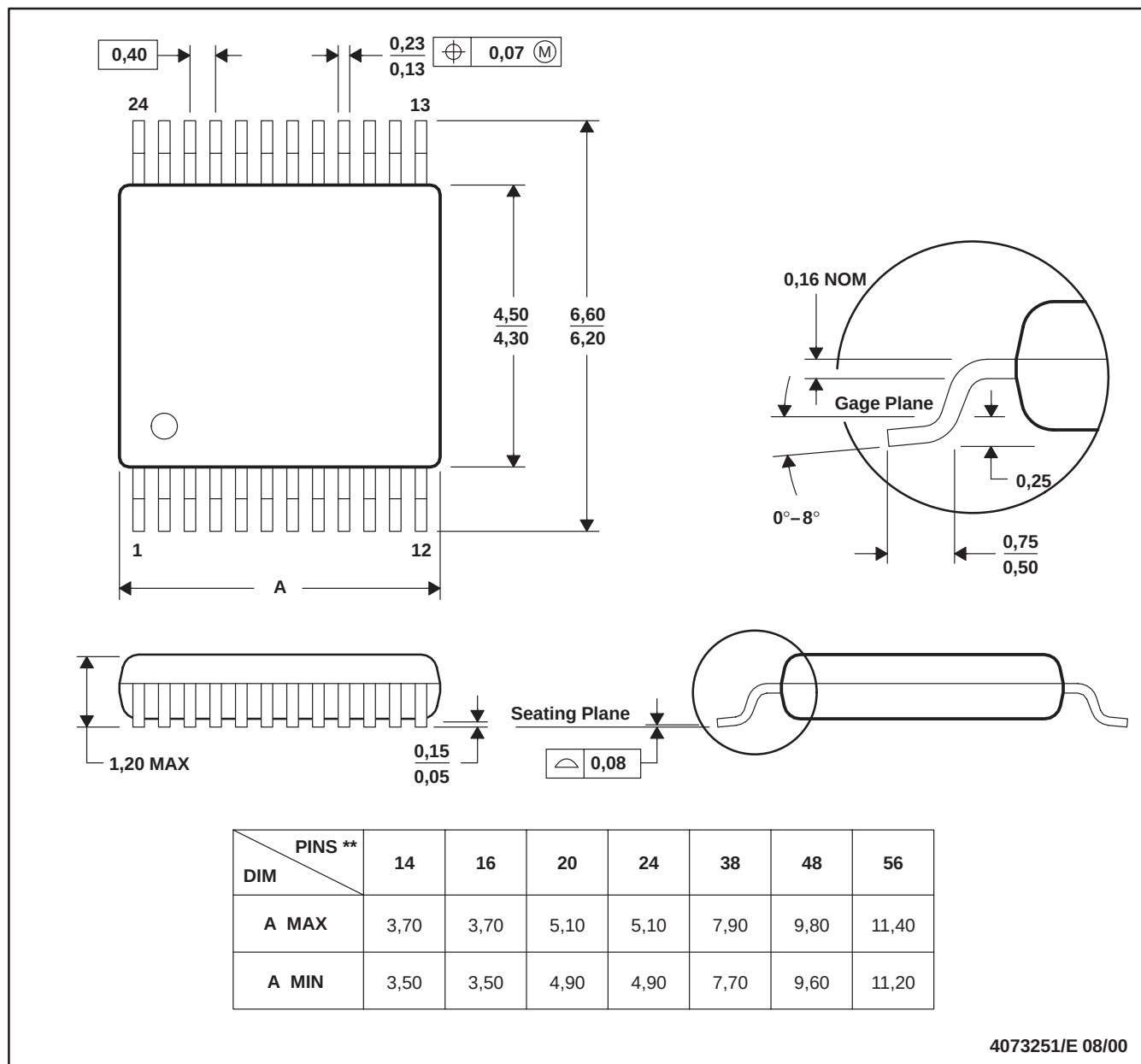
- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

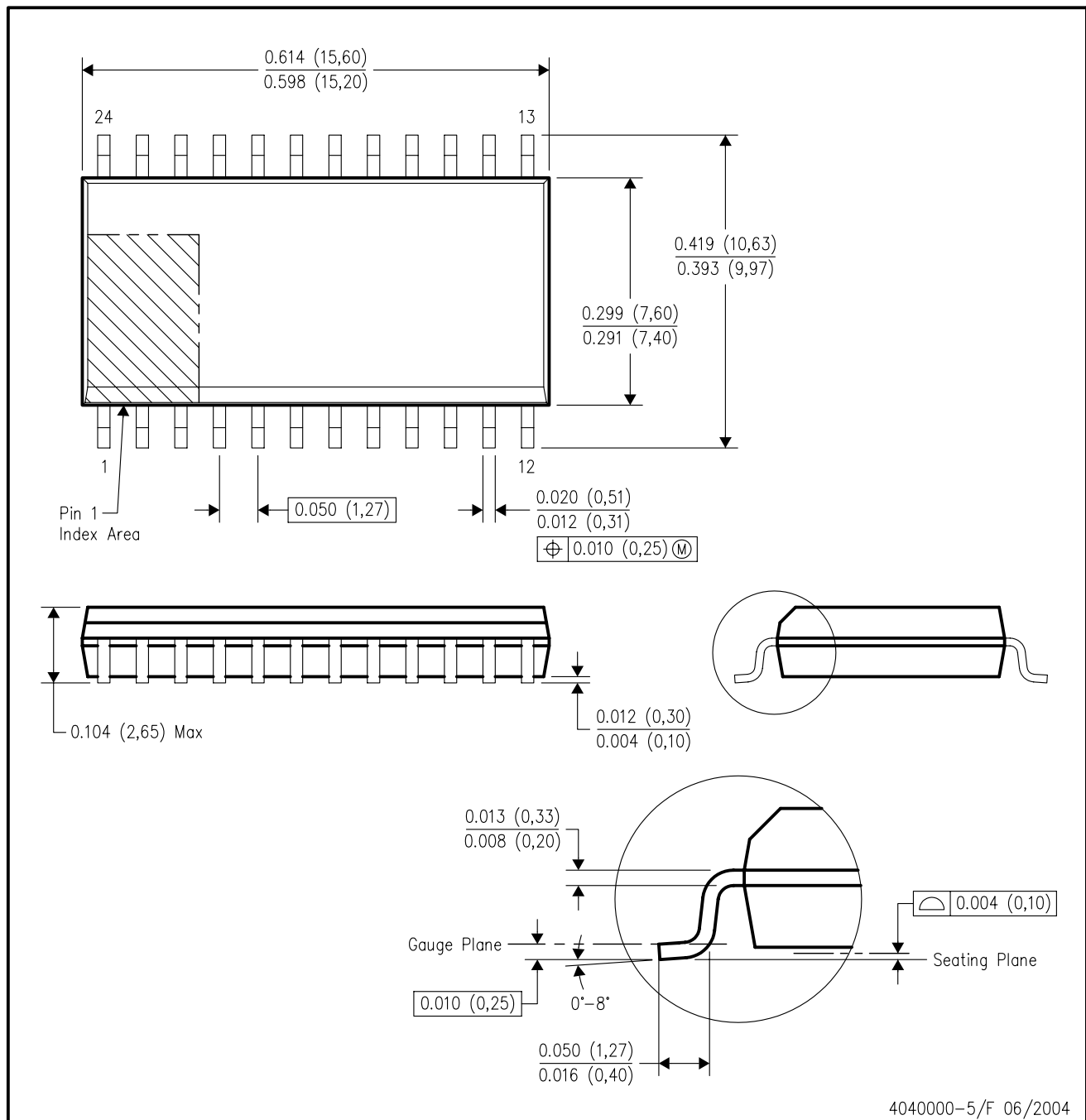
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

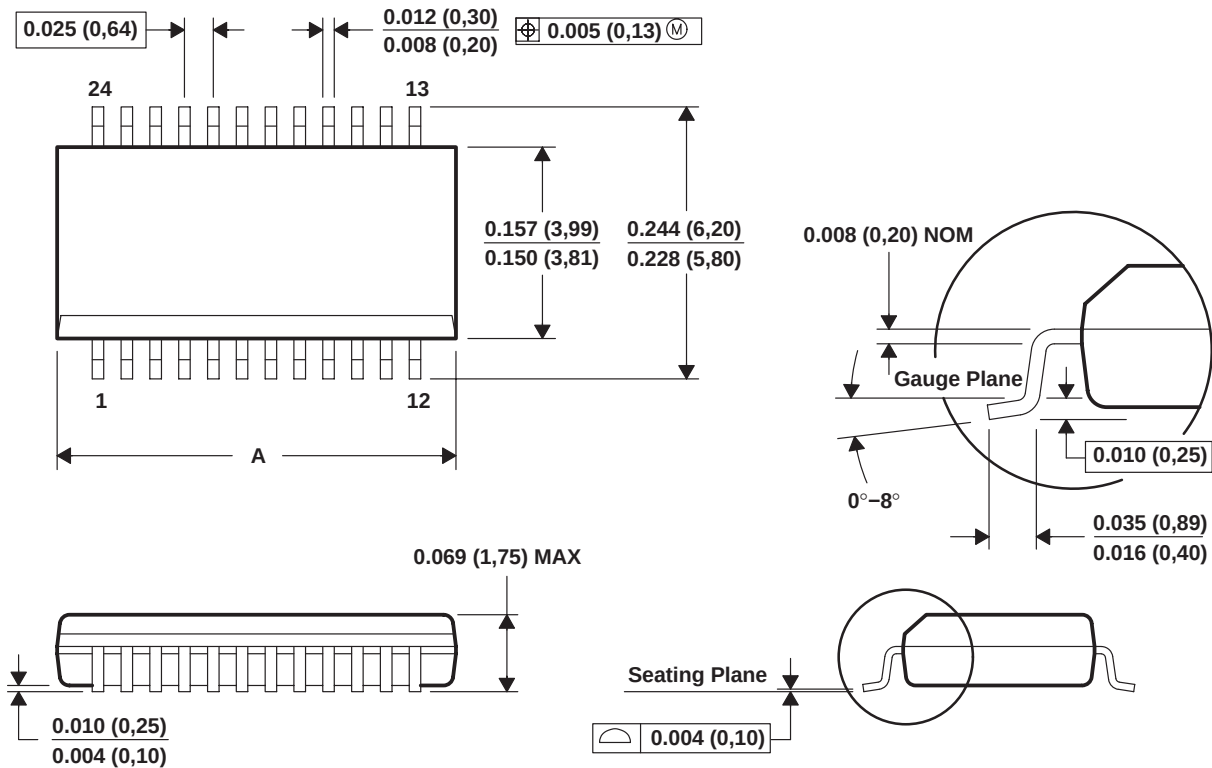
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	16	20	24	28
DIM				
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
M0-137 VARIATION	AB	AD	AE	AF

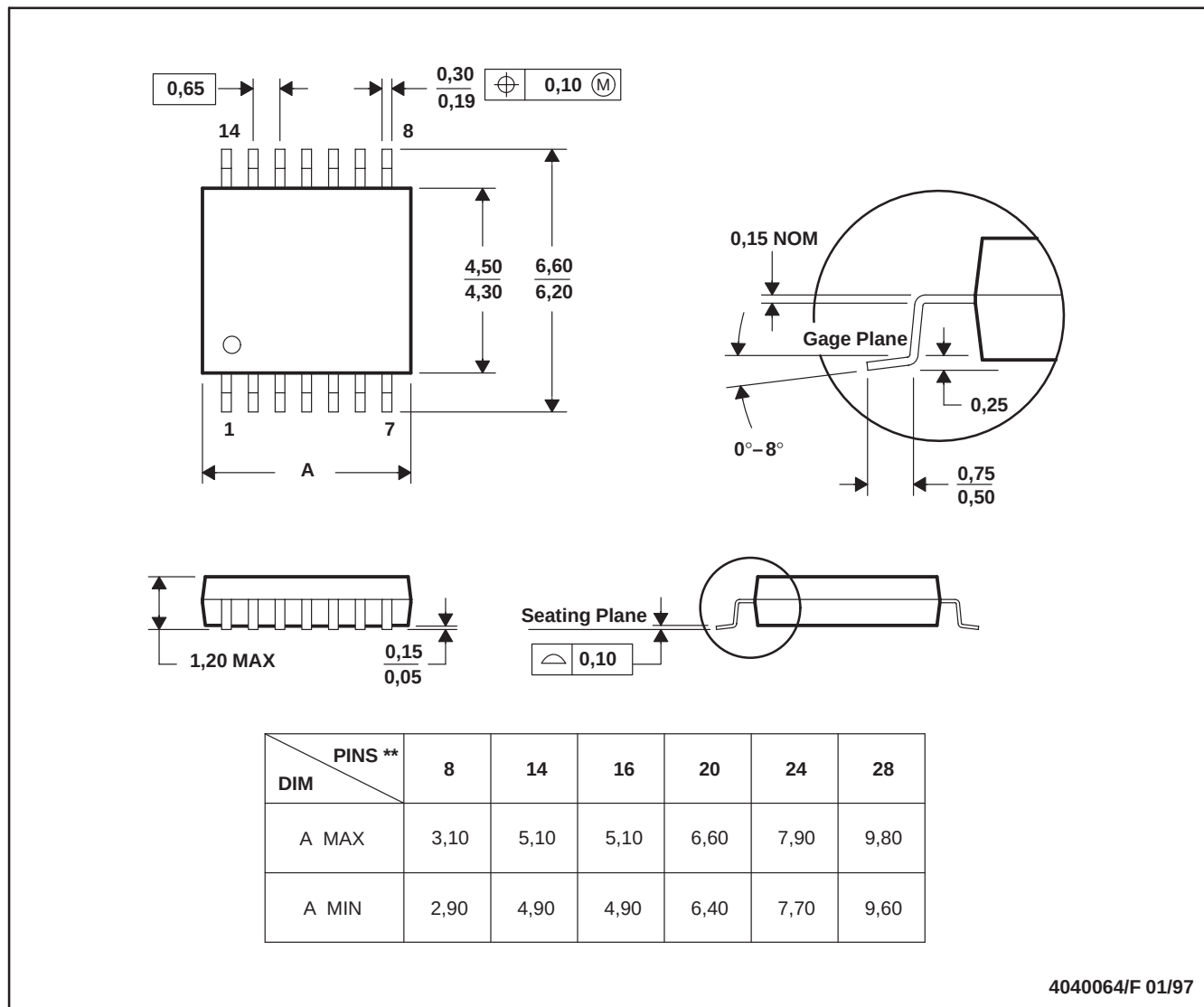
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- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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